INTI International University & Colleges

FINAL
Examination Paper

(COVER PAGE)

Session	:	**AUGUST 2019**
		Diploma In Information Technology (DITN)
Course	:	**ICT2101: Computer Organization**
Date of Examination	:	December 12, 2019 (Thursday)
Time	:	2:00pm – 4:00pm Reading Time : Nil
Duration	:	2 Hours

Special Instructions :

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided.

Materials permitted :
Calculator

Materials provided :
Nil

Examiner(s) : **Ryan Tee Ah Ann** and Kavitha Thamadharan

Moderator : Mohd Faizal Bin Alias

*This paper consists of **5** printed pages, including the cover page*

DIPLOMA IN INFORMATION TECHNOLOGY PROGRAMME (DITN)
ICT2101: COMPUTER ORGANISATION
FINAL EXAMINATION: AUGUST 2019 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

(a) Define the following terms.

(i) System Bus
(ii) Data Bus
(iii) Address Bus
(iv) Control Bus (8 marks)

(b) Each virtual machine is an abstraction of the level below it. The machines at each level execute their own particular instructions, calling upon machines at lower levels to perform tasks as required. List and explain the **SEVEN (7)** levels in layered approach.

(14 marks)

(c) How does Assembly Language relate to Machine Language? (3 marks)

(Total: 25 marks)

Question 2

(a) What are the **advantages** and **disadvantages** of having

(i) large register size? (4 marks)

(ii) small register size? (4 marks)

(b) Perform the following conversion:

(i) Decimal 99 to hexadecimal (2 marks)

(ii) Binary 110010 to decimal (2 marks)

(iii) Integer -78 to 8-bit two's complement binary (2 marks)

(c) Suppose the contents of registers are as follow:

AX = 0008 BX = 0019 CS = 305E DS = 4FF9

IP = 0025 SI = 1005

Find out the following:

(i) The logical and physical address for the next instruction. (4 marks)

(ii) If the instruction SUB AL, BL is executed, what is the value of register AX, carry flag and overflow flag?

(3 marks)

(iii) Give the instruction that store the result of subtraction (SUB AL, BL) in 2(c)(ii) in memory location 1000 of the data segment by using indexed addressing mode.

(4 marks)

(Total: 25 marks)

Question 3

(a) What is data 'overflow'? Illustrate it with an example. (5 marks)

(b) Trace the following program and write down the value of register AX and CL. The first two lines already filled up for you.

(10 marks)

	AX	CL
MOV AX,0307_H	0307	?
MOV CX,0005_H	0307	05
MUL AH		
AAM		
AND CX,$00F4_H$		
INC CL		

XCHG AL,CL		

(c) With regards to the fetch and execute cycle of 8086,

(i) What is the function of instruction pointer (IP)? (2 marks)

(ii) What is the function of instruction queue? (2 marks)

(iii) Provide two situations where the cycle is broken. (6 marks)

(Total: 25 marks)

Question 4

(a) The register content for an Intel 8086 microprocessor is as follows:
CS = 4000h, DS = 2000h, SS = 3000h, SI = 5000h, DI = 6000h,
BX = 5060h, BP = 7010h, AX = 5022h, CX = 5653h, DX = 8008h

Calculate the physical address of the memory where the operand is stored and the contents of the memory locations in each of the addresses as shown below:

(i) MOV [SI], AL
(ii) MOV [DI + 6h], BX
(iii) MOV [SI + BX – 5h], AX
(iv) MOV [DI][BX] + 10h, CX (16 marks)

(b) Comment and justify on the validity of the following addressing modes:

(i) MOV AX, [CADFh]
(ii) MOV [1A00h], [1ADh]
(iii) MOV AX, [BP]
(iv) MOV DS, CS (8 marks)

(c) What is the advantage of pipelined architecture in fetch and execute cycle? (1 mark)

(Total: 25 marks)

Question 5

(a) Explain what subroutine in detail. (6 marks)

(b) Explain the cache operation in detail. (10 marks)

(c) What is page fault? Explain the algorithm of page fault. (9 marks)

(Total: 25 marks)

Question 6

(a) There are different ways to achieve memory protection. These include segmentation and paging. Explain how it works. (10 marks)

(b) With the aids of flowchart (s), explain the **THREE (3)** modes of Direct Memory Access (DMA). (15 marks)

(Total: 25 marks)

~The End~