

 **INTI International  
University & Colleges**

**FINAL  
Examination Paper**

(COVER PAGE)

Session : APRIL 2018

Programme : Diploma In Information And Communication Technology (DICTN)  
Diploma In Information Technology (DITN)

Course : ICT2101: Computer Organization

Date of Examination : 28 July, 2018 (Saturday)

Time : 11:00am – 1:00pm Reading Time : Nil

Duration : 2 Hours

**Special Instructions :**

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided.

Materials permitted : Nil

Materials provided : Nil

Examiner(s) : Tee Ah Ann and Kavitha Thamadharan

Moderator : Mohd Faizal Bin Alias

*This paper consists of 6 printed pages, including the cover page*

DIPLOMA IN INFORMATION AND COMMUNICATION TECHNOLOGY PROGRAMME  
(DICTN)  
DIPLOMA IN INFORMATION TECHNOLOGY PROGRAMME (DITN)  
ICT2101: COMPUTER ORGANISATION  
FINAL EXAMINATION: APRIL 2018 SESSION

**Instruction:** This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

**Question 1**

- (a) Explain the data processing cycle with a diagram. (12 marks)
- (b) Explain the term assembly language and give **ONE (1)** example to illustrate the usage of such language. (5 marks)
- (c) Each virtual machine layer is an abstraction of the level below it. Complete the following table: (8 marks)

<i>Level 6</i>	<i>User Level</i>	<i>(i)</i>
<i>Level 5</i>	<i>(ii)</i>	<i>C++, Java, Fortran</i>
<i>Level 4</i>	<i>(iii)</i>	<i>(iv)</i>
<i>Level 3</i>	<i>System Software</i>	<i>(v)</i>
<i>Level 2</i>	<i>(vi)</i>	<i>Instruction Set Architecture</i>
<i>Level 1</i>	<i>Control</i>	<i>(vii)</i>
<i>Level 0</i>	<i>(viii)</i>	<i>Circuits, Gates</i>

**(Total: 25 marks)**

**Question 2**

(a) Convert the following by showing the working (without using calculator).

- i.  $85_{10}$  to base 2
- ii.  $D4_{16}$  to base 2
- iii.  $30_{10}$  to base 8
- iv.  $01011011_2$  to base 10
- v.  $10011010_2$  to base 16

(10 marks)

(b) The Bus Interface Unit (BIU) is programmed to fetch a new instruction whenever the queue has room for two additional bytes. Explain what are the **THREE (3)** conditions that will cause the execution unit to enter a “wait” mode?

(9 marks)

(c) Explain the following registers.

- i. Destination Index
- ii. Source Index
- iii. Base Pointer

(6 marks)

**(Total: 25 marks)**

**Question 3**

(a) Briefly describe the following addressing modes with an example.

- i. Direct Addressing
- ii. Based Addressing
- iii. Register Indirect Addressing

(15 marks)

(b) Demonstrate by using binary on how an 8bit two's complement computer system will perform the following:

i.  $79 - 42$

(4 marks)

ii.  $65 + 13$

(3 marks)

iii.  $28 + 12$

(3 marks)

**(Total: 25 marks)**

#### Question 4

(a) Assume the following register conditions:

AX = ADEFh, BX = 4175h, CX = 9695h, DX = 55AAh

Find the status of Carry Flag (CF), Parity Flag (PF), Auxiliary Flag (AF), Zero Flag (ZF) and Sign Flag (SF) for the following operations:

- i. MOV BX, 8Fh  
ADD BL, 7Eh
- ii. CMP BX, CX
- iii. NOT BX
- iv. ADD AX, DX

(10 marks)

(b) Develop an assembly language program to perform the arithmetic operations below by only using registers AX and BX.

$$18_{10} * (225_{10} - 165_{10}) + 85_{10}$$

(5 marks)

(c) A pipeline hazard is anything that disrupts orderly flow of data through the pipeline flow. There are three types of hazards which are structural hazards, data hazards and branch hazards. Discuss the **THREE (3)** situations that causes data hazard to occur and explain **TWO (2)** ways how data hazard can be eliminated.

(10 marks)

**(Total: 25 marks)**

**Question 5**

(a) The register content for an Intel 8086 microprocessor is as follows:

CS = 4000h, DS = 5000h, SS = 3000h, SI = 5000h, DI = 6000h,  
 BX = 5060h, BP = 7050h, AX = 5022h, CX = 3206h, DX = 7227h

Calculate the physical address of the memory where the operand is stored and the contents of the memory locations in each of the addresses as shown below:

i. MOV [SI], AL (2 marks)

ii. MOV [DI + 6h], BX (3 marks)

iii. MOV [SI + BX - 5h], AX (3 marks)

iv. MOV [DI][BX] + 10h, CX (3 marks)

(b) Comment and justify on the validity of the following addressing modes:

- i. MOV [100Ah], AX
- ii. MOV [1F00h], [1ACh]
- iii. MOV AX, [BP]
- iv. MOV DS, CS
- v. MOV AX, 10110011b

(10 marks)

(c) Explain the following arithmetic instruction with an example:

- i. IMUL
- ii. IDIV

(4 marks)

**(Total: 25 marks)**

**Question 6**

- (a) Cache memory is high speed memory that is used to store frequently accessed instructions or data. Explain the **TWO (2)** locality of reference in cache memory. (10 marks)
- (b) Explain the interrupt driven input/output with an aid of diagram. (10 marks)
- (c) Discuss the characteristics of Reduced Instruction Set Computer (RISC). (5 Marks)

**(Total: 25 marks)**

**~ The End ~**  
*Ict2101(f)/april2018*