INTI International University & Colleges

FINAL
Examination Paper

(COVER PAGE)

Session	:	**AUGUST 2017**
Programme	:	Diploma In Information And Communication Technology (DICTN)
Course	:	**ICT2101: Computer Organization**
Date of Examination	:	7 December, 2017 (Thursday)
Time	:	2:00 pm – 4:00 pm Reading Time : Nil
Duration	:	2 Hours

Special Instructions :

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Materials permitted :

Nil

Materials provided :

Nil

Examiner(s) : **Tee Ah Ann** and Kavitha a/p Thamadharan

Moderator : Mohd Faizal Bin Alias

This paper consists of 5 printed pages, including the cover page

DIPLOMA IN INFORMATION AND COMMUNICATIONS TECHNOLOGY PROGRAMME (DICTN)
ICT2101: COMPUTER ORGANISATION
FINAL EXAMINATION: AUGUST 2017 SESSION

Instruction: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

(a) Von Neumann architecture consists of three primary components. Explain all **THREE (3)** components. (6 marks)

(b) List and explain the **THREE (3)** of system bus. (6 marks)

(c) What are the **TWO (2)** separate processing units in 8086 microprocessor? Explain the steps involved in fetch and execute cycle in 8086 microprocessor. (13 marks)

Question 2

(a) Discuss the characteristics differences between CISC and RISC in term of their design architecture. (10 marks)

(b) Briefly explain what pipeline structure in computer organization design perspective is. (6 marks)

(c) Provide **TWO (2)** advantages of using pipeline structure as mentioned in **Q2 (b)**. (4 marks)

(d) Discuss why interrupt is better than polling in handling I/O for a computer system. (5 marks)

Question 3

(a) Convert the following.

(i) 50_{10} to base 8 (2 marks)

(ii) 1011_2 to base 10 (2 marks)

(iii) 1111_2 to base 16 (2 marks)

(iv) $AE2_{16}$ to base 10 (2 marks)

(v) $3EF_{16}$ to base 2 (2 marks)

(b) Briefly describe the following addressing modes and provide an example.

(i) Immediate Addressing (4 marks)

(ii) Register Addressing (4 marks)

(c) Demonstrate using binary how an 8 bit two's complement computer system will perform the following:

(i) 84 – 42 (4 marks)

(ii) 75 + 23 (3 marks)

Question 4

(a) Assume the following register conditions:
AX = DEAFh, BX = 1845h, CX = 2255h, DX = 55FFh

Find the status of Carry Flag (CF), Parity Flag (PF), Auxiliary Flag (AF), Zero Flag (ZF) and Sign Flag (SF) for the following operations:

(i) MOV BX, 5Fh
ADD BL, AFh

(ii) CMP BX, CX

(iii) NOT BX

(iv) ADD AX, DX

(20 marks)

(b) Develop an assembly language program to perform the arithmetic operations below by only using registers AX and BX.

$$15_{10} * (220_{10} - 185_{10}) + 135$$

(5 marks)

Question 5

(a) The register content for an Intel 8086 microprocessor is as follows:
CS = 4000h, DS = 2000h, SS = 3000h, SI = 5000h, DI = 6000h,
BX = 5060h, BP = 7010h, AX = 5022h, CX = 5653h, DX = 8008h

Calculate the physical address of the memory where the operand is stored and the contents of the memory locations in each of the addresses as shown below:

(i) MOV [SI], AL

(ii) MOV [DI + 6h], BX

(iii) MOV [SI + BX – 5h], AX

(iv) MOV [DI][BX] + 10h, CX (8 marks)

(b) Comment and justify on the validity of the following addressing modes:

(i) MOV AX, [AAFFh]
(ii) MOV [1F00h], [1ACh]
(iii) MOV AX, [BP]
(iv) MOV DS, CS (8 marks)

(c) Explain the following logic instructions with example using assembly language.

(i) AND
(ii) OR
(iii) XOR (9 marks)

Question 6

(a) Cache memory is high speed memory that is used to store frequently accessed instructions or data. Explain the cache operations in brief. (10 marks)

(b) Explain how cache hit can occur. (4 marks)

(c) A pipeline hazard is anything that disrupts orderly flow of data through the pipeline flow. There are three types of hazards which are structural hazards, data hazards and branch hazards.

(i) Explain what data hazard is. (1 mark)
(ii) Discuss the **THREE (3)** situations that causes data hazard to occur. (6 marks)
(iii) Explain **TWO (2)** ways how data hazard can be eliminated. (4 marks)

~The End~