INTI International College Penang

FINAL
ALTERNATIVE ASSESSMENT

(COVER PAGE)

Session	:	**January 2021**
Programme	:	Diploma in Electrical & Electronic Engineering (DEEI)
Course	:	**EEE2101: Introduction to Digital Electronics**
Date of Examination	:	9 March 2021 (Tuesday)
Time	:	8.00am – 11.00am Reading Time : Nil
Duration	:	3 Hours

Special Instructions :

This paper consists of **FOUR (4)** questions. Answer **ALL** questions. All questions carry equal marks.

Material permitted : Non-Programmable Scientific Calculator

Materials provided : Nil

Examiner(s)	:	**Steven Khoo Boo Tap**
Chief Moderator	:	Chan Tse Wei

*This paper consists of **8** printed pages, including the cover page*

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE2101: INTRODUCTION TO DIGITAL ELECTRONICS
FINAL ALTERNATIVE ASSESSMENT: JANUARY 2021 SESSION

Instructions: This paper consists of **FOUR (4)** questions. Answer **ALL** questions. All questions carry equal marks.

Question 1

(a) Present the following Boolean expressions according to the stated simplest form, using the specified method:

(i) $F_1(W,X,Y,Z) = \sum m(3,7,12,14,15) + d(8,9,10)$
Simplest Form: POS.
Method: Karnaugh Map and/or Boolean Algebra.

(4 marks)

(ii) $F_2(R,S,T,U) = \sum m(0,5,10,15) + d(3,6,9,12)$
Simplest Form: Any type of gate implementation deemed appropriate.
Method: Karnaugh Map and/or Boolean Algebra.

(4 marks)

(iii) $F_3(K,L,M,N) = \prod M(0,2,4,6,8,10,13,15) \cdot \prod d(3,9)$
Simplest Form: Any type of gate implementation deemed appropriate.
Method: Karnaugh Map and/or Boolean Algebra.

(4 marks)

(b) Produce the simplest Boolean expression for F in Figure 1(b) and present the minimum expression using Boolean simplification method only. Suggest only one type of gate to represent the simplified expression and state the IC part number for the implementation. Show all workings clearly.

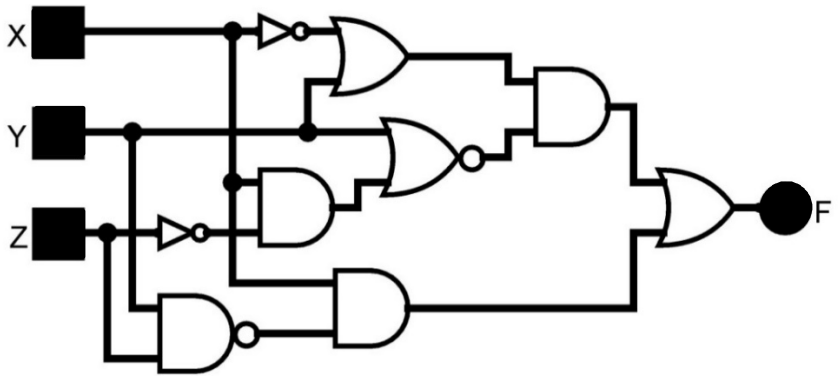

Figure 1(b)

(8 marks)

(c) Solve the numbering system transformation of [$3016.3016_{16} - 2021.2021_{16}$] to its decimal equivalent with 5 decimal points accuracy. Show all workings clearly.

(5 marks)

Question 2

(a) A D flip-flop is connected as shown in Figure 2a(i). Sketch the output, Q with the given input, X waveform as shown in Figure 2a(ii). The output Q is initially HIGH. Assume that there is no propagation delay issue and the flip-flop has been enabled. Copy Figure 2a(ii) into your answer sheet.

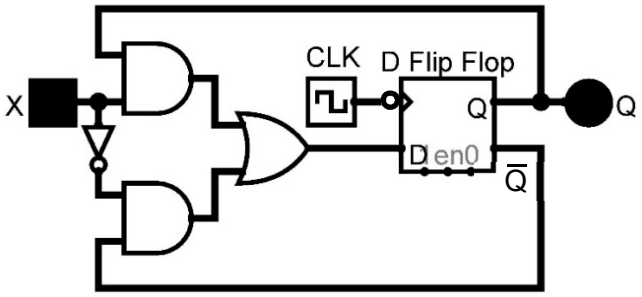

Figure 2a(i)

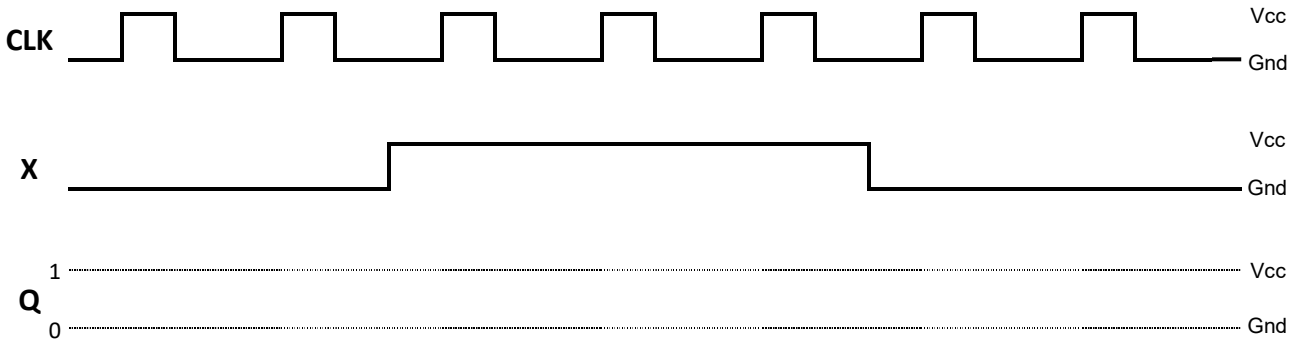

Figure 2a(ii)

(5 marks)

(b) A NOR SR latch is driven from a 2-bit binary counter with outputs designated B_1B_0 (B_1 is the MSB). Output B_1 is ANDed with $B1 \oplus B0$ and drives the R input of the SR latch. B_0 is also ANDed with $B1 \oplus B0$ and drives the S input.

(i) Draw the logic circuit showing the inputs, B_1 & B_0 and output, Q of SR latch.

(2.5 marks)

(ii) Construct a truth table to record the output, Q of the SR latch as the counter steps through its 4 states beginning with $B_1B_0 = 00$. Assume the output is initially RESET.

(2.5 marks)

(c) A synchronous 3-bit up/down counter using positive edge-triggered JK flip-flop for MSB, D flip-flop for second bit and SR flip-flop for LSB. Assume J_2 & K_2 are the MSB input, D_1 is the next flip-flop inputs and S_0 & R_0 are the LSB inputs. Assume all unused states as don't care.

Input S will be used as the up/down control. The counter will count from 0 ⇨ 7 ⇨ 5 ⇨ 4 ⇨ 3 ⇨ 1 ⇨ 0 when input, S = 0 and 0 ⇨ 1 ⇨ 3 ⇨ 4 ⇨ 5 ⇨ 7 ⇨ 0 when input, S = 1 as shown below in Figure 2(c). Flip-flop J_2K_2 has output Q_2, flip-flop D_1 has output Q_1 and flip-flop S_0R_0 has output Q_0.

Show all workings according to the procedures listed in part (c)(i), (c)(ii) and (c)(iii).

(i) Prepare the transition table/next state table for the up/down counter.

(4 marks)

(ii) Produce the simplest Boolean expressions for J_2, K_2, D_1, S_0 and R_0 inputs using Karnaugh map and/or Boolean algebra.

(5 marks)

(iii) Construct the logic circuit diagram for the simplified Boolean expressions obtained in part (c)(ii) using JK, D, SR flip-flops and other logic gates with proper labelling.

(6 marks)

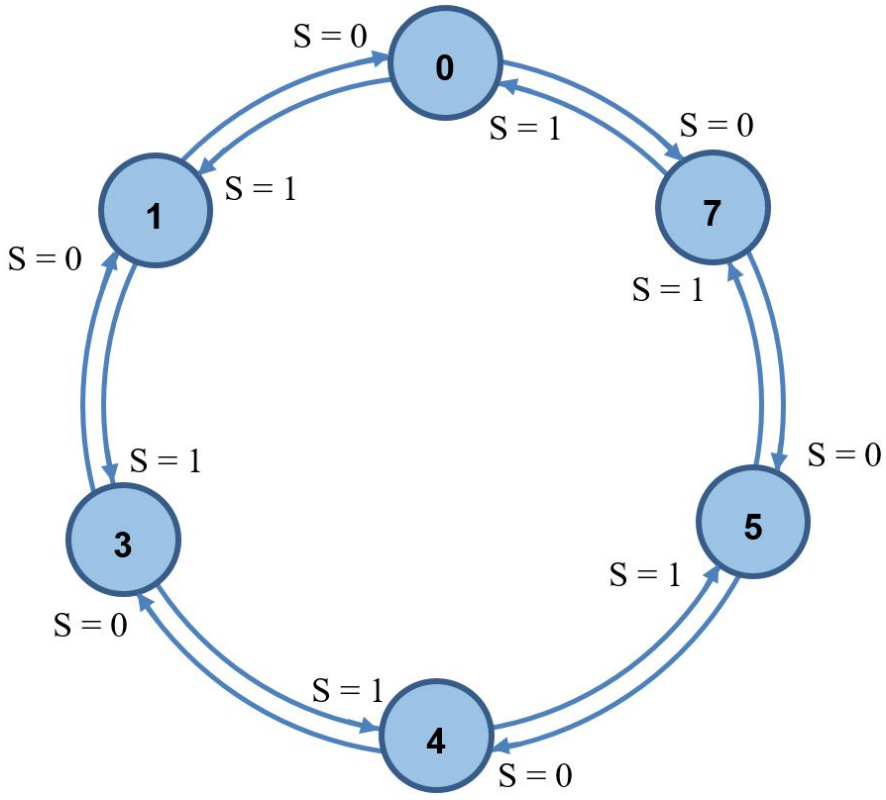

Figure 2(c)

Question 3

(a) Solve the numbering system transformation of $[10215.01_8 \times 16_8]$ to its hexadecimal equivalent with 2 hexadecimal points accuracy. Show all workings clearly.

(5 marks)

(b) Table 3(b) shows a portion of a quadruple 2-input NOR gates (SN54LS02) datasheet. Compute the following parameters from this datasheet, show all workings clearly:

(i) Power dissipation, $P_{D(max)}$ on an SN54LS02 IC when the output condition is as shown in Figure 3(b). Assume that the V_{CC} used is maximum.

(6 marks)

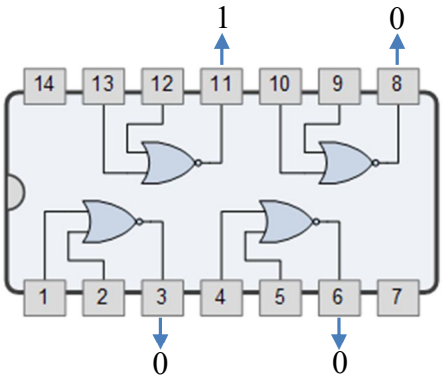

Figure 3(b)

(ii) Fan-out, the number of gates from the same IC family that can be safely driven by an output under worst-case consideration.

(3 marks)

(iii) Noise Margin voltages, V_{NL} and V_{NH}.

(3 marks)

Table 3(b)

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

continue next page…

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH				3.2	mA	V_{CC} = MAX	
	Total, Output LOW				5.4			

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
t_{PLH}	Turn-Off Delay, Input to Output		10	15	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	Turn-On Delay, Input to Output		10	15	ns	

(c) Table 3(c) shows the current ratings of TTL series logic gates. A 74S08 AND gate output is driving a few other TTL inputs as shown in Figure 3(c).

(i) Discover through calculation whether there is a loading problem.

(5 marks)

Table 3(c)

TTL Series	Output Drive		Input Loading	
	I_{OH}	I_{OL}	I_{IH}	I_{IL}
74	400μA	16mA	40μA	1.6mA
74S	1.0mA	20mA	50μA	2.0mA
74LS	400μA	8mA	20μA	400μA
74AS	2.0mA	20mA	200μA	2.0mA
74ALS	400μA	8mA	20μA	100μA
74F	1.0mA	20mA	20μA	600μA

(ii) The 74S08 AND gate output needs to drive some 74S inputs in addition to the loads shown in Figure 3(c). Compute the additional number of 74S inputs that can be driven by the output of the 74S08 AND gate.

(3 marks)

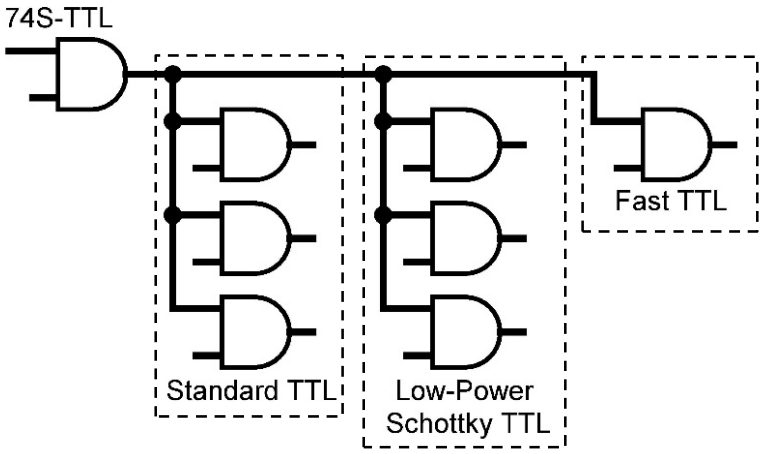

Figure 3(c)

Question 4

(a) Compute the 2's complement number of -6.625_{10} in signed binary numbering system. Assuming the binary system is 4-bit system with 4 binary points. Show all workings clearly.

(5 marks)

(b) A 14-bit DAC produces an output current in proportion to its digital input. For a digital input of 00000001010000_2, an output current of 20mA is produced.

(i) Compute the output current if the digital input is 10010001111010_2.

(4 marks)

(ii) Compute the maximum output current produced by this DAC.

(3 marks)

(iii) Compute the digital input if a 2101mA output current is required.

(3 marks)

Figure 4(b)

(c) Analog to Digital Converter (ADC) is an important element in signal processing for digital conversion of sensor signal. In the case of digitizing a vibration signal measured by an accelerometer (acceleration transducer) with the characteristics shown in Table 4(c).

Table 4(c)

Sensitivity	(±5.0%) 100 mV/g
Measurement Range	±50 g peak
Frequency Range	(±5%) 10 to 15000 Hz
Sensing Element	Quartz
Weight	100 gram

Assume the formula given is $resolution = \frac{Vrange}{2^n - 1}$. Apply an appropriate ADC for this sensor application by computing the:

(i) Number of bits.

(7 marks)

(ii) Resolution.

(3 marks)

~THE END~