INTI International College Penang

FINAL
ALTERNATIVE ASSESSMENT

(COVER PAGE)

Session	:	**January 2021**
Programme	:	Diploma in Electrical & Electronic Engineering (DEEI)
Course	:	**EEE1109: Analogue Electronics**
Date of Examination	:	10 March 2021 (Wednesday)
Time	:	8.00am – 11.00am Reading Time : Nil
Duration	:	3 Hours

Special Instructions :

This paper consists of **FOUR (4)** questions. Answer **ALL FOUR (4)** questions. All questions carry equal marks.

Material permitted :
Non-Programmable Scientific Calculator

Materials provided :
Nil

Examiner(s)	:	**Dr. Su Hsiao Wei**
Chief Moderator	:	Chan Tse Wei

*This paper consists of **9** printed pages, including the cover page*

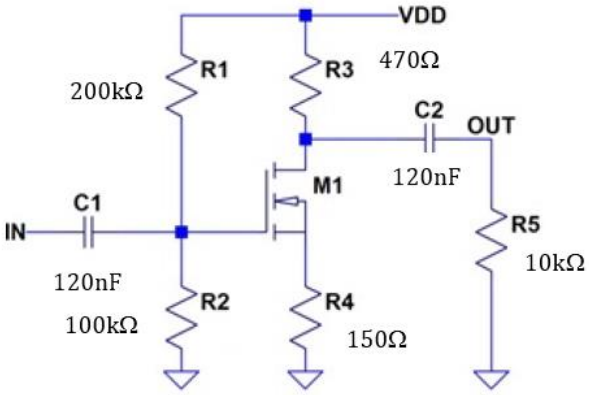
INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE1109: ANALOGUE ELECTRONICS
FINAL ALTERNATIVE ASSESSMENT: JANUARY 2021 SESSION

Instructions: This paper consists of **FOUR (4)** questions. Answer **ALL FOUR (4)** questions. All questions carry equal marks.

Question 1

(a) Figure 1(a) shows a single stage FET amplifier and its voltage gain frequency response.



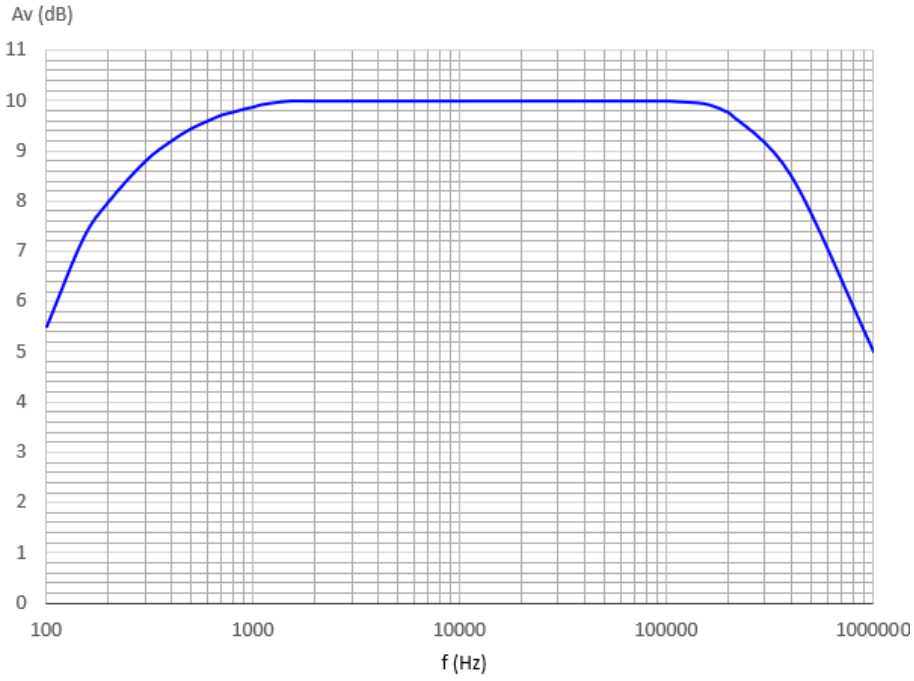


Figure 1 (a)

(i) Identify and explain the components that contribute to the gain reduction at the low frequency band.

(3 marks)

(ii) Identify and explain the components that contribute to the gain reduction at the high frequency band.

(3 marks)

(iii) Find the upper and lower cutoff frequencies from the amplifier voltage gain frequency response. Then estimate the bandwidth of the amplifier.

(4 marks)

(b) Figure 1(b) shows a single-stage FET amplifier. The FET has the following parameter values:
$I_{DQ} = 8mA@V_{GSQ} = 3.6V$

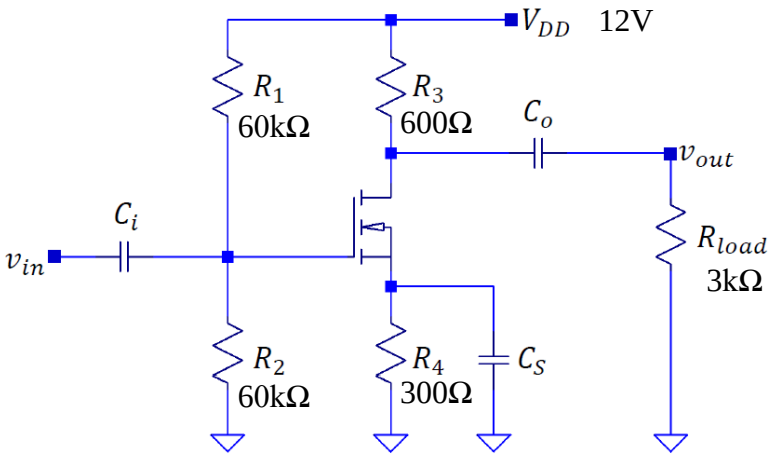


Figure 1(b)

(i) Explain the importance of DC biasing for this amplifier.

(2 marks)

(ii) Explain the influence on the DC biasing of the amplifier if capacitors C_i and C_o are not present in the circuit.

(2 marks)

(iii) Calculate the quiescent voltages $V_{GQ}, V_{DQ}, V_{SQ}, and\ V_{DSQ}$.

(4 marks)

(c) Figure 1(c) shows the AC equivalent circuit model of an FET voltage amplifier.

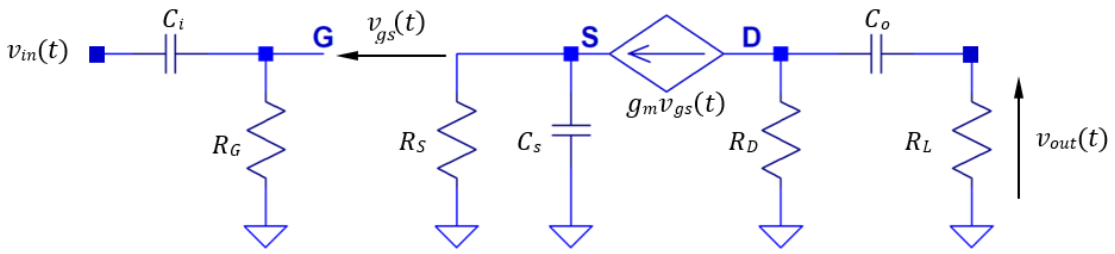


Figure 1(c)

(i) Redraw the AC equivalent circuit model to evaluate the cutoff frequency contributed by capacitor C_s.

(2 marks)

(ii) By utilizing the AC equivalent circuit model obtained in part 1(c)(i), show that the voltage transfer function of $V_S(s)/V_G(s)$ can be expressed in the form of,

$$\frac{V_S(s)}{V_G(s)} = \frac{a_0}{s + \omega_o}$$

and state a_0 and ω_o in terms of the relevant passive components and transistor parameter, g_m. Obtain the cutoff frequency expression of the amplifier which is contributed by capacitor C_s.

(5 marks)

Question 2

(a)

(i) Draw the schematic diagram of an inverting amplifier which is utilizing a single op-amp, operating from a single positive supply.

(2 marks)

(ii) By using relevant circuit principles or rules, derive the voltage transfer function expression of the amplifier in part 2(a)(i).

(3 marks)

(iii) Sketch the input and output voltage waveforms of the amplifier in part 2(a)(i) as a function of time with a closed-loop voltage gain of -3 and $V_{in} = 2\sin(1000\pi t)$. Show all your calculations. Label your sketch clearly.

(4 marks)

(b) Figure 2(b) shows an inverting amplifier implemented with an op-amp having the following specifications:

$Vs(max)$ = +20 V
$slew\ rate$ = 9 V/μs
$|V_{o(sat)}| = |Vsupply| - 1$ V

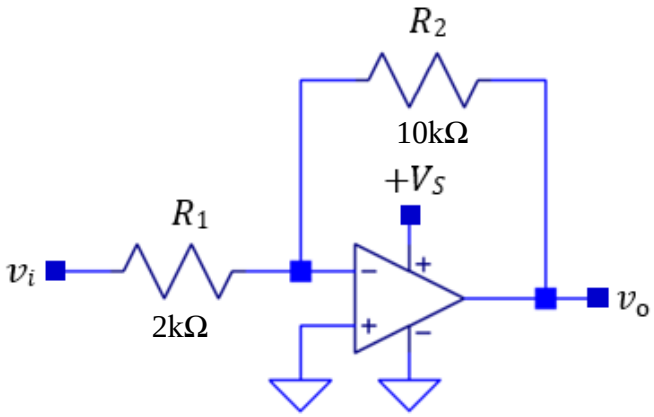


Figure 2(b)

If $v_i = 2\sin(300000\pi t)$, do the followings:

(i) Calculate the maximum output voltage v_o of the amplifier. Justify the suitability of the op-amp implementation from the saturation voltage point of view.

(4 marks)

(ii) Calculate the maximum rate of change of the amplifier output. Justify the suitability of the op-amp implementation from the slew-rate point of view.

(4 marks)

(c) Figure 2(c) shows a Schmitt triggered comparator with a reference voltage circuitry. Assumed that the op-amps used in the circuit have rail-to-rail output.

(i) Calculate the reference voltage, upper and lower threshold points of the circuit.

(6 marks)

(ii) Sketch the voltage transfer curve of the circuit with clear labeling of all the relevant voltage levels.

(2 marks)

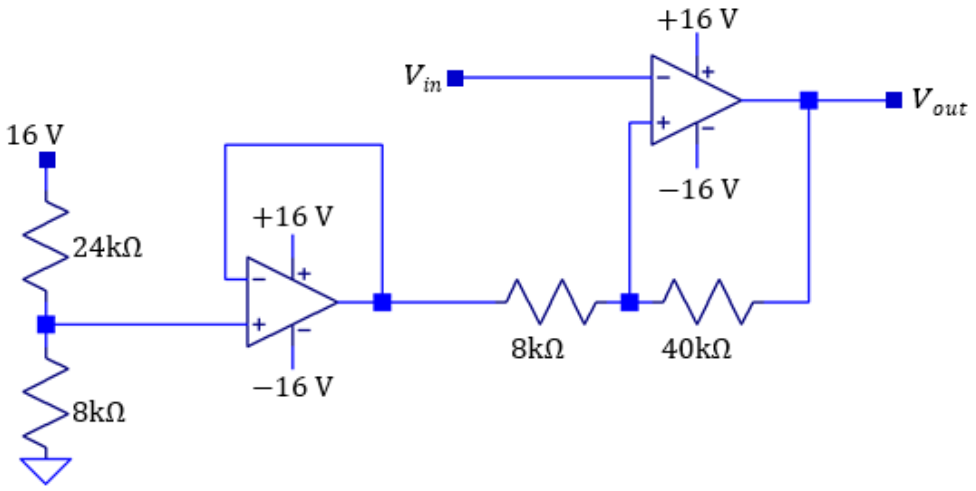


Figure 2(c)

Question 3

(a) Copy Table 3(a) into your answer script and complete the blank cells in the table by stating two pros and cons of the listed filters.

Table 3(a)

		Passive Filter	**Active Filter**
Pros	1		
	2		
Cons	1		
	2		

(4 marks)

(b) A filter is implemented by cascading several analogue circuit building blocks as shown in Figure 3(b).

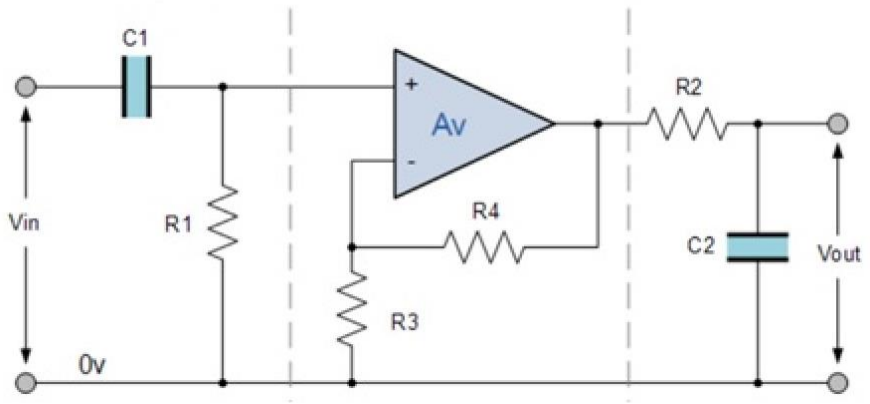


Figure 3(b)

(i) Identify the building blocks.

(1 mark)

(ii) Derive the filter voltage transfer function.

(7 marks)

(iii) Identify the type and order of the filter based on the voltage transfer function expression obtained in part 2(b)(ii).

(2 marks)

(c) A filter is realized by cascading two different filter building blocks and the overall filter transfer function is expressed as

$$T(s) = \left(\frac{9}{3s+40}\right)\left(\frac{2s}{3s+20}\right)$$

(i) Identify the type and order of the filter. Quantitatively justify your answers.

(3 marks)

(ii) Calculate the filter cutoff frequencies (lower and upper) in rad/s.

(6 marks)

(iii) Identify the filter type (passive or active). Quantitatively justify your answer.

(2 marks)

Question 4

(a) In general, explain the followings pertaining to an oscillator circuit.

(i) Operation.

(2 marks)

(ii) Output design requirements.

(2 marks)

(b) Figure 4(b) shows a design example of a relaxation oscillator constructed from a 555 timer IC.

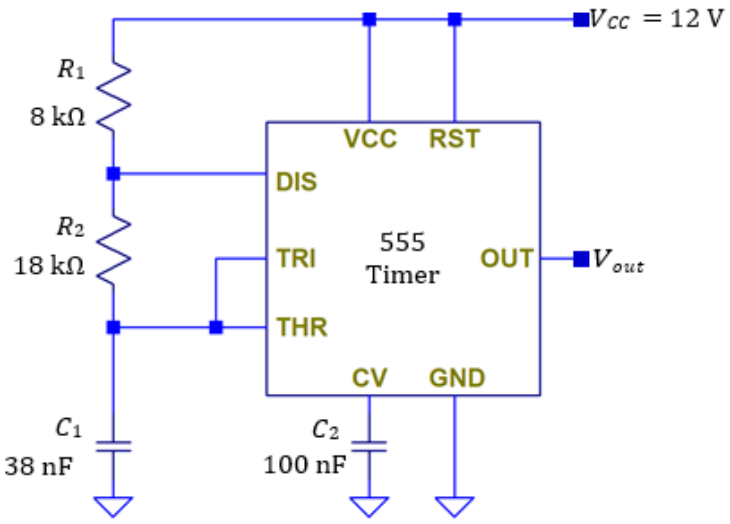


Figure 4(b)

(i) Calculate the oscillation frequency of the output signal V_{out}.

(2 marks)

(ii) Calculate the duty cycle of the output signal in %.

(2 marks)

(iii) Suggest and explain a way to reduce the output oscillation frequency with the duty cycle not affected.

(3 marks)

(iv) With additional external circuitry, suggest and explain a method to obtain a rectangular wave with duty cycle less than 50% with the frequency of oscillation not affected.

(3 marks)

(c) Figure 4(c) shows a Wien Bridge oscillator circuit.

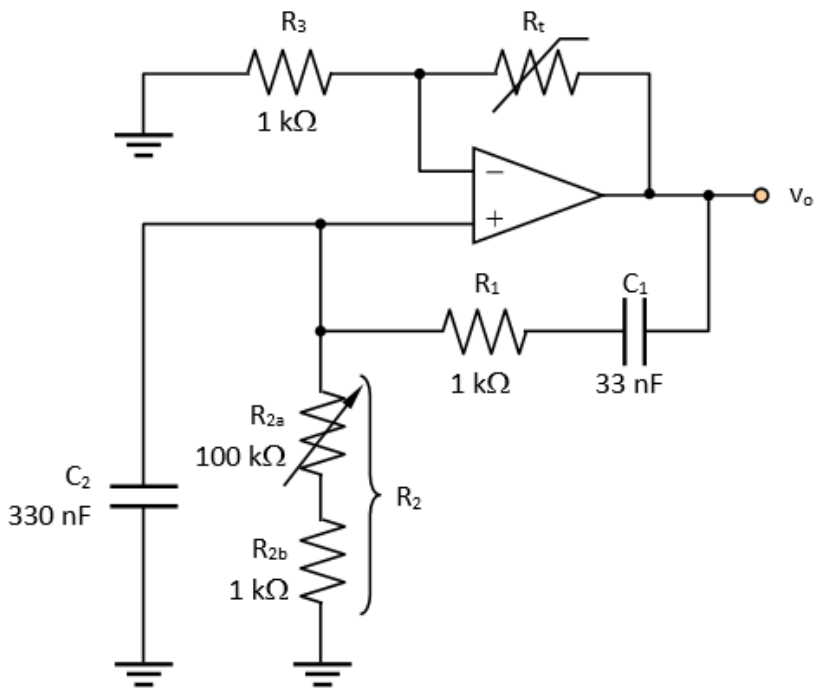


Figure 4(c)

(i) Explain the purpose of the variable resistor R_{2a}.

(2 marks)

(ii) Explain the purpose of the thermistor R_t.

(2 marks)

(iii) The positive feedback circuit transfer function is expressed as

$$\frac{V_f}{V_O} = \frac{\omega C_1 R_2}{\omega(C_1R_1 + C_2R_2 + C_1R_2) - j(1 - \omega^2 C_1C_2R_1R_2)}$$

Find the expression for the resonant angular frequency.
Prove that for the circuit to sustain oscillation, the oscillator's amplifier gain is given by $R_t = 2R_3$ if $R_1 = R_2$ and $C_1 = C_2$.

(5 marks)

(iv) Calculate the range of oscillation frequency when R_{2a} is adjusted between its extreme ends.

(2 marks)

~THE END~