INTI International College Penang

FINAL
ALTERNATIVE ASSESSMENT

(COVER PAGE)

Session	:	**January 2021**		
Programme	:	Diploma in Electrical & Electronic Engineering (DEEI)		
Course	:	**EEE1105: Circuit Theory & Electronic Devices**		
Date of Examination	:	11 March 2021 (Thursday)		
Time	:	8.00am – 11.00am	Reading Time :	Nil
Duration	:	3 Hours		

Special Instructions :
This paper consists of **FOUR (4)** questions. Answer **ALL** the questions. All questions carry equal marks.

Answer script Blackboard submission requirement:

- Submit your softcopy answer script ONE time only to Blackboard.
- Write on top of each page of the answer script student Inti ID or name, subject code and page number. *Example: P20209539 / EEE1105 / Page 2 of 5.*
- Arrange your answer in proper order, scan the answer scripts and submit it to Blackboard within the given examination allocated time. Late submission is NOT allowed.
- Use a proper scanner or CamScanner on your mobile for scanning. Combine all pages in ONE PDF file for submission to Blackboard. Filename: **EEE1105 Final Exam (Name).PDF**
- Make sure pages of answer script are scanned with the good contrast and readable quality.
- Marking will be based on the scanned document as final.

Material permitted :
Non-Programmable Scientific Calculator

Materials provided :
Nil

Examiner(s)	:	**Chai Yoon Yik**
Chief Moderator	:	Dr Su Hsiao Wei

*This paper consists of **6** printed pages, including the cover page*

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE1105 CIRCUIT THEORY & ELECTRONIC DEVICES
FINAL ALTERNATIVE ASSESSMENT: JANUARY 2021 SESSION

Instructions: This paper consists of **FOUR (4)** questions. Answer all the questions. All questions carry equal marks.

Question 1 [25]

(a) A multiple sources network is shown in Figure Q1(a). Using nodal analysis, calculate the nodal voltages, V_1, V_2 and V_3. [9]

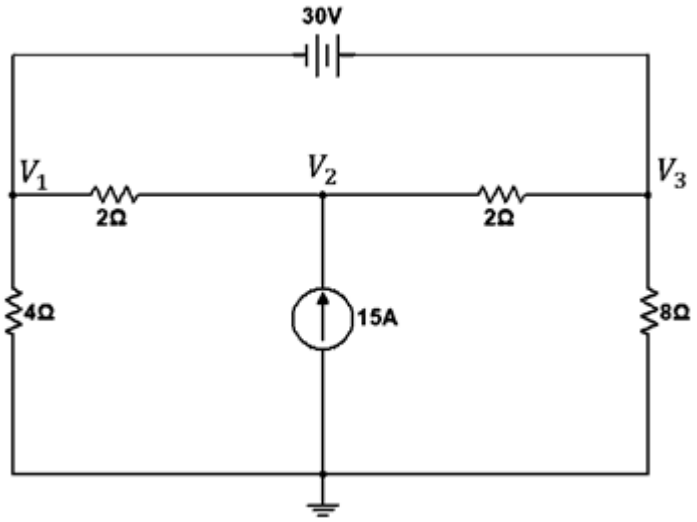


Figure Q1(a)

(b) Refer to the circuit of Figure Q1(b), using source transformation and Kirchhoff's law to calculate the current and power dissipated in the 8Ω resistor. [8]

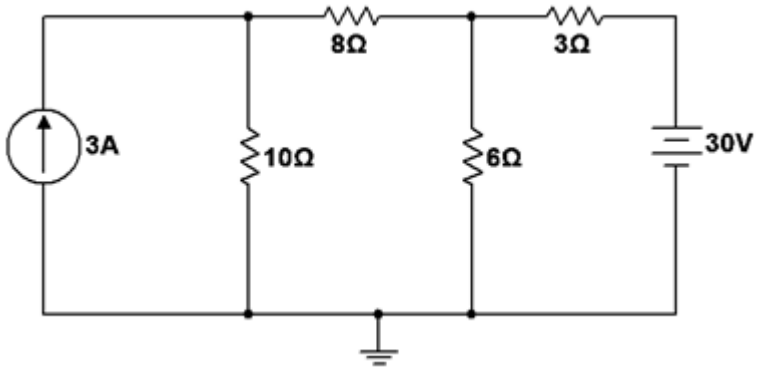


Figure Q1(b)

(c) Using superposition principle, find the current I through E_2 for the network in Figure Q1(c). [8]

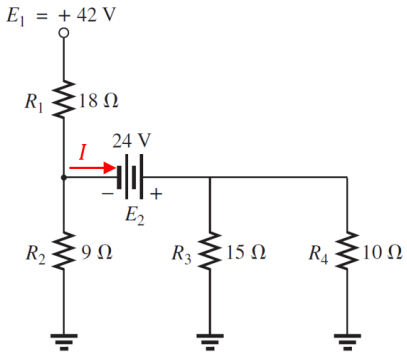


Figure Q1(c)

Question 2 [25]

(a) Figure Q2(a) shows a electrical circuit connection with sinusoidal voltage source of 50Hz.

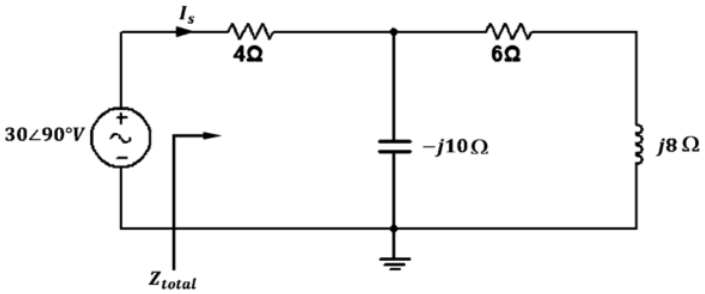


Figure Q2 (a)

Calculate:

(i) The total complex impedance $\boldsymbol{Z_{total}}$ of the circuit. [2]

(ii) The source current $\boldsymbol{I_s}$ from the source. [2]

(iii) The apparent power,**S** of the circuit. [2]

(iv) The active power,**P** of the circuit. [2]

(v) The circuit power factor. [2]

(b) For the series RLC circuit in Figure Q2(b), find:

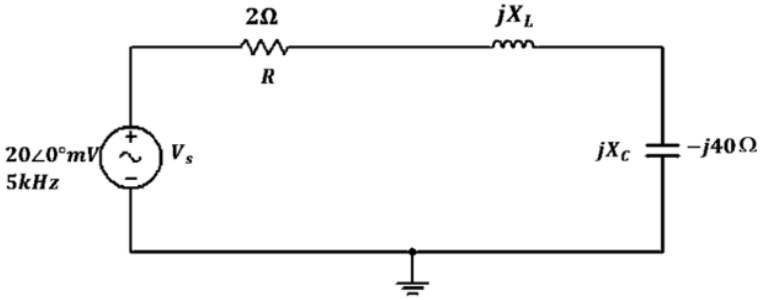


Figure Q2(b)

(i) The value of X_L for resonance. [1]

(ii) The magnitude of the circuit current, I at resonance. [2]

(iii) The voltage V_R, V_L and V_C at resonance. [3]
(iv) The quality factor of the circuit. [1]
(v) The value of L and C at resonant frequency. [2]
(vi) The bandwidth of the frequency response. [2]
(vii) The low and high cutoff frequencies. [2]
(viii) The power dissipation at -3dB frequency. [2]

Question 3 [25]

(a) Figure Q3(a) shows an RC and the switch opened at $t = 0s$.

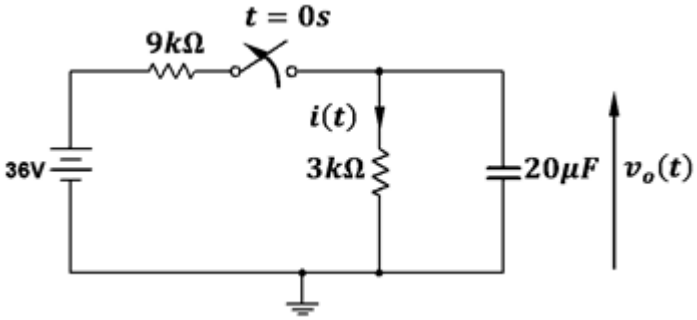
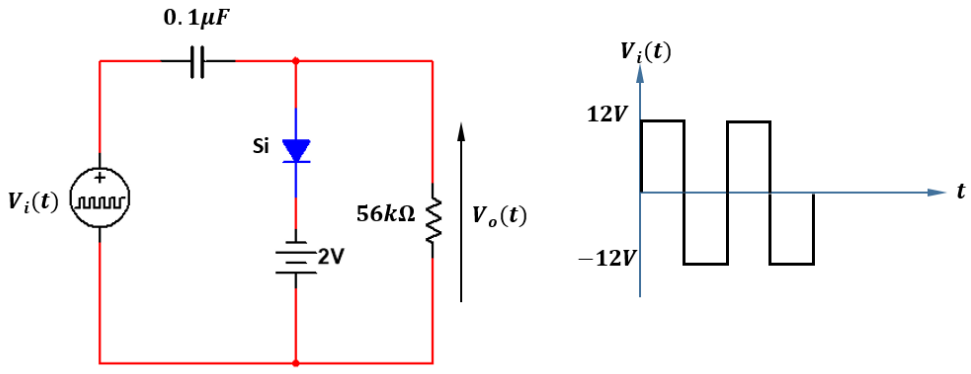


Figure Q3(a)

(i) Calculate the time constant for $t > 0\ s$. [1]
(ii) Calculate the v_o and i at $t = 0$s. [4]
(iii) Write the $v_o(t)$ equation for $t > 0$. [2]
(iv) Write the $i(t)$ equation for $t > 0$. [2]
(v) Calculate the time taken for the capacitor voltage to decay to one-third of its initial value. [2]
(vi) Sketch the $v_o(t)$ and $i(t)$. [2]

(b) Describe the meaning of barrier potential of a diode and how it is created. [4]

(c) Refer to the Figure 3(c), sketch the $V_o(t)$ waveform and label all the values of the waveform correctly. Show your calculation clearly.



[8]

Figure Q3(c)

Question 4 [25]

(a) A bipolar junction transistor is connected in voltage-divider-bias configuration as shown in the Figure Q4(a). Calculate:

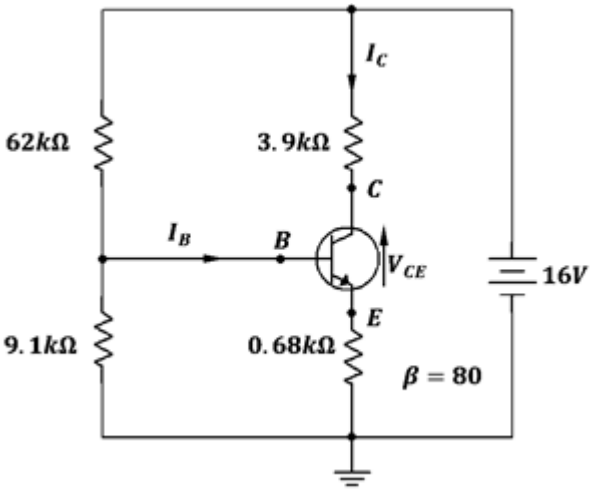


Figure Q4(a)

Using exact approach analysis, calculate:

(i) I_{BQ} [4]

(ii) I_{CQ} [1]

(iii) V_{CEQ} [2]

(iv) V_C [2]

(v) V_E [2]

(vi) V_B [2]

(vii) $transistor\ power\ dissipation$ [2]

(b) Figure Q4(b) shows an n-enhancement mode P-MOSFET circuit.

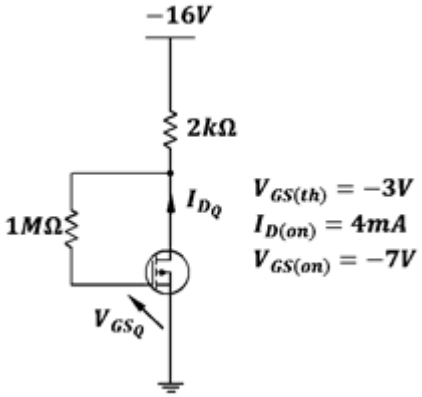


Figure Q4(b)

(i) Draw the transfer characteristics and bias line of the circuit. [4]

(i) Calculate the V_{GS_Q} and I_{D_Q}. [2]

(iii) Calculate the V_D. [3]

(iv) State the region of the drain characteristic the MOSFET operates. [1]

~THE END~

EEE1105 (F)/ January 2021 Session/ formatted