INTI International College Penang

FINAL
Examination Paper

(COVER PAGE)

Session	:	**January 2020**
Programme	:	Diploma in Electrical & Electronic Engineering (DEEI)
Course	:	**EEE2101: Introduction to Digital Electronics**
Date of Examination	:	5 April 2020 (Sunday)
Time	:	1.00pm – 4.00pm Reading Time : Nil
Duration	:	3 Hours
Special Instructions	:	

This paper consists of **FOUR (4)** questions. Answer all the **FOUR (4)** questions. All questions carry equal marks.

Materials permitted :

Nil

Materials provided :

Worksheet 2(a)

Examiner(s)	:	**Mr Steven Khoo Boo Tap**
Moderator	:	Ms Shalyn Lim

*This paper consists of **8** printed pages, including the cover page.*

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE2101: INTRODUCTION TO DIGITAL ELECTRONICS
FINAL EXAMINATION: JAN2020 SESSION

Instructions: This paper consists of **FOUR (4)** questions. Answer **ALL** questions in the answer booklet provided. All questions carry equal marks.

Question 1

(a) Present the following Boolean expression using Karnaugh Map and/or Boolean expression:

(i) $F_1(W,X,Y,Z) = \sum m(3,7,12,14,15) + d(8,9,10)$ to the simplest POS form.
(4 marks)

(ii) $F_2(R,S,T,U) = \sum m(0,5,10,15) + d(3,6,9,12)$ to the simplest form.
(4 marks)

(iii) $F_3(K,L,M,N) = \prod M(0,2,4,6,8,10,13,15) \cdot \prod d(3,9)$ to the simplest SOP form.
(4 marks)

(b) Produce the Boolean expression of F in Figure 1(b) and present the expression to the minimum using Boolean simplification only. Use only ONE IC (Integrated Circuit) of your choice to represent the simplified expression. Show working clearly.

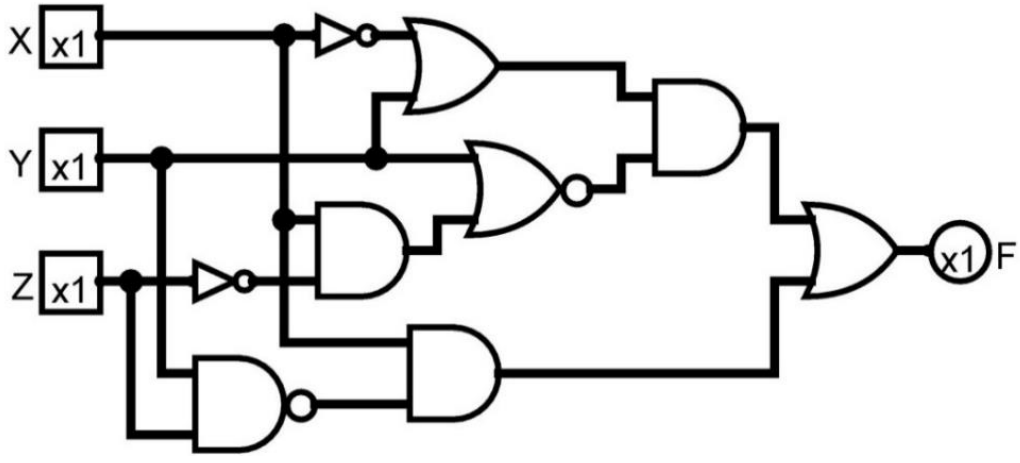

Figure 1(b)

(8 marks)

(c) Solve the numbering system transformation of [3020.24_{16} – 1001.1_8 + 1110.101_2] to decimal equivalent with 4 decimal points accuracy. Show all workings clearly.
(5 marks)

Question 2

(a) A D flip-flop is connected as shown below in Figure 2a(i). Sketch the output, Q with the given input, X waveform as shown below in Figure 2a(ii). The Q is initially at HIGH. Assume that there is no propagation delay issue and the flip-flop has been enabled.
Note: Use **Worksheet 2(a)** given to answer this question.

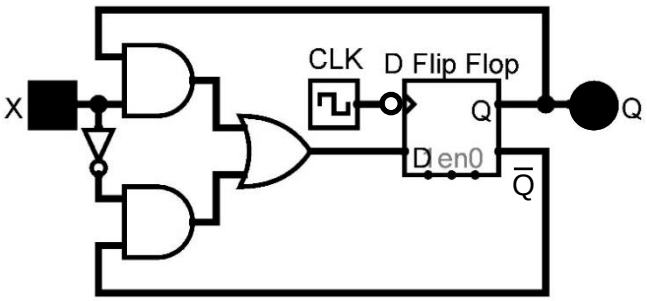

Figure 2a(i)

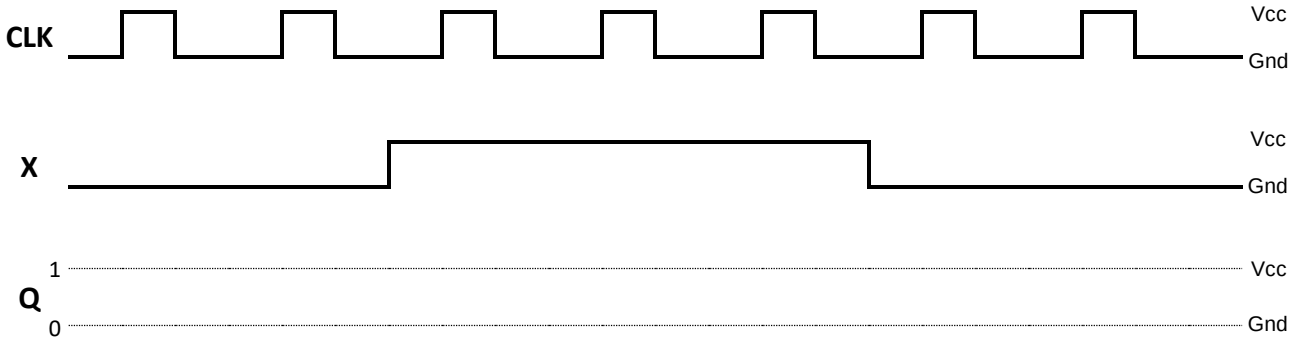

Figure 2a(ii)

(5 marks)

(b) For the given truth tables in Table 2b(i) and excitation tables in Table 2b(ii), illustrate how a D flip-flop function can be obtained using SR flip-flop. The design can be added with additional gates in order to fulfil the conversion. Show all workings clearly for SR-to-D converter.

(5 marks)

Table 2b(i) Flip-flop Truth Tables

Inputs		Outputs	
S	R	Q_n	Q_{n+1}
0	0	No Change	
0	1	Reset	
1	0	Set	
1	1	Invalid	

Inputs		Outputs	
J	K	Q_n	Q_{n+1}
0	0	No Change	
0	1	Reset	
1	0	Set	
1	1	Toggle	

Input	Outputs	
D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Input	Outputs	
T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Q_n: Present State
Q_{n+1}: Next State

Table 2b(ii) Flip-flop Excitation Tables

Outputs		Inputs	
Q_n	Q_{n+1}	S	R
0	0	0	×
0	1	1	0
1	0	0	1
1	1	×	0

Outputs		Inputs	
Q_n	Q_{n+1}	J	K
0	0	0	×
0	1	1	×
1	0	×	1
1	1	×	0

Outputs		Input
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Outputs		Input
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Q_n: Present State
Q_{n+1}: Next State

(c) Figure 2(c) shows a 4-bit synchronous counter, which is designed so that it performs a special counting sequence. Predict its operation by determining its counting sequence.

Assume that all flip-flops are initially in the State 0 (0000) for $Q_3Q_2Q_1Q_0$. Flip-flop FF3 is the MSB and FF0 is LSB. Use J_3K_3, D_2, S_1R_1 and T_0 inputs labelling for Q_3, Q_2, Q_1 and Q_0 outputs. All flip-flops used are positive edge triggered type. Show all workings clearly.

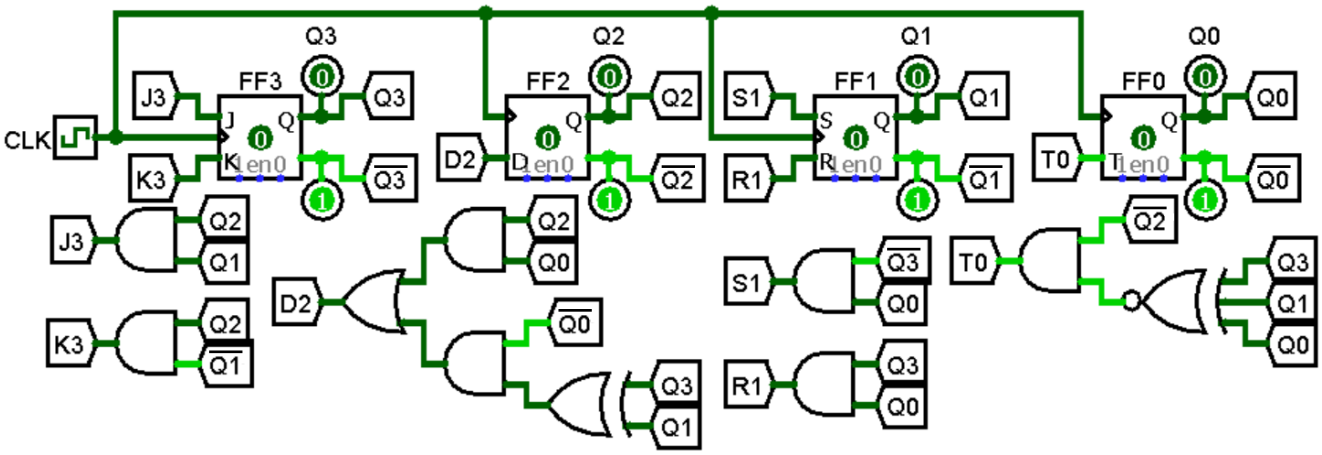

Figure 2(c)

(i) Produce the Boolean expressions from the logic circuit.

(3 marks)

(ii) Produce all Karnaugh maps according to the expressions obtained.

(4 marks)

(iii) Produce the transition table/next-state table.

(4 marks)

(iv) Sketch the state diagram and interpret on the outcome of the states obtained.

(4 marks)

Question 3

(a) Solve the numbering system transformation of [$12017.01_8 \times 15.5_{10}$] to hexadecimal equivalent with 2 hexadecimal points accuracy. Show all workings clearly.

(5 marks)

(b) Table 3(b) shows a portion of quadruple 2-input XOR gates (DM7486) datasheet. Compute the following parameters from this datasheet, show all working clearly:

(i) Power dissipation, $P_{D(max)}$ on a DM7486 IC when the output condition is as shown in Figure 3(b). Assume that the V_{CC} used is 5V.

(6 marks)

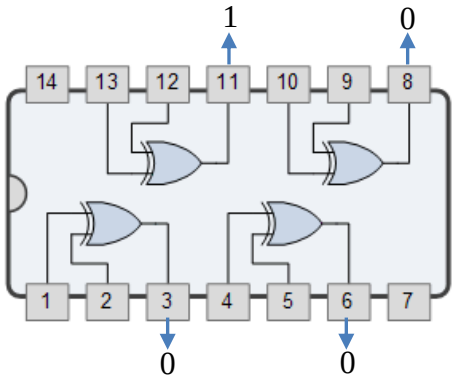

Figure 3(b) XOR gate pinout.

(ii) Fan-out, a gate can safely drive.

(3 marks)

(iii) Noise Margin voltages, V_{NL} and V_{NH}.

(3 marks)

Table 3(b) XOR gate.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = –18 mA			–1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.2	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			40	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			–0.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	–20		–100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max (Note 4)		6.1	10	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max (Note 5)		9	15	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CCH} is measured with all outputs OPEN, one input at each gate at 4.5V, and the other inputs grounded.

Note 5: I_{CCL} is measured with all outputs OPEN and all inputs grounded.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	Conditions	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Other Input Low		18		23	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			17		21	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Other Input High		10		15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			12		15	ns

(c) Table 3(c) shows the current ratings of TTL series logic gates. A 74S08 AND gate output is driving a few other TTL outputs as shown in Figure 3(c).

(i) Discover through calculation whether there is a loading problem.

(5 marks)

TTL Series	Output Drive		Input Loading	
	I_{OH}	I_{OL}	I_{IH}	I_{IL}
74	400µA	16mA	40µA	1.6mA
74S	1.0mA	20mA	50µA	2.0mA
74LS	400µA	8mA	20µA	400µA
74AS	2.0mA	20mA	200µA	2.0mA
74ALS	400µA	8mA	20µA	100µA
74F	1.0mA	20mA	20µA	600µA

Table 3(c)

(ii) The 74S08 AND gate output needs to be used to drive some 74S inputs in addition to the load inputs. Compute how many additional 74S inputs could the output drive without being overloaded?

(3 marks)

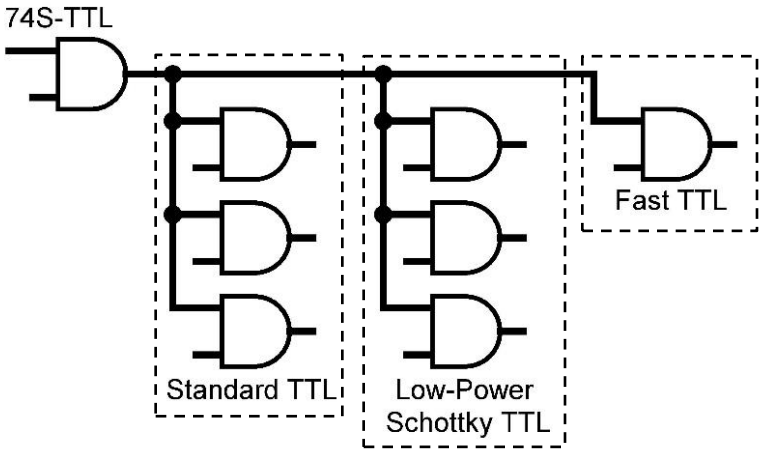

Figure 3(c)

Question 4

(a) Compute the 2's complement number of -6.625_{10} in signed binary numbering system. Assuming the binary system is 4-bit system with 4 binary points. Show all workings clearly.

(5 marks)

(b) Analog to Digital Converter (ADC) is an important element in signal processing for digital conversion of sensor signal. In the case of digitizing a vibration signal measured by an accelerometer with the following characteristics (PCB-301A10):

- Sensitivity: (±2.0%) 100 mV/g
- Measurement Range: ±100 g pk
- Frequency Range: (±5%) 0.5 to 10000 Hz
- Sensing Element: Quartz
- Weight: 176 gm

Apply an appropriate ADC for this sensor application by computing the:

(i) Number of bits

(10 marks)

(ii) Resolution

(3 marks)

(c) A 14-bit DAC produces an output current in proportion to its digital input. For a digital input of 00000001010000_2, an output current of 20mA is produced.

(i) Compute the output current be if the digital input is 10010001111010_2.

(3 marks)

(ii) Compute the maximum output current produced by this DAC.

(2 marks)

(iii) Compute the digital input if a 2109mA output current is required.

(2 marks)

Figure 4(c)

– THE END –

EEE2101(F)/Jan2020/Steven Khoo/24/03/2020

Worksheet 2(a)

(a) A D flip-flop is connected as shown below in Figure 2a(i). Sketch the output, Q with the given input, X waveform as shown below in Figure 2a(ii). The Q is initially at HIGH. Assume that there is no propagation delay issue and the flip-flop has been enabled.

Note: Use **Worksheet 2(a)** to answer this question, detach **Worksheet 2(a)** and tie with the answer booklet.

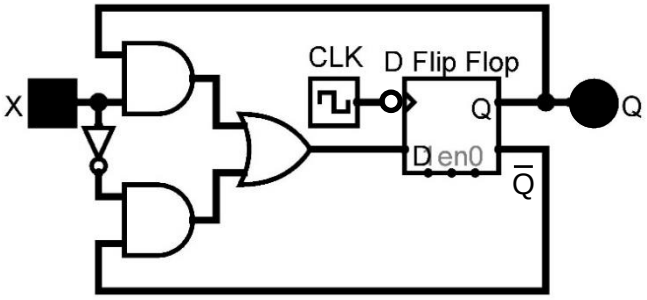

Figure 2a(i)

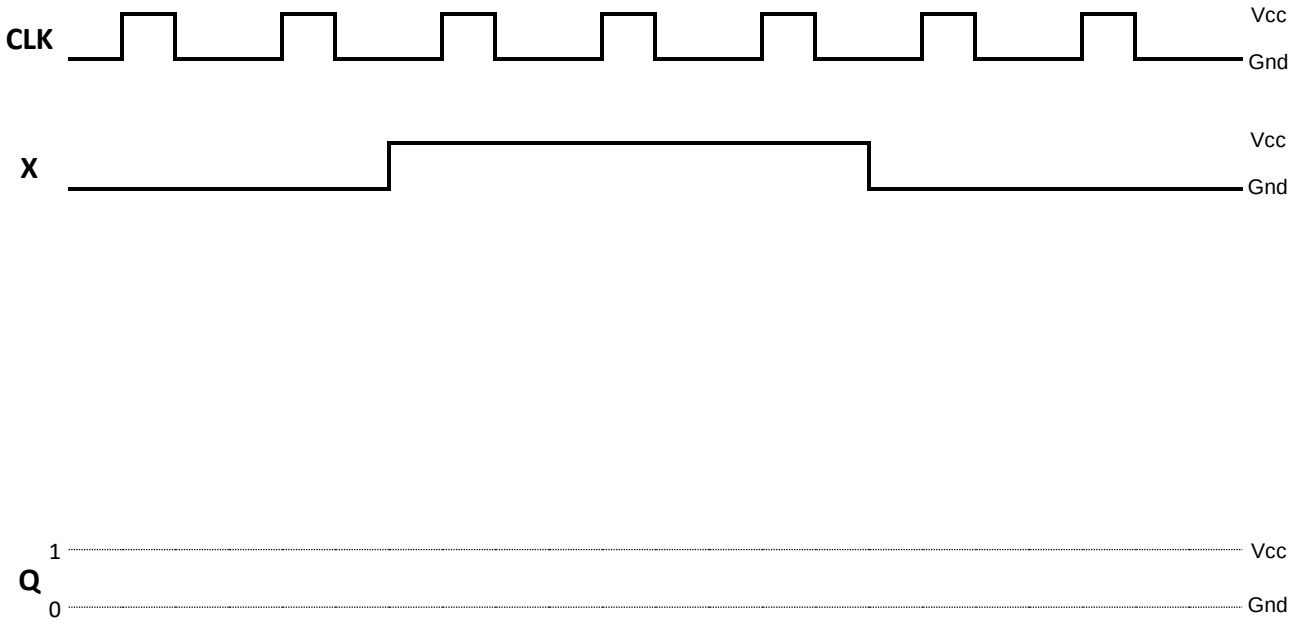

Figure 2a(ii)

(5 marks)