INTI International College Penang

FINAL
ALTERNATIVE ASSESSMENT

(COVER PAGE)

Session	:	**January 2022**
Programme	:	Diploma in Electrical & Electronic Engineering (DEEI)
Course	:	**EEE2101: Introduction to Digital Electronics**
Date of Examination	:	7 March 2022 (Monday)
Time	:	8.00am – 11.00am Reading Time : Nil
Duration	:	3 Hours

Special Instructions :

This paper consists of **FOUR (4)** questions. Answer **ALL** questions. All questions carry equal marks.

Material permitted :
Non-Programmable Scientific Calculator

Materials provided :
Nil

Examiner(s)	:	**Steven Khoo Boo Tap**
Chief Moderator	:	Dr Su Hsiao Wei

*This paper consists of **8** printed pages, including the cover page*

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE2101: INTRODUCTION TO DIGITAL ELECTRONICS
FINAL ALTERNATIVE ASSESSMENT: JANUARY 2022 SESSION

Instructions: This paper consists of **FOUR (4)** questions. Answer **ALL** questions. All questions carry equal marks.

Question 1

(a) Present the following Boolean expressions to the stated simplest form, using the specified method:

(i) $F_1(W,X,Y,Z) = \sum m(2,7,8,13) + d(1,4,11,14)$
Simplest Form: Any type of gate(s) implementation deemed appropriate.
Method: Karnaugh Map and/or Boolean Algebra.

(5 marks)

(ii) $F_2(R,S,T,U) = \prod M(0,2,5,6,8,9,10,15) \cdot \prod d(1,4)$
Simplest Form: Any type of gate(s) implementation deemed appropriate.
Method: Karnaugh Map and/or Boolean Algebra.

(5 marks)

(b) Produce the simplest Boolean expression for Z in Figure 1(b) and show the minimum expression using 2-input NAND gate representation only. State the number of 7400 IC used for the simplified expression. Show all workings clearly.

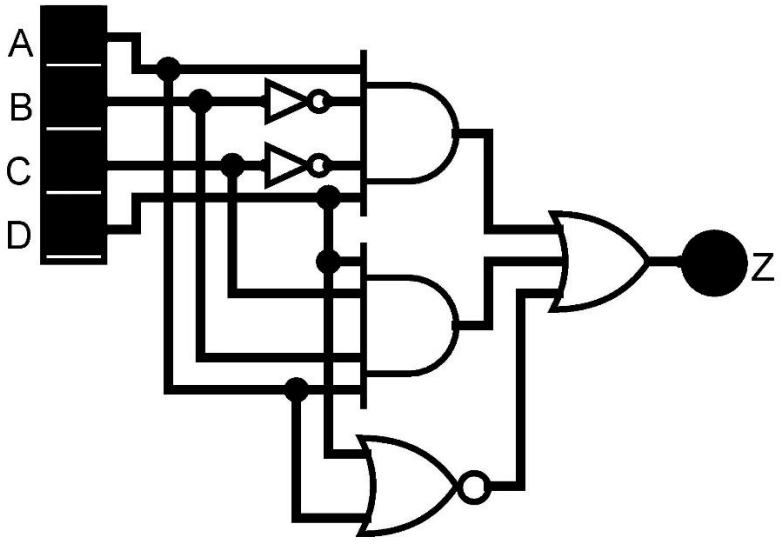

Figure 1(b)

(10 marks)

(c) Solve the numbering system transformation of [123.35_8 – 20.21_{16}] to its decimal equivalent with 8 decimal points accuracy. Show all workings clearly.

(5 marks)

Question 2

(a) A NAND SR latch is driven from a 2-bit binary counter with outputs designated C_1C_0 (C_1 is the MSB). Output C_1 is ORed with $\overline{C_1 \oplus C_0}$ and drives the R input to the latch. C_0 is also ORed with $\overline{C_1 \oplus C_0}$ and drives the S input.

(i) By applying logic gate concept, draw the logic circuit showing the inputs, C_1 & C_0 and output, Q of the NAND SR latch with detail labelling.

(4 marks)

(ii) Construct a table to record the output, Q of the NAND SR latch as the counter steps through its 4 states beginning with $C_1C_0 = 00$. Assume the output is initially SET.

(4 marks)

(b) Figure 2(b) shows a 4-bit synchronous counter, which is designed to perform a specific counting sequence.

Flip-flop FF3 is MSB and flip-flop FF0 is LSB. Flip-flop J_3K_3 has outputs Q_3 and $\overline{Q_3}$, flip-flop T_2 has outputs Q_2 and $\overline{Q_2}$, flip-flop S_1R_1 has outputs Q_1 and $\overline{Q_1}$, and flip-flop D_0 has outputs Q_0 and $\overline{Q_0}$. Assume all flip-flops are initially in 0000 (State 0) for $Q_3Q_2Q_1Q_0$.

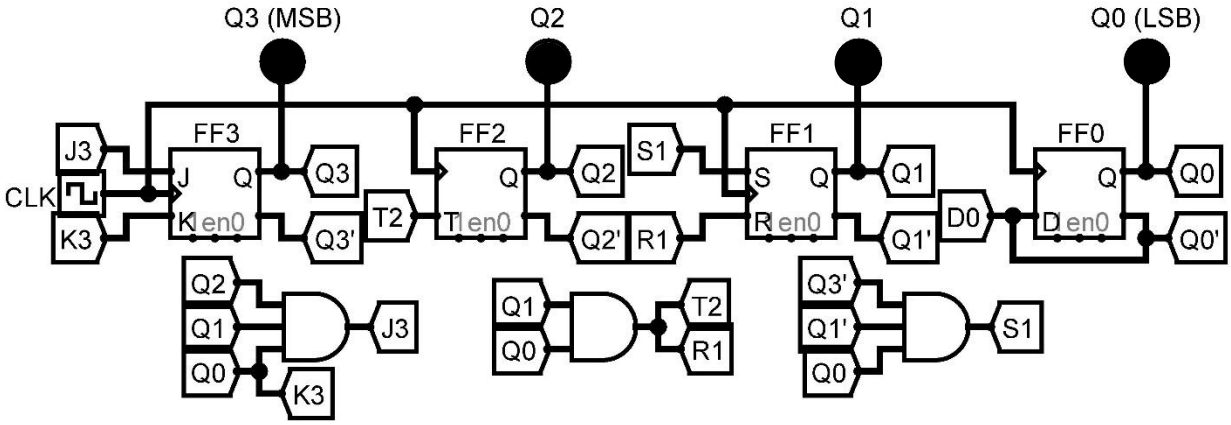

Figure 2(b)

Show all workings clearly according to the procedures listed in part (b)(i), (b)(ii), (b)(iii) and (b)(iv).

(i) Provide all input Boolean expressions (D_0, S_1, R_1, T_2, J_3 and K_3) obtained from Figure 2(b).

(3 marks)

(ii) Produce the Karnaugh maps according to the Boolean expressions obtained in part (b)(i).

(6 marks)

(iii) Build the transition table/next state table from the Karnaugh maps obtained in part (b)(ii).

(4 marks)

(iv) Sketch the state diagram(s) obtained in part (b)(iii) and comment on the states obtained.

(4 marks)

Question 3

(a) Solve the numbering system transformation of [$186.32_{16} \times 14.25_{8}$] to its binary equivalent with 13 binary points accuracy. Show all workings clearly.

(5 marks)

(b) Table 3(b) shows a portion of quadruple 2-input OR gates (DM74LS32) datasheet. Compute the following parameters from this datasheet, show all working clearly:

(i) Power dissipation, $P_{D(max)}$ on a DM74LS32 IC when the output condition is as shown in Figure 3(b). Assume that the V_{CC} used is maximum.

(3 marks)

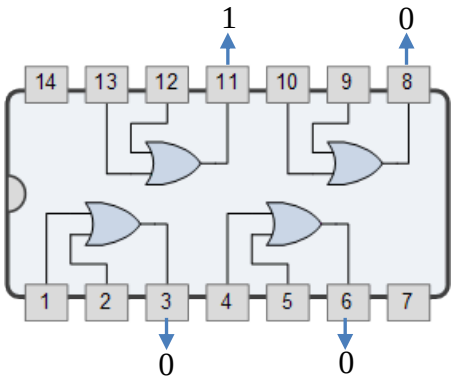

Figure 3(b)

(ii) Fan-out, the number of gates from the same IC family that can be safely driven by an output under worst-case consideration.

(3 marks)

Table 3(b)

Symbol	Parameter	DM54LS32			DM74LS32			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Input Current			–0.4			–0.4	mA
I_{OL}	Low Level Input Current			4			8	mA
T_A	Free Air Operating Temperature	–55		125	0		70	°C

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = –12mA				–1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				–1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	–20		–55	mA
			DM74	–18		–55	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			6	12	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			18	33	mA

(c) Explain the reason for connecting input B as shown in Figure 3(c). Show using diagram another method of connection that is also performing the same outcome. Assume that Figure 3(c) is a TTL gate. The solution should include the truth table.

(6 marks)

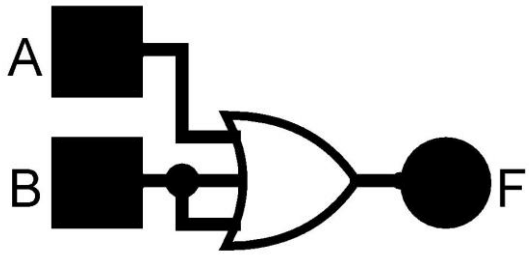

Figure 3(c)

(d) Figure 3(d) has three inputs (A, B, C) and two outputs (Y, Z).
Table 3d(i) shows a portion of quadruple 3-input AND gates datasheet.
Table 3d(ii) shows a portion of quadruple 2-input OR gates datasheet.
Table 3d(iii) shows a portion of quadruple 2-input NAND gates datasheet.
Table 3d(iv) shows a portion of hextuple NOT gates datasheet.

(i) Using the datasheets given, determine the maximum propagation delay time. Show all working clearly.

(7 marks)

(ii) Determine the maximum operating frequency that can be applied to Figure 3(d) without affecting its functionality. Show all working clearly.

(1 mark)

Table 3d(i)

Symbol (DM74LS11)	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	4	13	6	18	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	11	5	18	ns

Table 3d(ii)

Symbol (DM74LS32)	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	11	4	15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	11	4	15	ns

Table 3d(iii)

Symbol (DM74LS00)	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	10	4	15	ns

Table 3d(iv)

Symbol (DM74LS04)	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	10	4	15	ns

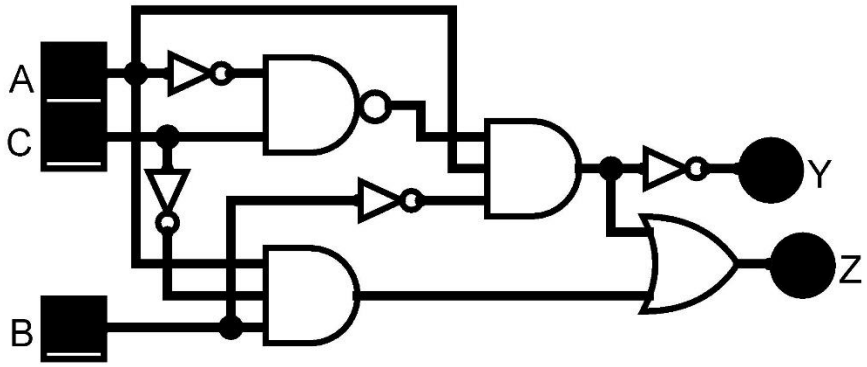

Figure 3(d)

Question 4

(a) Compute the 2's complement number of -2021.125_{10} in signed binary numbering system. Assuming the binary system is 12-bit system with 4 binary points. Show all workings clearly.

(5 marks)

(b) Figure 4(b) shows a computer controlling the speed of a motor. The 0 to 2mA analog current from the DAC is amplified to produce motor speeds from 0 to 2000 rpm (revolutions per minute).

(i) Compute the number of bits should be used if the computer is able to produce a motor speed that is within 2 rpm of the desired speed.

(5 marks)

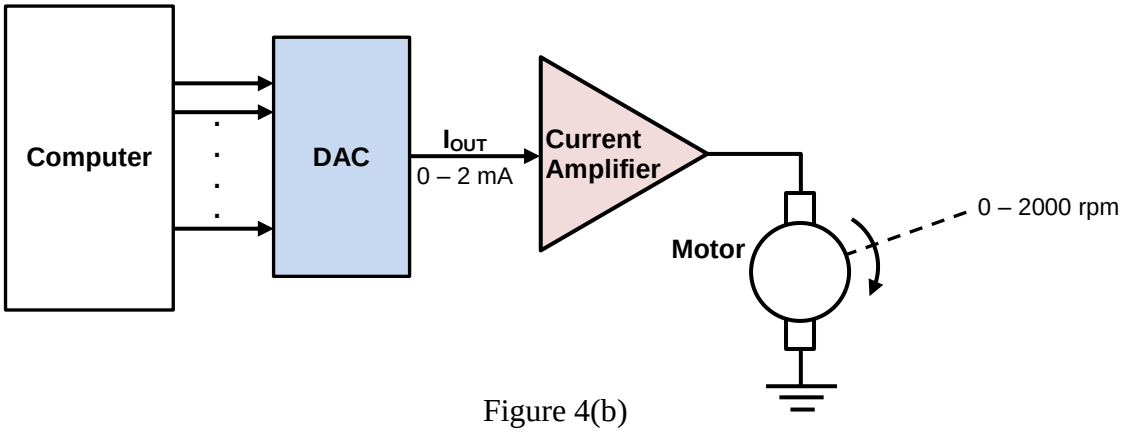

Figure 4(b)

(ii) Using the number of bits obtained in part (b)(i), compute the nearest motor speed (in rpm) achievable if 666 rpm is required.

(5 marks)

(c) Analog to Digital Converter (ADC) is an important element in signal processing for digital conversion of sensor signal. In the case of digitizing a Celsius signal measured by a temperature sensor with the characteristics shown in Table 4(c).

Table 4(c)

Sensitivity	(±0.2%) 10 mV/°C
Measurement Range	(±2.0%) –40 °C to +110 °C
Output Current	10 mA

Assume the formula given is $resolution = \frac{Vrange}{2^n - 1}$.

Apply an appropriate ADC for this sensor application by computing the:

(i) Number of bits.

(7 marks)

(ii) Resolution.

(3 marks)

~THE END~