



**FINAL
ALTERNATIVE ASSESSMENT**

(COVER PAGE)

Session : January 2022

Programme : Diploma in Electrical & Electronic Engineering (DEEI)

Course : EEE1109: Analogue Electronics

Date of Examination : 9 March 2022 (Wednesday)

Time : 8.00am – 11.00am Reading Time : Nil

Duration : 3 Hours

Special Instructions :

This paper consists of **FOUR (4)** questions. Answer **ALL FOUR (4)** questions. All questions carry equal marks.

Material permitted : Non-Programmable Scientific Calculator

Materials provided : Nil

Examiner(s) : Dr. Su Hsiao Wei

Chief Moderator : Dr. Solahuddin

This paper consists of 9 printed pages, including the cover page

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
 EEE1109: ANALOGUE ELECTRONICS
 FINAL ALTERNATIVE ASSESSMENT: JANUARY 2022 SESSION

Instructions: This paper consists of **FOUR (4)** questions. Answer **ALL FOUR (4)** questions. All questions carry equal marks.

Question 1

- (a) Figure 1(a) shows a single stage field effect transistor (FET) amplifier and its voltage gain frequency response.

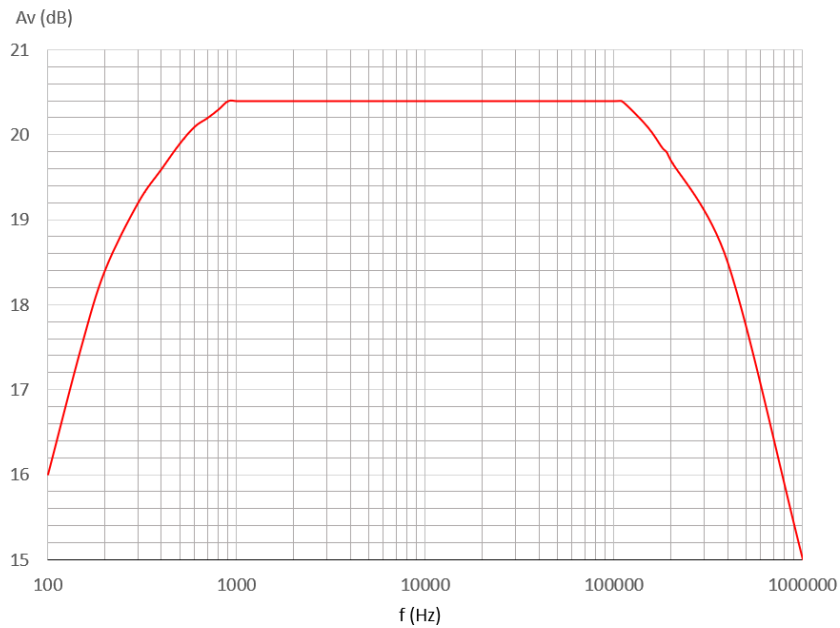
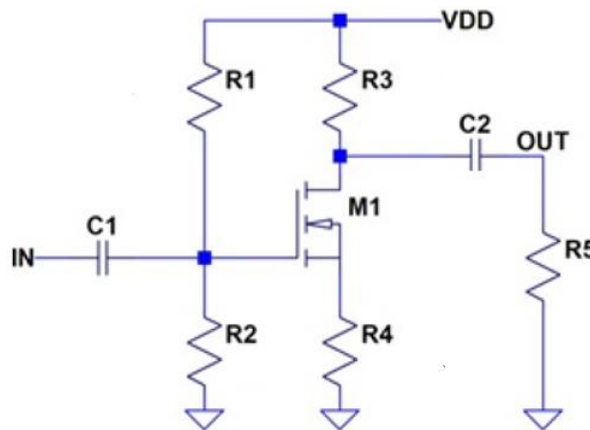


Figure 1(a)

From the amplifier's voltage gain response, do the followings:

- (i) Identify the maximum amplifier gain. (2 marks)
- (ii) Find the upper and lower cutoff frequencies. Then estimate the bandwidth of the amplifier. (3 marks)
- (iii) Explain a way to reduce the amplifier lower cutoff frequency. State any assumption made. (3 marks)

- (b) Figure 1(b) shows a single-stage enhancement metal oxide semiconductor field effect transistor (E-MOSFET) amplifier. The E-MOSFET has the following quiescent value:
 $I_{DQ} = 2.5mA$

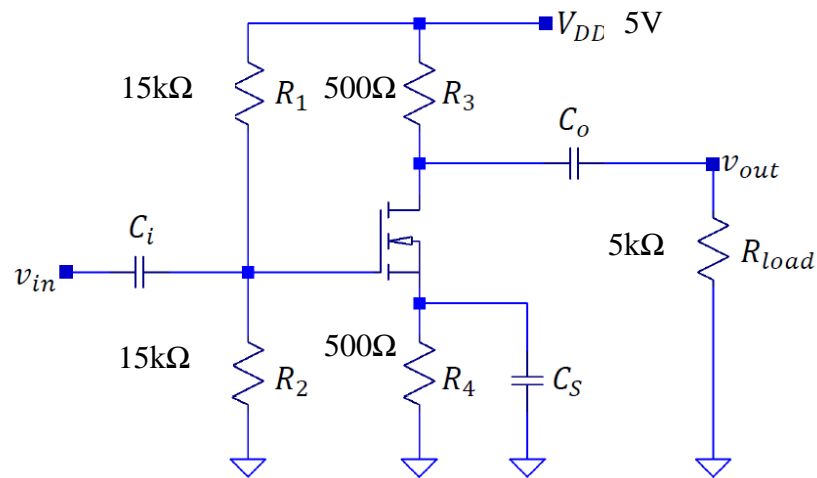


Figure 1(b)

- (i) Explain the purpose of the capacitor C_i and C_o in the circuit. (2 marks)
- (ii) Calculate the quiescent voltages of V_{GQ} and V_{SQ} (2 marks)
- (iii) Calculate the quiescent voltages of V_{GSQ} , V_{DQ} and V_{DSQ} . (3 marks)

(c) Figure 1(c) shows the AC equivalent circuit model of an FET voltage amplifier.

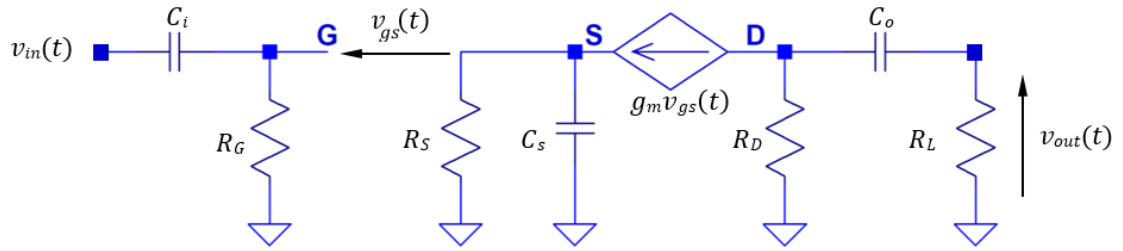


Figure 1(c)

(i) Modify the AC equivalent circuit model to evaluate the cutoff frequency contributed by capacitor C_o . (2 marks)

(ii) Draw the AC equivalent circuit model obtained in part 1(c)(i). Show that the voltage transfer function of $V_{OUT}(s)/V_{IN}(s)$ can be expressed in the form of,

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{a_0 s}{s + \omega_o}$$

and state a_0 and ω_o in terms of the relevant passive components and transistor parameter, g_m . Obtain the upper cutoff frequency of the amplifier which is contributed by capacitor C_o .

(6 marks)

(iii) Quantitatively explain a way to increase the amplifier upper cutoff frequency.

(2 marks)

Question 2

(a)

(i) For the operational-amplifier (op-amp) circuit as shown in Figure 2(a), assuming the op-amps are ideal, apply the relevant circuit or op-amp rules and principles to derive the expression for the overall gain

$$A_v = \frac{V_{out}}{V_{in}}$$

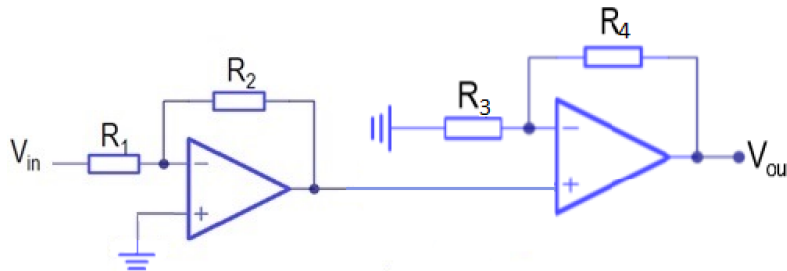


Figure 2(a)

- (ii) Explain the operation of the op-amp circuit in Figure 2 (a) with the aid of a diagram showing the input, intermediate, and output time-domain voltage waveforms with clear labels. Assuming the input voltage signal is sinusoidal and the op-amps operate in linear region from a dual-supply voltage and assuming $R_2 > R_1$ and $R_4 > R_3$. (6 marks)
- (4 marks)
- (iii) If $R_2 = R_4 = 2R$ and $R_1 = R_3 = R$, calculate the overall voltage gain (in dB) of the op-amp circuit in Figure 2(a). (2 marks)

(b) Figure 2(b) shows an op-amp circuit implemented with the following specifications:

$$V(max) = \pm 18 \text{ V}$$

$$slew\ rate = 18 \text{ V}/\mu\text{s}$$

$$|V_{out(sat)}| = |V_S| - 1 \text{ V}$$

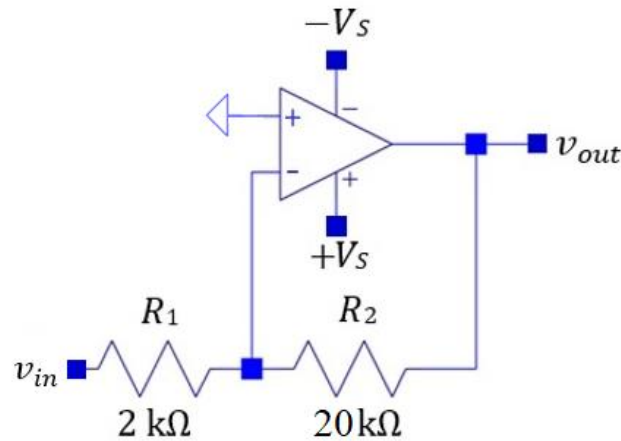


Figure 2(b)

If $v_{in} = 2\sin(300000\pi t)$, do the followings:

- (i) Calculate the maximum output voltage V_{out} of the amplifier. Justify the suitability of the op-amp implementation from the saturation voltage point of view. (4 marks)
- (ii) Calculate the maximum rate of change of the amplifier output. Justify the suitability of the op-amp implementation from the slew-rate point of view. (5 marks)

- (iii) Suggest a design based way to reduce the maximum rate of change of the op-amp circuit output in Figure 2(b) assuming the input signal sine wave amplitude and frequency are fixed. Justify your answer.

(4 marks)

Question 3

- (a) Copy Table 3(a) into your answer script and complete the blank cells in the table by stating two pros and cons of the listed passive and active filters.

Table 3(a)

		Passive Filter	Active Filter
Pros	1		
	2		
Cons	1		
	2		

(4 marks)

- (b) A filter is implemented based on the cascade of 3 analogue circuit building blocks, as shown in Figure 3(b).

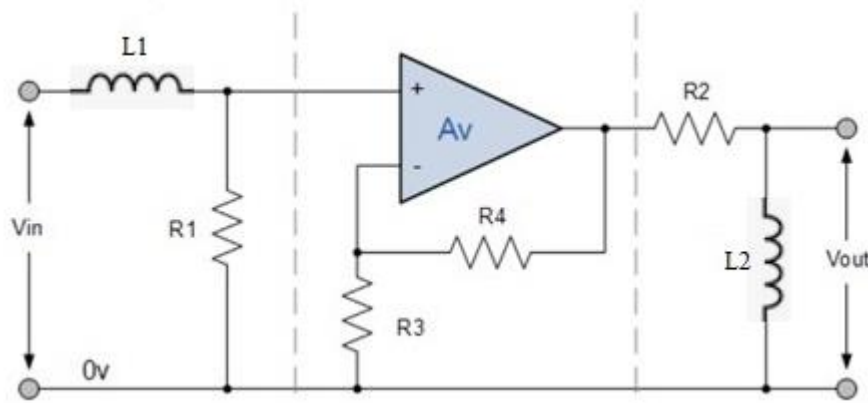


Figure 3(b)

- (i) Identify and label the building blocks. (2 marks)
- (ii) Based on elementary filter voltage transfer functions, derive the filter voltage transfer function $(V_{out}(s)/V_{in}(s))$. (6 marks)
- (iii) Identify the type and order of the filter based on the voltage transfer function expression obtained in Q3(b)(ii). (2 marks)

- (c) A filter is realized by cascading two different filter building blocks and the overall filter transfer function is expressed as

$$T(s) = \left(\frac{1}{s + 30} \right) \left(\frac{s}{s + 30} \right)$$

- (i) Identify the type and order of the filter. Quantitatively justify your answers. (3 marks)
- (ii) Calculate the filter cut-off frequencies (lower and upper) in rad/s. (6 marks)
- (iii) Identify the filter type (passive or active). Quantitatively justify your answer. (2 marks)

Question 4

- (a) Briefly explain the followings pertaining to an oscillator circuit.
 - (i) Functionality. (2 marks)
 - (ii) Output design requirements. (2 marks)
- (b) Figure 4(b) shows a relaxation oscillator constructed from a 555 timer integrated circuit (IC).

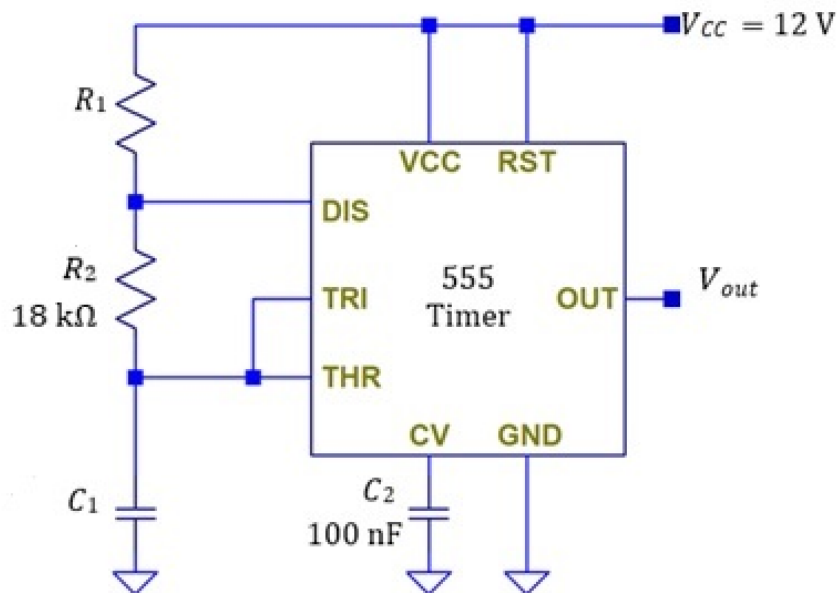


Figure 4(b)

- (i) If the desired oscillation frequency of the output signal V_{out} is 863Hz, determine the design values of resistor R_1 and capacitor C_1 . State any assumption made. (3 marks)
- (ii) Calculate the duty cycle of the output signal in %, based on your resistor values in Q4(b)(i). (2 marks)
- (iii) Derive the design relationship between the resistors R_1 and R_2 if duty cycle of 88% is targeted. (2 marks)
- (iv) Explain a way to double the oscillation frequency without affecting the duty cycle. (3 marks)

(c) Figure 4(c) shows a Wien Bridge oscillator circuit.

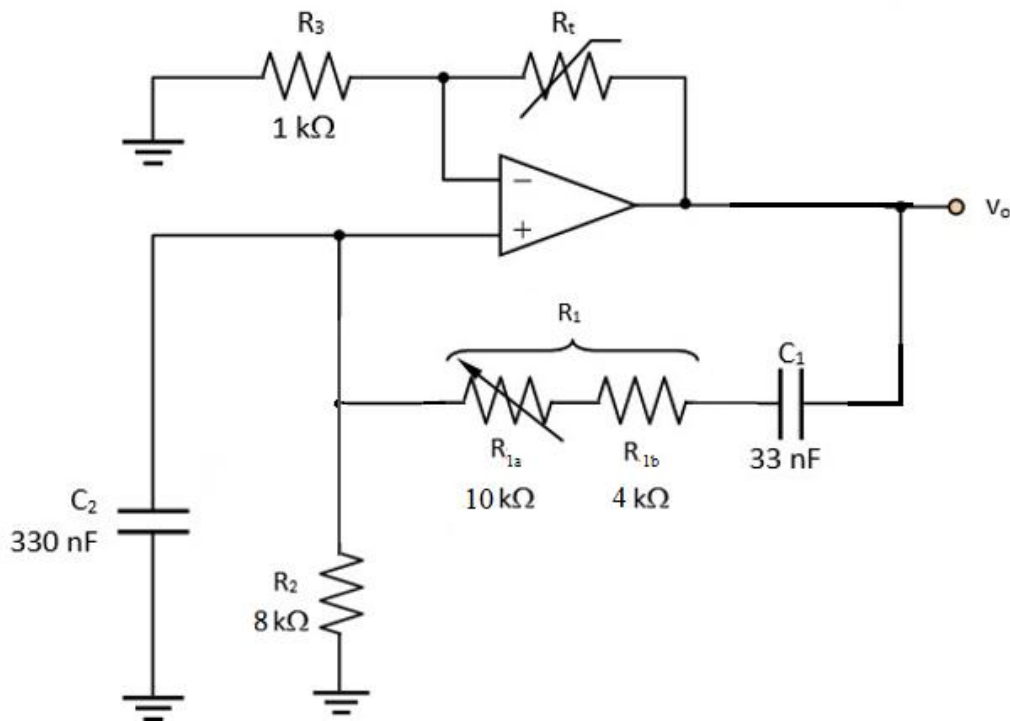


Figure 4(c)

- (i) Explain the purpose of the fixed resistor R_{1b} . (2 marks)
- (ii) Explain the purpose of the thermistor R_t . (2 marks)
- (iii) The positive feedback circuit transfer function is expressed as
$$\frac{V_f}{V_o} = \frac{\omega C_1 R_2}{\omega(C_1 R_1 + C_2 R_2 + C_1 R_2) - j(1 - \omega^2 C_1 C_2 R_1 R_2)}$$

Find the expression for the resonant angular frequency.

Prove that for the circuit to sustain oscillation, the oscillator's amplifier resistor relationship is given by $2R_1 = 21R_3$. Assuming $R_2 = 2R_1$ and $C_2 = 10C_1$.

(5 marks)

- (iv) Calculate the range of oscillation frequency when R_{1a} is adjusted between its extreme ends.

(2 marks)

~THE END~

EEE1109 (F) / January 2022 Session / formatted