



INTI
International College Penang
LAUREATE INTERNATIONAL UNIVERSITIES*

FINAL
Examination Paper

(COVER PAGE)

Session : January 2017

Programme : Diploma in Electrical and Electronic Engineering (DEEI)

Course : EEE2101: Introduction To Digital Electronics

Date of Examination : 7 March 2017 (Tuesday)

Time : 11:00am – 1:00pm Reading Time : Nil

Duration : 2 Hours

Special Instructions :

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL

Materials permitted : Non-Programmable Scientific Calculator

Materials provided : Nil

Examiner(s) : Mr. Steven Khoo Boo Tap

Moderator : Mr. Kevin Tan Geok Su

This paper consists of 11 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
 EEE2101: INTRODUCTION TO DIGITAL ELECTRONICS
 FINAL EXAMINATION: JAN2017 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

- (a) A combinational logic circuit is required, which accepts BCD inputs 0000 to 1001 and displays the letter 'ACEFHJLOPS', respectively, as shown below in Figure 1(a-1). The BCD inputs are labelled as KLMN, J is the MSB and M is the LSB. Figure 1(a-2) shows a Common-Anode 7 segment display. Assume all unused inputs as don't care.

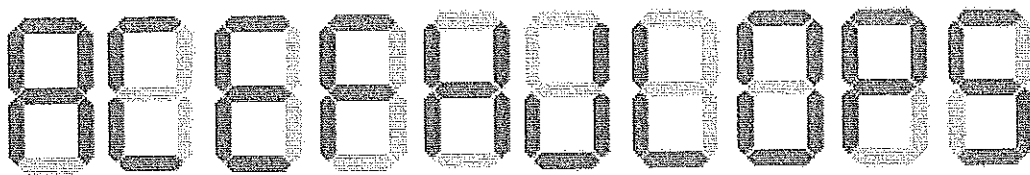


Figure 1(a-1)

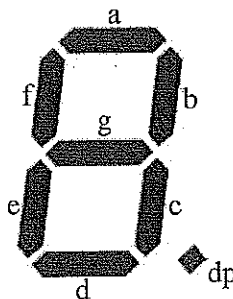


Figure 1(a-2)

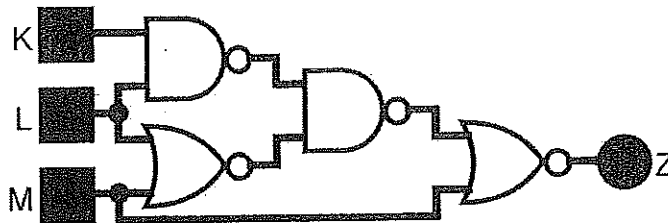
- (i) Develop the truth table for the inputs to segments a through g of the 7 segment. (4 marks)
- (ii) Determine the SOP form of the logic expression for segments b and c. (6 marks)
- (iii) Implement the logic expression using only 3-input NAND gate with minimum 7410 ICs consideration. State the number of ICs used. Show all working clearly. (7 marks)

(b) Using Boolean algebra only, simplify to the simplest logic form in term of gate(s):

(i)
$$y = \overline{AC}(\overline{ABD}) + \overline{A} \cdot B \cdot \overline{C} \cdot \overline{D} + \overline{ABC}$$

(4 marks)

(ii)



(4 marks)

Question 2

(a) Table 2(a) and Table 2(b) show a portion of a dual positive edge-triggered JK flip-flops (DM7476) and a triple 3-input AND gate datasheet respectively. Figure 2(a) show the logic circuit diagram of an asynchronous counter which uses positive edge-triggered JK flip-flops with labelling of $Q_A Q_B Q_C Q_D$ where Q_D is MSB and Q_A is LSB. Assume the environment is at $T_A = 25^\circ\text{C}$ with $V_{CC} = 5\text{V}$.

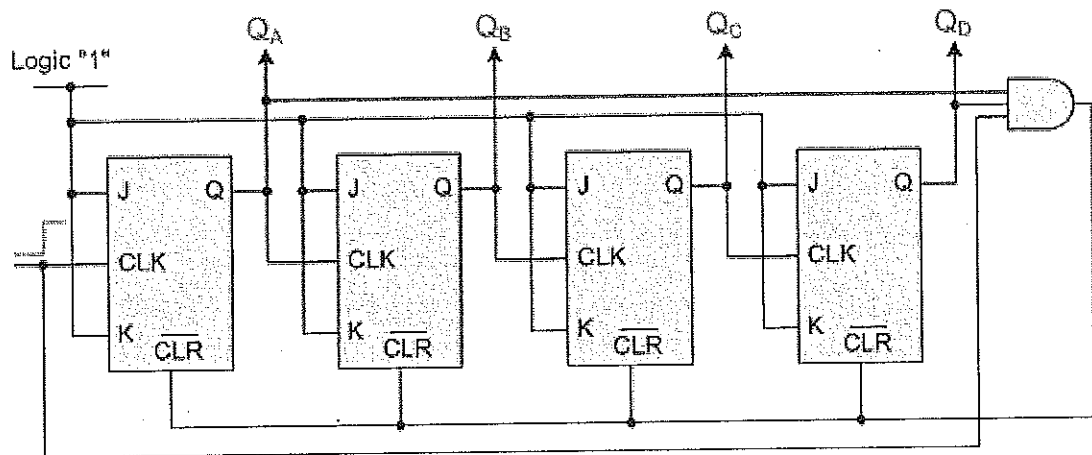


Figure 2(a)

Switching Characteristics					
at $V_{CC} = 5\text{V}$ and $T_A = 25^\circ\text{C}$					
Symbol	Parameter	From (Input) To (Output)	$R_t = 400\Omega$; $C_L = 15\text{pF}$		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		15		MHz
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Preset to \overline{Q}		40	ns

t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Preset to Q		25	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Q		40	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clear to \bar{Q}		25	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Q or \bar{Q}		40	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Q or \bar{Q}		25	ns

Table 2(a) JK flip-flop

Symbol	From (Input)	To (Output)	Test Conditions	Min	Typ	Max	Units
t_{PLH}	A, B or C	Y	$C_L = 15 \text{ pF}, R_L = 2\text{k}\Omega$		8	27	ns
t_{PHL}					10	19	ns

Table 2(b) AND gate

- (i) Determine the total propagation delay from the given datasheets in Table 2(a) and Table 2(b). (5 marks)
- (ii) Determine the maximum frequency at which the counter can be operated stably. (3 marks)
- (iii) Show the output timing diagram of Figure 2(a) and state the function of this counter. (5 marks)
- (b) Perform the following number system transformation. Show all workings clearly.
- (i) $[3020.3020_{16} - 1001.1001_8]$ to decimal equivalent with 6 decimal points accuracy. (4 marks)
- (ii) $[11010.101_2 \times 11.1_8]$ to binary equivalent with 8 binary points accuracy. (4 marks)
- (iii) $[163.0703125_{10} + 11.101_8]$ to hexadecimal equivalent with 3 hexadecimal points accuracy. (4 marks)

Question 3

- (a) Design a synchronous 3-bit up/down Gray code counter using positive edge-triggered T flip-flops only. Assume T_A is the MSB and T_C is the LSB inputs. Input Y will be used as the up/down controller. The counter will count from $000 \Rightarrow 001 \Rightarrow 011 \Rightarrow 010 \Rightarrow 110 \Rightarrow 111 \Rightarrow 101 \Rightarrow 100 \Rightarrow 000$ for counting up when input, $Y = 0$ and $000 \Rightarrow 100 \Rightarrow 101 \Rightarrow 111 \Rightarrow 110 \Rightarrow 010 \Rightarrow 011 \Rightarrow 001 \Rightarrow 000$ for counting down when input, $Y = 1$. Use $Q_A Q_B Q_C$ outputs labelling for T_A , T_B and T_C inputs. Provide proper labelling for the designed logic circuit. Show all workings clearly.
- Provide the excitation table used and the state diagram. (2 marks)
 - Provide the transition table/ next state table. (4 marks)
 - Simplify using Karnaugh map and Boolean algebra if necessary. (6 marks)
 - Draw the complete logic circuit diagram with proper label. (5 marks)
- (b) A chemical plant needs a microprocessor driven alarm (A) system to warn of critical conditions in one of its chemical tanks. The tank has four HIGH/LOW (Input/Output) switches that monitor temperature (T), pressure (P), fluid level (L) and weight (W). Design a system that will notify the microprocessor to activate an alarm when any of the following conditions arise:
- High fluid level with high temperature and high pressure.
 - Low fluid level with high temperature and high weight.
 - Low fluid level with low temperature and high pressure.
 - Low fluid level with low weight and high temperature.
- (8 marks)

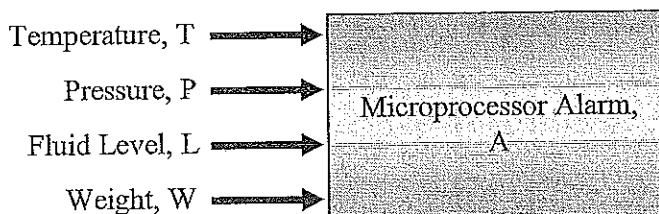


Figure 3(b)

Question 4

- (a) For the pulse shown in Figure 4(a) below, graphically determine the Rise time, Fall time, Pulse time and Amplitude.

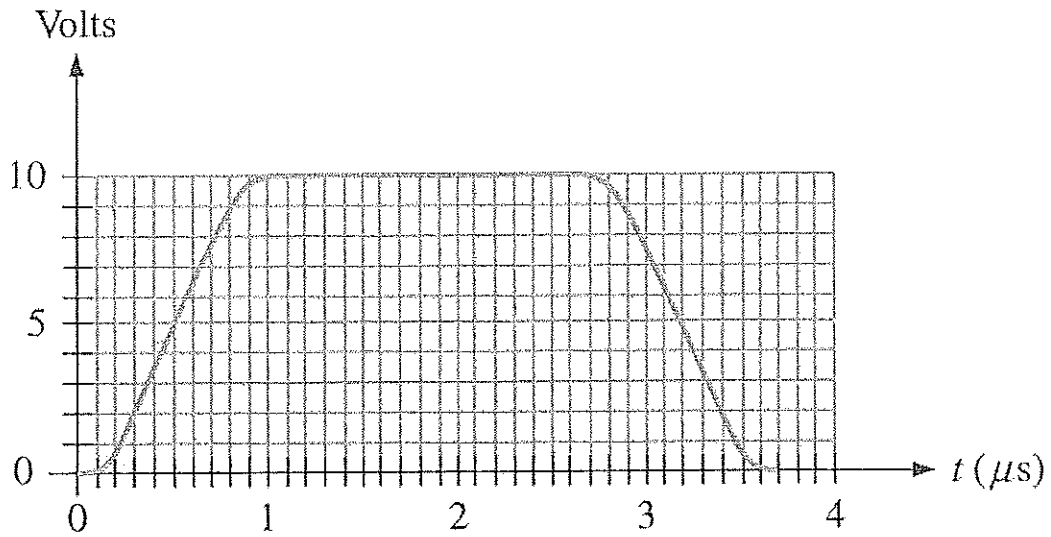


Figure 4(a)

(4 marks)

- (b) Figure 4(b) below shows a 4-bit synchronous counter which is designed so that it performs a special counting sequence. Analyse its operation by determining its counting sequence. Assume that all flip-flops are initially in the 0 state (0000) for $Q_3Q_2Q_1Q_0$. Flip-flop FF3 is MSB and FF0 is LSB. Use J_3K_3 , J_2K_2 , J_1K_1 and J_0K_0 inputs labelling for Q_3 , Q_2 , Q_1 and Q_0 outputs. Show all workings clearly.

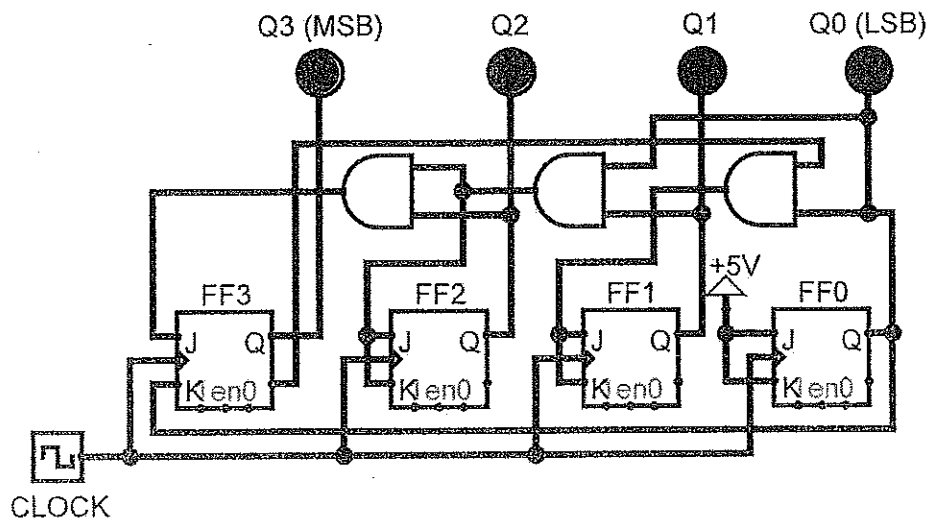


Figure 4(b)

- (i) Provide the Boolean expressions from the logic circuit. (2 marks)
- (ii) Provide all Karnaugh maps according to the expressions. (4 marks)
- (iii) Provide the transition table/ next state table with excitation table. (5 marks)
- (iv) Draw the state diagram and comment on the outcome of the states obtained. (4 marks)

- (c) A binary-weighted-input DAC is shown in Figure 4(c). If the LSB bit resistor has a value of $480\text{k}\Omega$, compute the values of the other input resistors. Also, calculate the V_{out} if the DAC has a binary input of 1010 with Logic 1 (HIGH) as $+3.0\text{V}$ and Logic 0 (LOW) as 0V . Assume that R_f equals to $10\text{k}\Omega$. What are the disadvantages of this method of DAC? (6 marks)

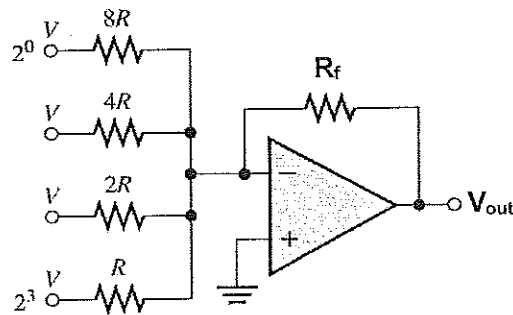


Figure 4(c)

Question 5

- (a) Figure 5(a) represents an adder circuit that takes two-bit binary numbers X_1X_0 and Y_1Y_0 and produces an output binary number Z_1Z_0 and Carry that is equal to the arithmetic addition of the two input numbers.

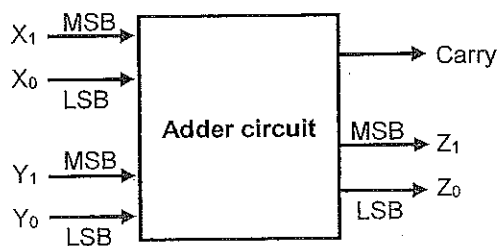


Figure 5(a)

Design the logic circuit for the adder. Show all working clearly. Hint: The logic circuit will have four inputs and three outputs as shown in Table 5(a).

i) Complete the truth table below.

Input X		Input Y		Output Z		Carry
X_1	X_0	Y_1	Y_0	Z_1	Z_0	
0	0	0	0	0	0	0
0	0	0	1	0	1	0
.
1	1	1	0	0	1	1
1	1	1	1	1	0	1

Table 5(a)

(3 marks)

ii) Simplify the Boolean expression to the simplest form using Karnaugh map and/or Boolean algebra for output Z_1 , Z_0 and Carry.

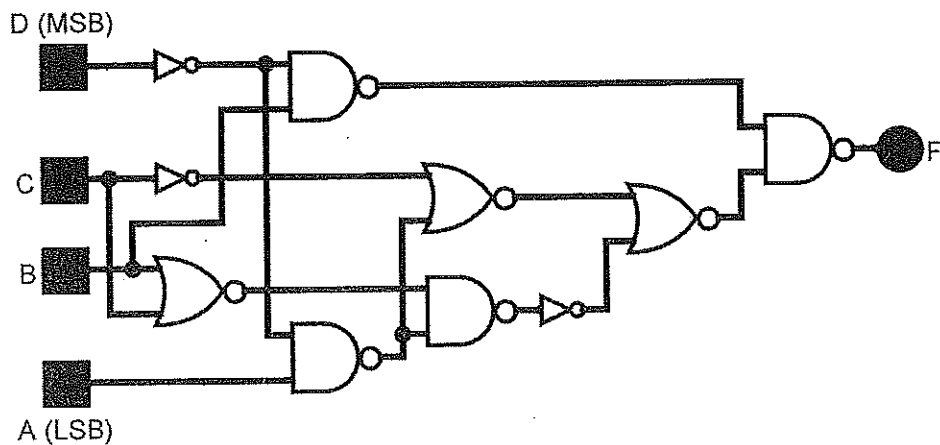
(9 marks)

iii) Implement the logic circuit of the simplest Boolean expression for Z_1 using minimum number of gates for your design.

(5 marks)

(b) Use the given Karnaugh map and/or Boolean algebra to obtain the minimum

(i) POS expression for the logic circuit,



(5 marks)

(ii) SOP expression for the truth table,

R	S	T	U	F
0	0	0	×	1
0	0	1	×	0
0	1	×	×	1
1	0	0	×	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	×	0

(3 marks)

Question 6

(a) Figure 6(a) has three inputs (A, B, C) and two outputs (Y, Z).
 Table 6a(i) shows a portion of quadruple 2-input AND gates datasheet.
 Table 6a(ii) shows a portion of quadruple 2-input OR gates datasheet.
 Table 6a(iii) shows a portion of quadruple 2-input XOR gates datasheet.
 Table 6a(iv) shows a portion of hex-tuple NOT gates datasheet.

(i) Using the datasheets given, determine the maximum propagation delay time. Show all working clearly.

(6 marks)

(ii) What is minimum operating frequency that can be applied to this circuit without affecting the functionality of the circuit? State the function of this circuit.

(4 marks)

Symbol	Parameter	Conditions	Min	Max	Units
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	C _L = 15 pF R _L = 400Ω		27	ns
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			19	ns

Table 6a(i) AND gate

Symbol	Parameter	R _L = 2 kΩ				Units
		C _L = 15 pF		C _L = 50 pF		
		Min	Max	Min	Max	
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	11	4	15	ns
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	11	4	15	ns

Table 6a(ii) OR gate

Symbol	Parameter	Conditions	CL = 15 pF, RL = 400Ω		Units
			Min	Max	
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Other input LOW		23	ns
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			17	ns
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Other input HIGH		30	ns
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			22	ns

Table 6a(iii) XOR gate

Symbol	Parameter	RL = 2 kΩ				Units
		CL = 15 pF		CL = 50 pF		
		Min	Max	Min	Max	
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	10	4	15	ns
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	10	4	15	ns

Table 6a(iv) NOT gate

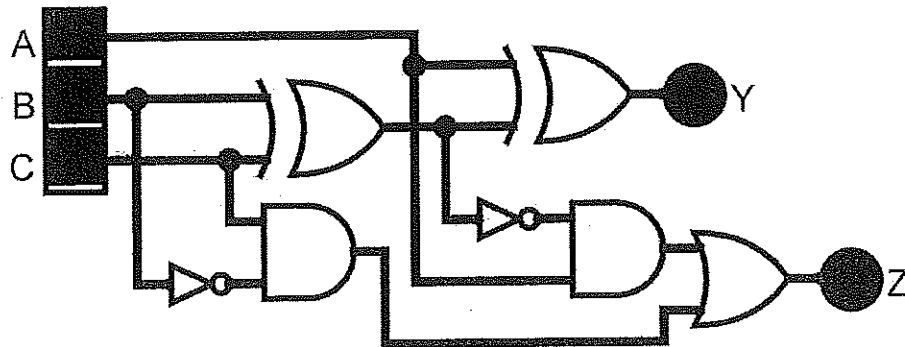


Figure 6(a)

- (b) An 8-bit DAC produces an output current in proportion to its digital input. For a digital input of 01010000, an output current of 75mA is produced.
- (i) What will the output current be if the digital input is 10010001? (3 marks)
 - (ii) What is the maximum output current produced by this DAC? (2 marks)
 - (iii) What should the digital input be if a 120mA output current is required? (2 marks)

- (c) Table 6(c) shows the current ratings of TTL series logic gates. A 74LS04 NOT gate output is driving 2 (TWO) Standard TTL gate inputs, 3 (THREE) Advanced Low-Power Schottky TTL gate inputs, 4 (FOUR) Fast TTL gate inputs and 1 (ONE) Schottky TTL gate input as shown in Figure 6(c). Determine if there is a loading problem.

(8 marks)

TTL Series	Output Drive		Input Loading	
	I_{OH}	I_{OL}	I_{IH}	I_{IL}
74	400 μ A	16mA	40 μ A	1.6mA
74S	1.0mA	20mA	50 μ A	2.0mA
74LS	400 μ A	8mA	20 μ A	400 μ A
74AS	2.0mA	20mA	200 μ A	2.0mA
74ALS	400 μ A	8mA	20 μ A	100 μ A
74F	1.0mA	20mA	20 μ A	600 μ A

Table 6(c)

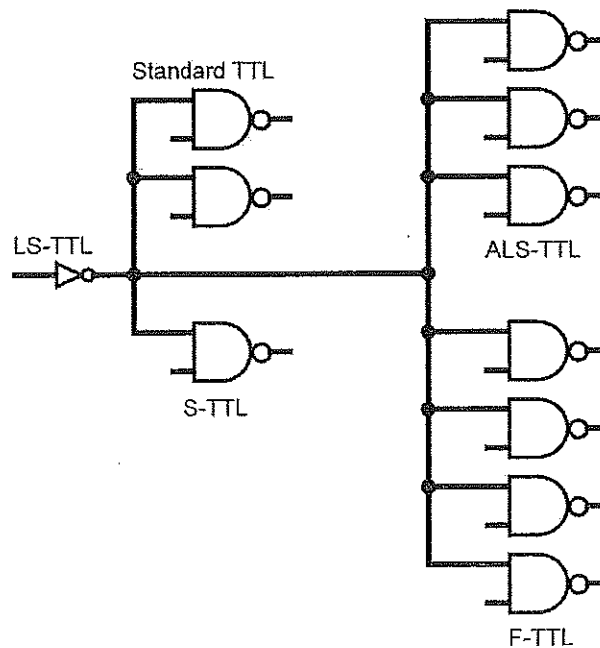


Figure 6(c)

-- THE END --

