

**INTI**

**International College Penang**

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**FINAL**  
Examination Paper

(COVER PAGE)

Session : January 2017

Programmes : Diploma In Electrical And Electronic Engineering (DEEI)

Course : EEE1106: Analogue Electronics

Date of Examination : 6 March 2017 (Monday)

Time : 11:00am – 1:00pm

Duration : 2 Hours Reading Time: Nil

Special Instructions :

This paper consists of SIX (6) questions. Answer any FOUR (4) questions in the answer booklet provided. All questions carry equal marks.

**IMPORTANT NOTE : THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL BY THE STUDENTS.**

Materials Permitted : Scientific Calculator (Model fx570 Series)

Materials Provided : Nil

Examiner(s) : Chan Tse Wei

Moderator : Dr. Khoo Bee Ee

*This paper consists of 10 printed pages, including the cover page.*

## INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)

EEE1106: ANALOGUE ELECTRONICS

FINAL EXAMINATION: JANUARY 2017 SESSION

**Instructions:** This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks. The marks allocated to each sub-question are shown in square brackets at the right-hand margin. Present your answers neatly and clearly. The assessor reserves the rights to ignore your answers if they are ambiguous.

## Question 1

a. State the three types of configuration of BJT-based single-stage amplifier. For each of the stated configuration, describe its amplification characteristics. [6]

b. The performance of a FET-base single-stage amplifier circuit was being evaluated. Figure-Q1(b) shows the evaluation result.

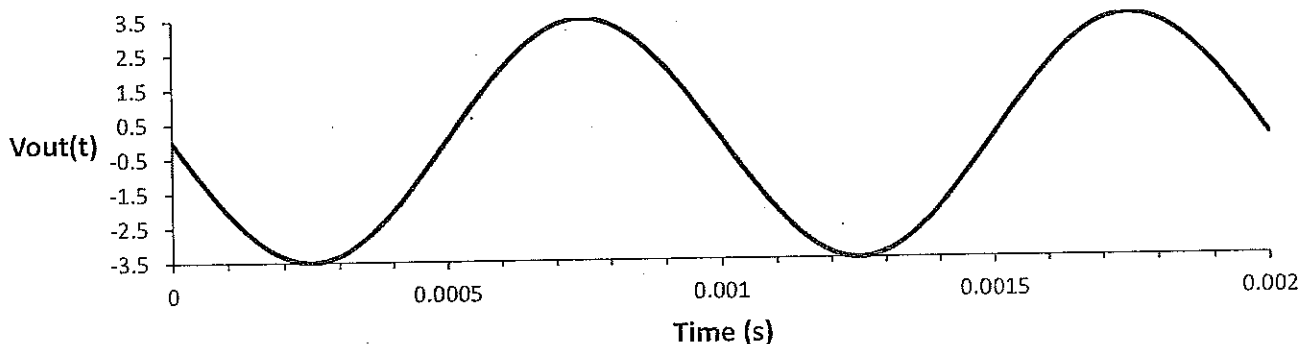
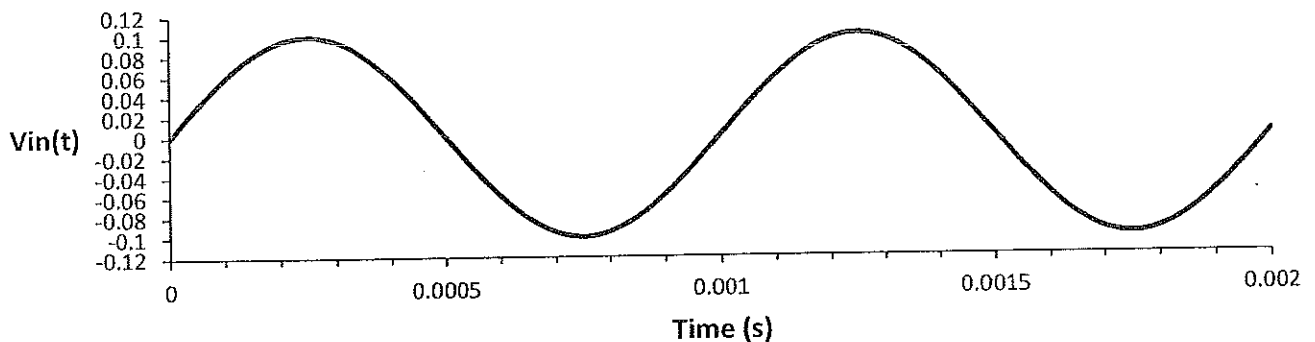


Figure-Q1(b)

- i. State the type of configuration of the amplifier being evaluated. [ 2 ]
  - ii. Calculate the voltage gain of the amplifier circuit. [ 2 ]
  - iii. Express the voltage gain obtained in part (b)(ii) in dB. [ 2 ]
- c. Figure-Q1(c) shows the circuit model of an audio amplifier circuit.  $g_m$  is the transconductance parameter of the active element in the amplifier.

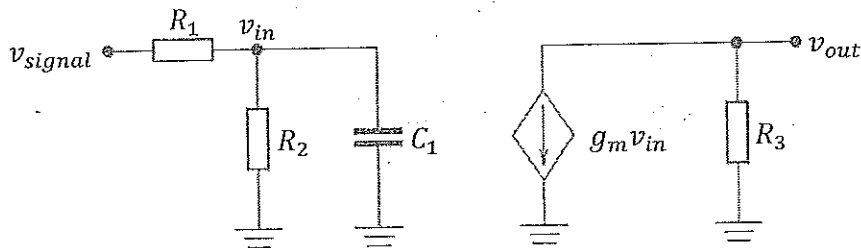


Figure-Q1(c)

- i. Derive the low frequency voltage gain expression,  $v_{out}/v_{signal}$  of the amplifier circuit in terms of the circuit components and  $g_m$ . [ 5 ]
- ii. Quantitatively evaluate the impact on the low frequency voltage gain when a load resistor, with resistance value 10 times smaller than  $R_3$ , is connected across the output terminal and ground. [ 5 ]
- iii. Derive the upper cutoff frequency expression of the amplifier circuit. [ 3 ]

## Question 2

- a.
  - i. Differentiate the respective conduction period of the power transistor used in Class B and Class C power amplifier. [ 4 ]
  - ii. State the main reason one should choose Class C power amplifier instead of Class B for one's design implementation, despite its circuit complexity. [ 2 ]
  - iii. A power amplifier is able to deliver 8 W of AC output power when drawing 12 W power from its DC supplies. Calculate the amount of power loss in the amplifier and its power efficiency in percentage. [ 4 ]

- b. Figure-Q2(b)(i) shows a basic push-pull power amplifier circuit, while Figure-Q2(b)(ii) shows the circuit's voltage transfer curve (VTC),  $v_{out}$  against  $v_{in}$ .

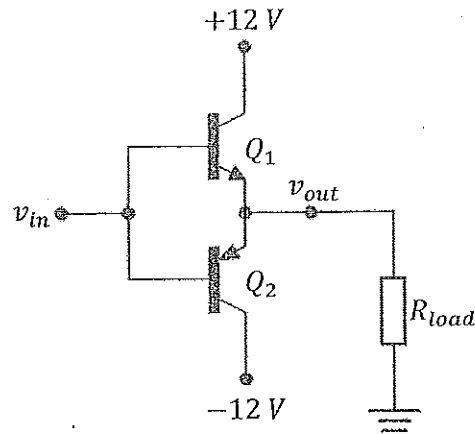


Figure-Q2(b)(i)

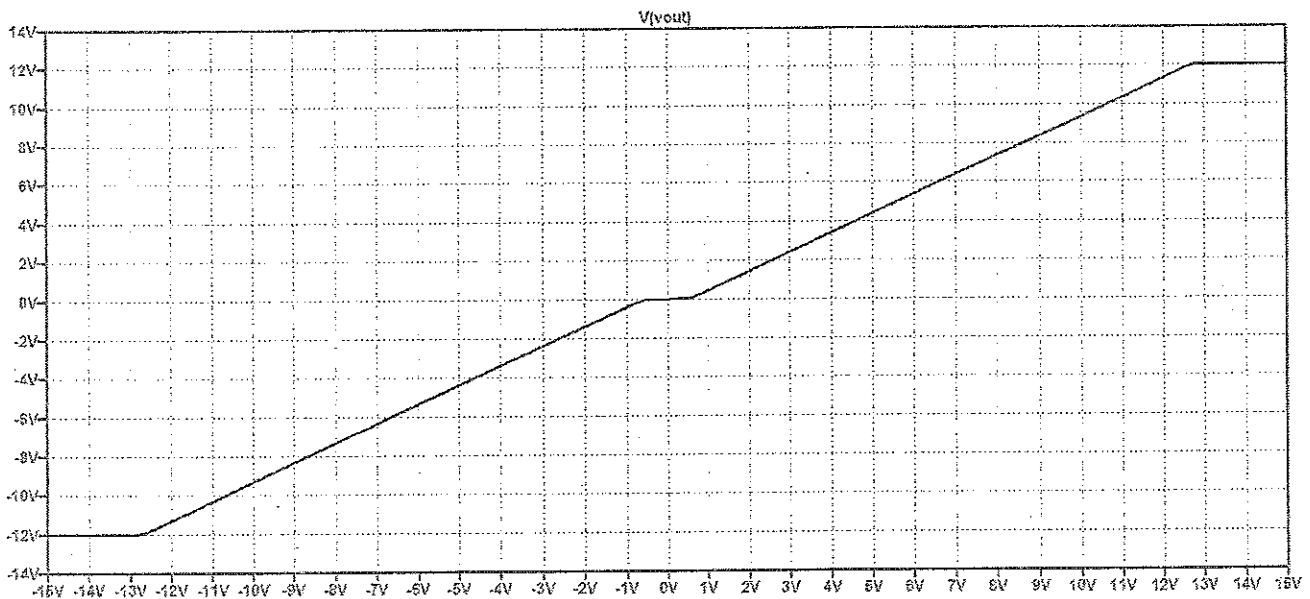


Figure-Q2(b)(ii)

- i. Quantitatively explain the given VTC, closely relating it to the characteristics of the transistors used in the circuit. [ 5 ]
- ii. The circuit in Figure-Q1(b)(i) exhibits thermal runaway problem. Explain this problem. [ 3 ]

- c. Figure-Q2(c) shows an enhanced version of the push-pull power amplifier in Figure-Q2(b)(i).

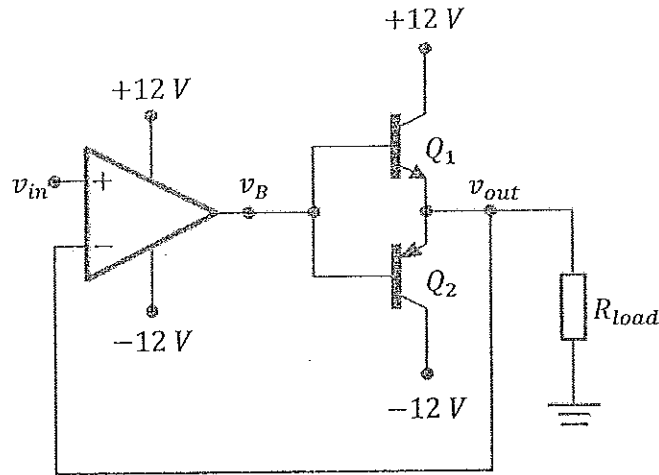


Figure-Q2(c)

- i. Assume ideal op-amp operation, sketch the VTC of the amplifier circuit for  $-3\text{ V} \leq v_{in} \leq 3\text{ V}$ . [ 3 ]
- ii. With reference to Figure-Q2(b)(ii), sketch the timing diagram of  $v_B(t)$  if  $v_{in}(t)$  is a sinusoidal waveform of 2 V peak at 1 kHz. [ 4 ]

## Question 3

Parameter	Symbol	Op-Amp A	Op-Amp B
Maximum Supply Voltage	$V_{CC}$	$\pm 22\text{ V}$	$\pm 16\text{ V}$
Maximum output current	—	1 A	1 A
Operating Temperature Range	$T_{OPR}$	$-25^\circ\text{C}$ to $85^\circ\text{C}$	$-40^\circ\text{C}$ to $120^\circ\text{C}$
Large Signal Voltage Gain	$G_v$	100 V/mV	200 V/mV
Input Resistance	$R_{in}$	800 M $\Omega$	1 T $\Omega$
Common Mode Rejection Ratio	CMRR	70 dB	100 dB
Slew Rate at Unity Gain	SR	13 V/ $\mu\text{s}$	0.5 V/ $\mu\text{s}$

Table-Q3(a)

a. Table-Q3(a) list the typical values of several specifications of two op-amps. Between the two op-amps, choose the one that is most appropriate for each of the following design requirement. Justify your choice.

- i. Buffer signals supplied from a source having a source resistance close to hundredth-M $\Omega$  range. [ 4 ]
- ii. Produce a sawtooth wave with a ramp of 4 V in 2  $\mu$ s. [ 4 ]
- iii. Produce a low frequency sinusoidal output voltage of 18 V peak. [ 3 ]
- iv. Circuit must be independent of noise signals appearing at the op-amp input terminals. [ 3 ]

b. Figure-Q3(b)(i) shows the circuit model of a voltage dependent current source (VDCS), while Figure-Q3(b)(ii) shows the circuit implementation of the VDCS.

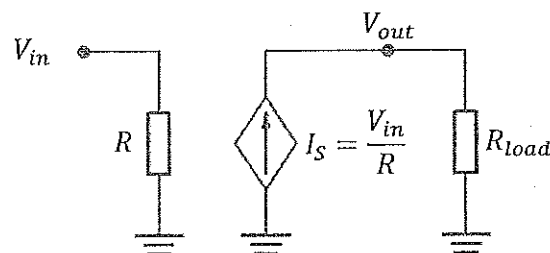


Figure-Q3(b)(i)

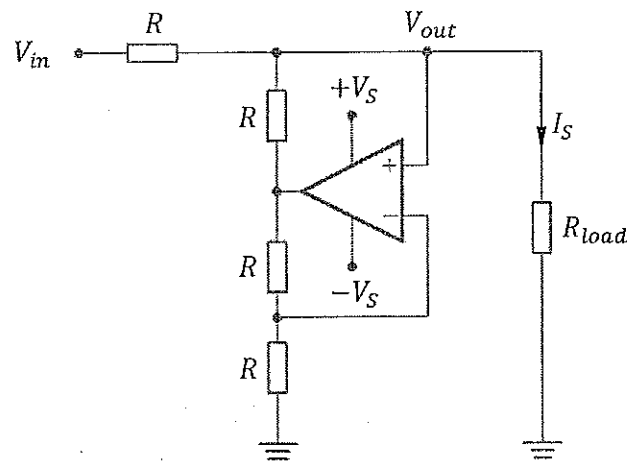


Figure-Q3(b)(ii)

- i. Prove that the circuit in Figure-Q3(b)(ii) will produce  $I_S = V_{in}/R$ . [ 6 ]
- ii. Quantitatively determine the operation limit of the circuit in Figure-Q3(b)(ii). [ 5 ]

## Question 4

- a. i. Explain the reason for a circuit designer to opt for a second order filter instead of a first order, despite its circuit complexity. [ 3 ]
- ii. Explain the significant effect of Q-factor on a second order high pass filter when its value is swept from a fractional value to a value beyond unity. [ 3 ]
- iii. "A high quality radio tuner filter circuit has high selectivity." Explain this statement. [ 4 ]
- b. i. Draw a passive second order bandpass filter circuit, clearly showing the input and output terminals. [ 3 ]
- ii. Derive the Q-factor expression of the filter circuit drawn in part (b)(i). [ 5 ]
- c. Figure-Q4(c) shows the Sallen-Key active low pass filter. Quantitatively show that the filter circuit must not have  $R_A > 2R_B$ . [ 7 ]

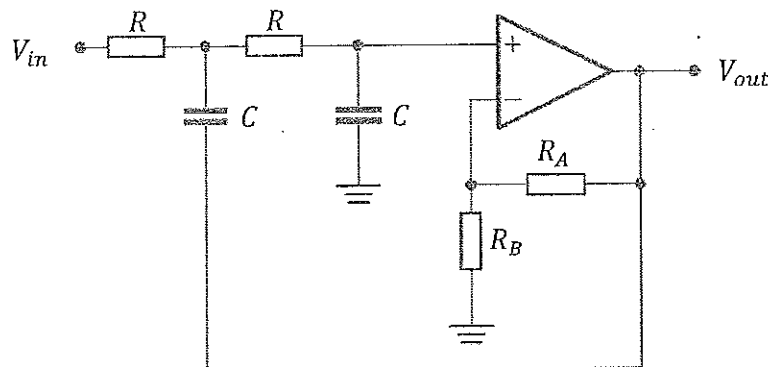


Figure-Q4(c)

Question 5

- a. i. Explain the function of a relaxation oscillator. [ 2 ]
- ii. Explain the importance of relaxation oscillator in a microcontroller circuit. [ 3 ]
- b. i. Explain the Barkhausen criterion of oscillation, which is widely used in harmonic oscillator design. [ 4 ]
- ii. Base on the Barkhausen criterion of oscillation, determine the required amplifier voltage gain value of an RC feedback oscillator if its frequency determining network has a voltage transfer function of  $0.2 \angle 180^\circ$ . [ 3 ]
- c. Figure-Q5(c)(i) shows a basic Wien Bridge Oscillator circuit in association with a filament lamp, while Figure-Q5(c)(ii) shows the non-linear resistance characteristics of the lamp in response to the voltage across it.

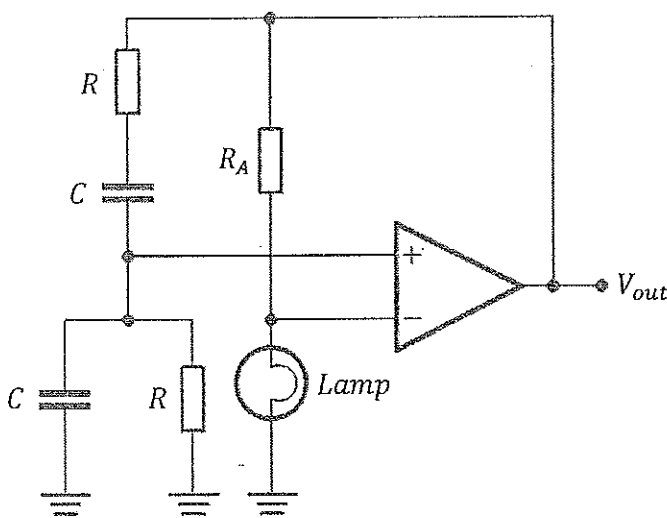


Figure-Q5(c)(i)

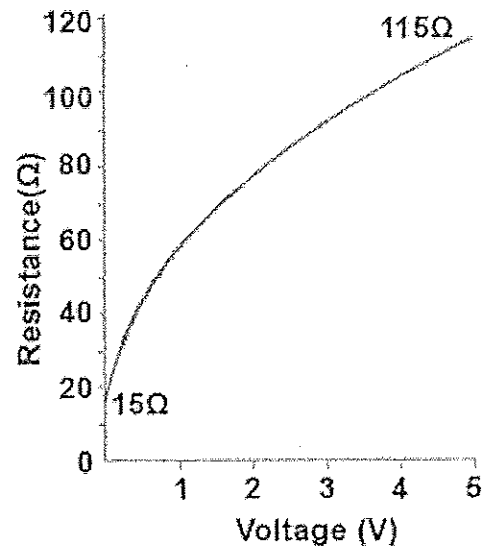


Figure-Q5(c)(ii)

- i. State the voltage gain expression of the amplifier circuit in the Wien Bridge Oscillator shown in Figure-Q5(c)(i). [ 3 ]
- ii. Explain how the resistance characteristic of the filament bulb helps to initiate and later sustain output signal oscillation. [ 6 ]

- iii. If  $R_A = 200 \Omega$ , estimate the output signal amplitude of the Wien Bridge Oscillator to sustain oscillation. Justify your answer. [4]

### Question 6

- a. Figure-Q6(a) shows the result of an experiment conducted on a second order low pass filter circuit. Base on the result obtained, express the transfer function of the filter circuit. [12]

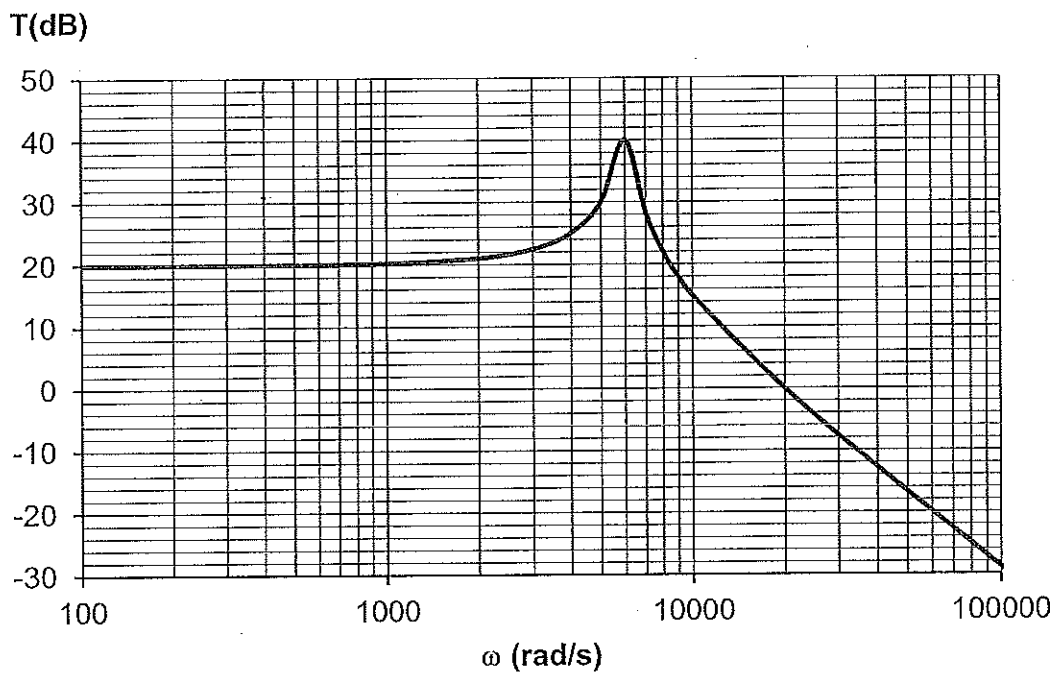


Figure-Q6(a)

- b. Figure-Q6(b) shows a difference amplifier (DA). DA has the ability to reject noise signals that appear as common-mode inputs to the circuit. If  $R_1 = R_3$  and  $R_2 = R_4$ , the output voltage of the DA can be expressed as,

$$V_{out} = \frac{R_2}{R_1} (V_2 - V_1)$$

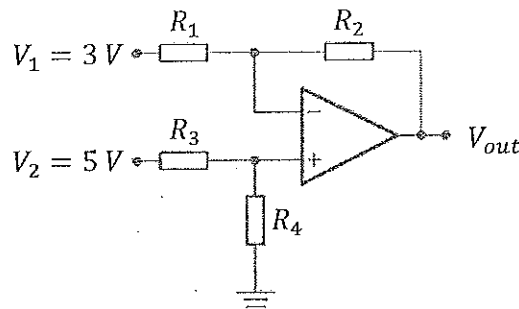


Figure-Q6(b)

- i. Determine the value of the common mode and differential mode input voltages of the DA respectively. [ 4 ]
- ii. Assume ideal op-amp operation, calculate the output voltage of the DA if  $R_1 = R_3 = 1\text{ k}\Omega$  and  $R_2 = R_4 = 3\text{ k}\Omega$ . [ 3 ]
- iii. If  $R_4$  is 0.5% less than its rated value in part (b)(ii), determine the common-mode output voltage value of the DA. [ 6 ]

~ The End ~