**INTI**INTERNATIONAL COLLEGE PENANG (507232-U)
LAUREATE INTERNATIONAL UNIVERSITIESFINAL
Examination Paper

(COVER PAGE)

Session : JAN 2014

Programme : DIPLOMA IN ELECTRICAL & ELECTRONIC ENGINEERING

Course : EEE2105: INTRODUCTION TO MICROPROCESSOR

Date of Examination : 12 March 2014

Time : 11:00am – 1:00pm Reading Time : Nil

Duration : 2 Hours

Special Instructions :

This paper consists of SIX (6) questions. Answer any FOUR (4) questions in the answer booklet provided. All questions carry equal marks.

Students are not allowed to remove the question papers from the examination venue.

Students are also not allowed to write anything on the Appendix handout given

Materials permitted :

Non-Programmable Scientific Calculator

Materials provided :

Appendix A (8086 Instruction Set Summary), Appendix B (ASCII Table)

Appendix C (8255 PPI), Appendix D (8253/8254 PIT), Appendix E (8259 PIC)

Examiner(s) :

Steven Khoo

Moderator :

Dr. Chen Li Choo

This paper consists of 9 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEE/I)

EEE2105: INTRODUCTION TO MICROPROCESSORS
FINAL EXAMINATION: JAN2014 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

- (a) Figure 1(a) shows a TM497GU8 Dynamic RAM Module pin configuration. Determine the memory capacity, memory organization, number of address pins and number of data pins.

(4 marks)

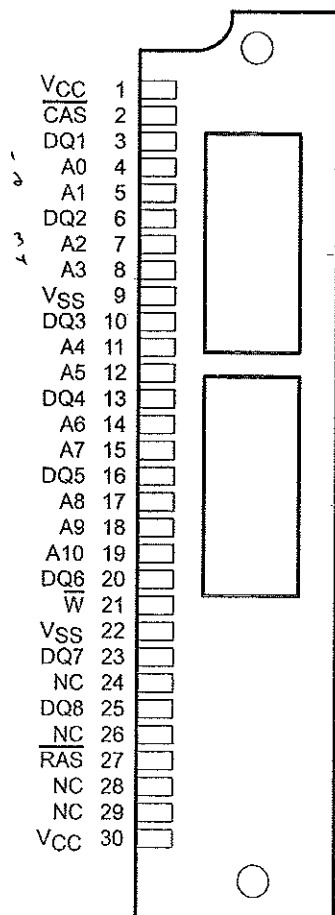


Figure 1(a) Pin configuration

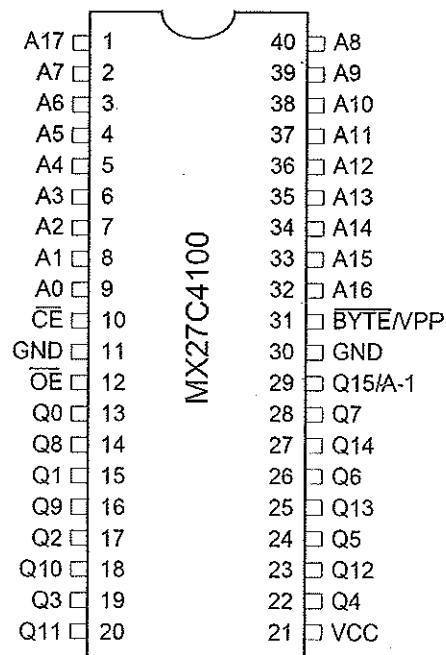


Figure 1(b) Pin configuration

- (b) Determine the memory capacity, number of address pins and number of data pins for MX27C4100 CMOS EPROM memory chip as shown in Figure 1(b).

(4 marks)

- (c) What is the result of $1010.1011_2 + CA.FE_{16} - 134.25_{10}$? Express the answer in octal equivalent number. (8 marks)
- (d) Explain the term of the following with an appropriate diagram.
 (i) Simplex
 (ii) Half-Duplex
 (iii) Full-Duplex (9 marks)

Question 2

- (a) Mention how the following instructions differ in their functionality.
 (i) NEG & NOT
 (ii) DIV & IDIV
 (iii) AND & TEST
 (iv) CMP & SUB (8 marks)
- (b) At a certain moment the state of an 8086 microprocessor based system is as follows: (All values are in Hexadecimal).

Registers											
	H		L								
AX	2C	15	CS	12	34	BP	90	9B			
BX	08	14	DS	34	45	SP	AB	CD			
CX	10	07	SS	56	78	SI	CD	EF			
DX	8B	26	ES	78	90	DI	00	12			

Table 2(b)(i) Registers.

Memory																
	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
5F800H	11	22	33	44	55	66	77	88	99	00	A1	B1	C1	D1	E1	F1
5F810H	02	04	45	78	90	11	22	33	44	55	66	77	88	99	00	12
5F820H	34	56	78	90	12	34	56	78	90	12	34	56	78	90	11	22
5F830H	33	44	55	66	77	88	99	00	00	00	12	34	56	78	9A	BC
5F840H	DE	F0	00	11	00	11	00	11	99	88	77	66	55	44	33	22
5F850H	00	FF	00	FF	00	FF	00	00	FF	FF	00	00	FF	FF	00	00

Table 2(b)(ii) Memory.

(i) Calculate the physical address of the memory where the operand is stored and the contents of the memory location for MOV [BP+DI-11+11H-110+11B], DX. Draw the affected memory locations and register. (6 marks)

(ii) Provide the registers and memory locations that are affected, and their new values after the execution of ADD [BP + 11H], AX, also state the number of bytes used for this instruction. (5 marks)

(c) Explain the functions of the following:

- (i) Debugger
- (ii) Assembler
- (iii) Linker

(6 marks)

Question 3

(a) Calculate the time delay taken for Program Q3(a) running on 8086 microprocessor at 5MHz. Show all workings clearly for each instruction. What is the final result stored in register AX?

(13 marks)

Program		
	MOV	AX, 01H
	MOV	CX, 03H
LOOP1:	NOP	
	LOOP	LOOP1
	DEC	AX
	JZ	LOOP2
	ADD	AX, AX
LOOP2:	DEC	AX
	HLT	

Program Q3(a) Coding.

[Refer to APPENDIX A for the cycle time]

(b) Referring to Program Q3(a), the equivalent machine code for JZ LOOP2 is 74 02. If JZ operation code is 75, explain how the LOOP2 is equivalent to 02. Justify your answer with the aid of diagram. Show all workings clearly.

(4 marks)

[Refer to APPENDIX A for the bytes count]

- (c) Explain the following instructions in 8086 with example and their effect on flag:
- (i) CWD
 - (ii) SAR
 - (iii) LOOP
 - (iv) IMUL
- (8 marks)
- [Refer to APPENDIX A for the instruction]

Question 4

- (a) The 8255 PPI is configured as shown in Figure 4(a).
- (i) Find the port addresses and control register. Thus, program the PPI to reset PC2 to low. Also include comments for any instruction used. (5 marks)
 - (ii) Write a program to test the incoming data from port B continuously via 8255 PPI. If the data is odd number, send 38H to port A but if the data is even number, send 83H to port C. Also, include comments for any instruction used.

Examples of incoming data and the respective action:

- 25_H (Odd number) ⇒ send 38_H out to port A
- 52_H (Even number) ⇒ send 83_H out to port C
- C1_H (Odd number) ⇒ send 38_H out to port A
- B6_H (Even number) ⇒ send 83_H out to port C

ODD send 38H to A
Even send 83H to C

(8 marks)

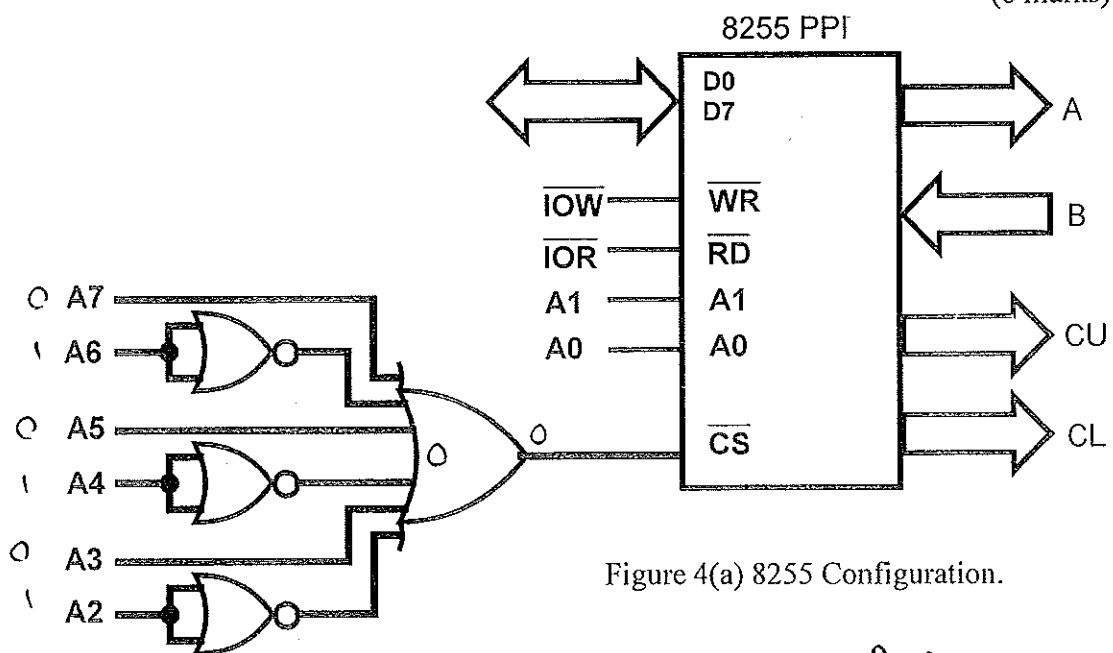


Figure 4(a) 8255 Configuration.

[Refer to Appendix C for 8255 PPI Control Word]

M A A A C B B C
M M M M M M M M

~~1 0 0 0 0 0 1 0~~

~~4 3 H~~

1 0 0 0 / 0 0 1 0

(b) The 8259 PIC is configured as shown in Figure 4(b).

(i) Find the ICWs of the 8259 if it is used with an 8088/86 microprocessor, single, edge triggering IRs, and IR0 is assigned "INT 28H". The 8259 is in master buffered mode with normal EOI and not nested. (6 marks)

(ii) Write a program to initialize the 8259 using the port addresses in Figure 4(b). Also include comments for any instruction used. (6 marks)

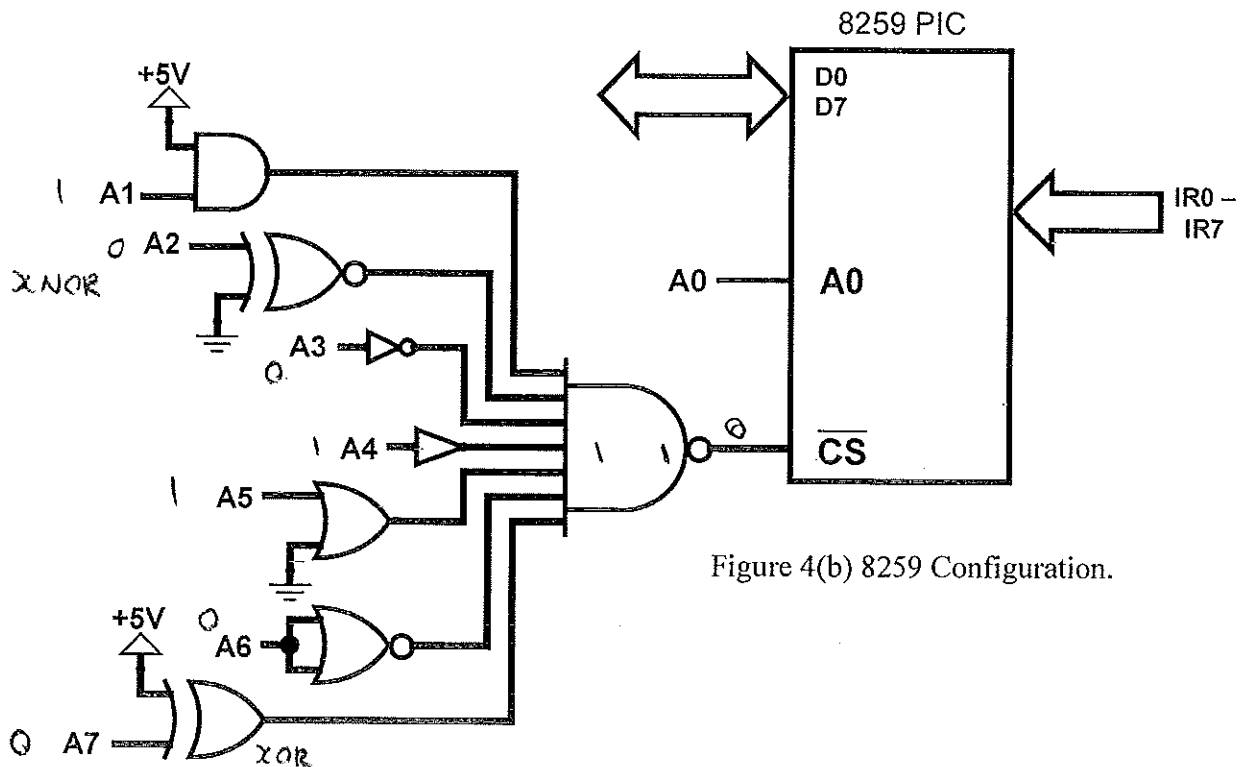


Figure 4(b) 8259 Configuration.

[Refer to Appendix E for 8259 PIC Control Words]

Question 5

(a) Pin \overline{CS} of a given 8237 DMA is activated by binary address $A7 - A4 = 0110$. Find the port addresses assigned to the four channels. Write a program using channel 1 memory address and count registers to transfer 2K starting from offset 3456H using the port address obtained. (5 marks)

Handwritten marks: \overline{CS} and a vertical line.

- (b) A transmission system uses asynchronous serial data communication as shown in Figure 5(b) with LSB being transmitted first to transmit a passkey to the receiver.

Bits per second: 14400

Data bits: 7

Parity: Space

Stop bits: 2

Flow control: None

Figure 5(b) Serial communication settings.

Decode the following serial data received in continuous ASCII characters message:

Incoming data:

00000101011000000010110101011001101010110011011101110110000011001110010010101011000100110111

What is the passkey transmitted?

Also, calculate the total time wasted due to overhead when transmitting the above message. [Refer to Appendix B for ASCII codes].

(15 marks)

- (c) Table Q5(c) below shows the data and the offset addresses of the data segment in memory. Based on the table below, find the values stored in AL and BL after execution of the following sequence of instructions. Also, show the final result and the location where it is stored. All values are in Hexadecimal.

Data	Offset Address
45	DS:2000H
96	DS:2001H
51	DS:2002H
A7	DS:2003H
5D	DS:2004H
B4	DS:2005H
FC	DS:2006H
EF	DS:2007H
A3	DS:2008H
27	DS:2009H

Table Q5(c) Memory.

Program	
MOV	DI, 1FFFH
MOV	AL, [DI+5]
MOV	SI, 2007H
MOV	BL, [SI]
ADD	AL, BL
INC	SI
ADD	AL, [SI]
MOV	[DI], AL

Program Q5(c) Coding.

(5 marks)

Question 6

- (a) Design an address decoding for the following memory mapping shown in Figure 6(a)(i) using given decoder and any suitable logic gate(s) into the implementation. The designed circuit should be showing memory chips, microprocessor, buses and Read or Write connections. All memory chips are active low. Decoder (74LS138) information is as shown below.

(15 marks)

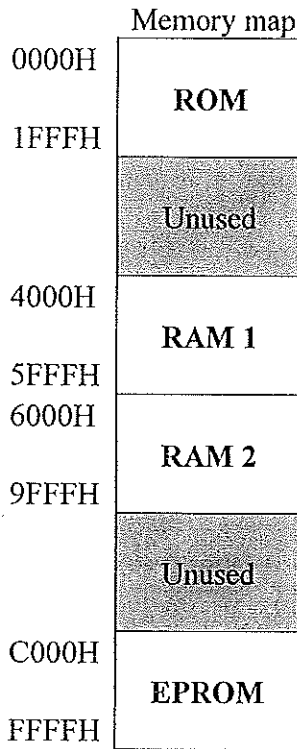


Figure 6(a)(i) Memory map

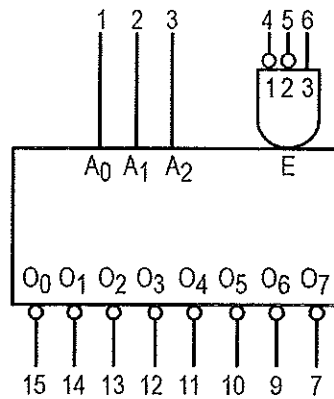


Figure 6(a)(ii) Decoder: Logic symbol

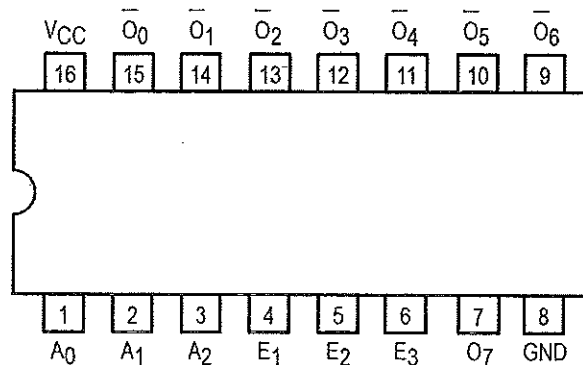


Figure 6(a)(iii) Decoder: Pin Configuration

Table 6(a) Decoder: Truth Table

INPUTS						OUTPUTS							
E ₁	E ₂	E ₃	A ₀	A ₁	A ₂	O ₀	O ₁	O ₂	O ₃	O ₄	O ₅	O ₆	O ₇
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care

- (b) The 8254 PIT chip is configured as shown in Figure 6(b).
- (i) Find the port address assigned to all the counters and the control register. (2 marks)
 - (ii) CLK0 of counter 1 is 1.193MHz and Gate1 is connected to high permanently. Counter 0 uses a square wave to trigger the 8259 interrupt controller to provide time-of-day interrupt. Write assembly instructions to divide this counter by 65,536. What is the OUT1 frequency? (4 marks)
 - (iii) CLK1 of counter 2 is 1.193MHz and Gate2 is connected to high permanently. Counter 2 generates a periodic pulse every 15.088 μ s to refresh DRAM memory. Write assembly instructions to generate this periodic pulse through OUT2. (4 marks)

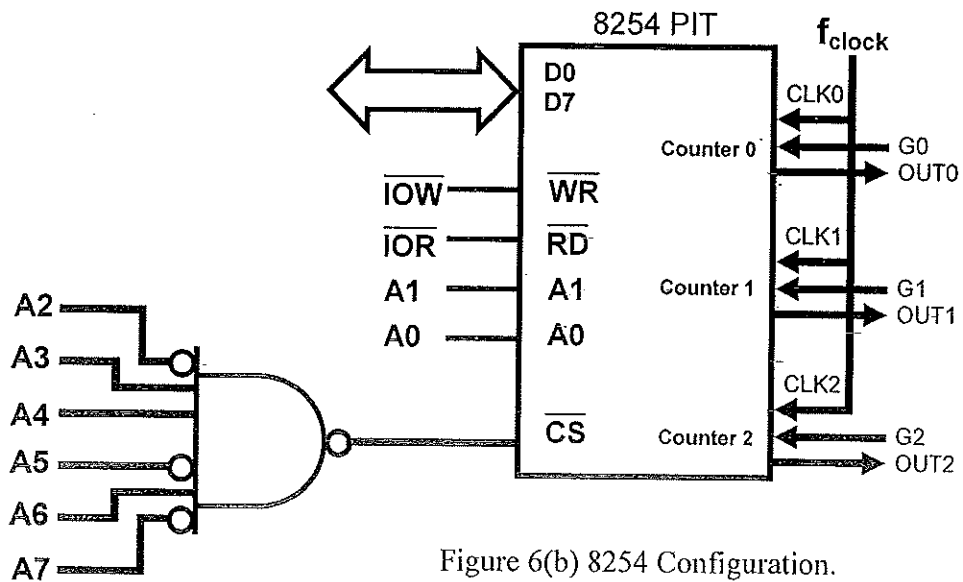


Figure 6(b) 8254 Configuration.

[Refer to Appendix D for 8253/8254 PIT Control Word]

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