INTI
INTERNATIONAL COLLEGE PENANG (507232-U)
LAUREATE INTERNATIONAL UNIVERSITIES

FINAL
Examination Paper

(COVER PAGE)

Session	:	Janauary 2014
Programme	:	DIPLOMA IN ELECTRICAL & ELECTRONIC ENGINEERING
Course	:	EEE2101: INTRODUCTION TO DIGITAL ELECTRONICS
Date of Examination	:	14 March 2014
Time	:	08:00am – 10:00am Reading Time : Nil
Duration	:	2 Hours
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Students are not allowed to remove the question papers from the examination venue.

Materials permitted :

Non-Programmable Scientific Calculator

Materials provided :

Graph Paper (A4 size)

Examiner(s) : **Steven Khoo**

Moderator : **Dr. Chen Li Choo**

This paper consists of 10 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEE/I)

EEE2101: INTRODUCTION TO DIGITAL ELECTRONICS
FINAL EXAMINATION: JAN2014 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

(a) Perform the following number system transformation. Show all workings clearly.

i) 1010.1011_2 to hexadecimal equivalent.

(3 marks)

ii) 134.25_{10} to binary equivalent.

(3 marks)

iii) $CA.FE_{16}$ to decimal equivalent.

(3 marks)

(b) What is the result of $1010.1011_2 + CA.FE_{16} - 134.25_{10}$? Express the answer in octal equivalent number.

(6 marks)

(c) Determine the input condition needed to produce Z = 0 in Figure 1(c) below.

(5 marks)

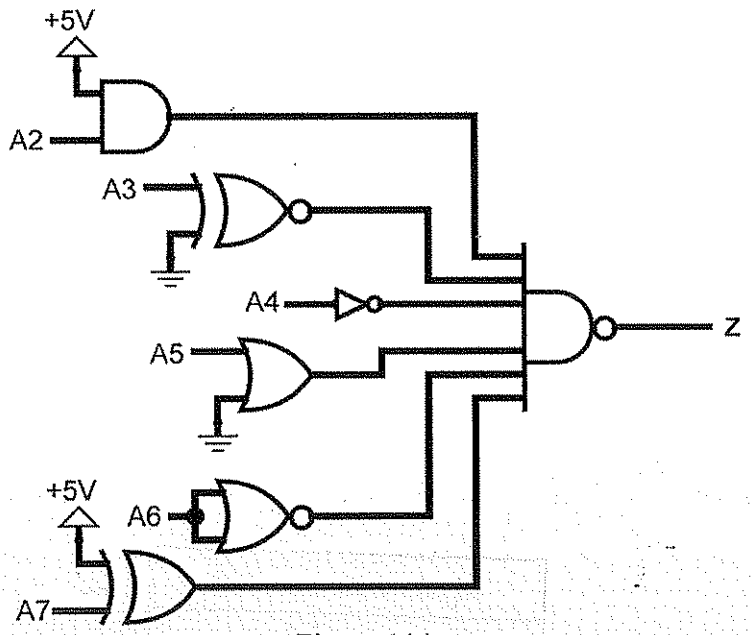

Figure 1(c)

(d) What is the 2's complement number of -6.625_{10} in signed numbering system? Show the calculation working clearly.

(5 marks)

Question 2

(a) Use Boolean algebra to:

i) Simplify the expression, $x = (\bar{A} + B)(A + B + D)\bar{D}$ to the simplest form.

(4 marks)

ii) Simplify the expression, $y = \bar{A}C(\overline{\bar{A}BD}) + \bar{A}B\bar{C}\bar{D} + A\bar{B}C$ to the simplest form.

(4 marks)

iii) Simplify the logic circuit shown in Figure 2(a)(iii) below to the simplest form.

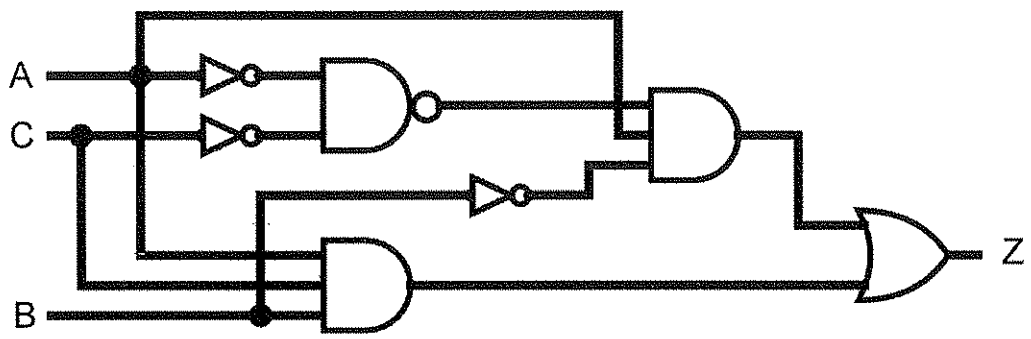

Figure 2(a)(iii)

(5 marks)

iv) Simplify the output, S as shown below in Table 2(a)(iv) to the simplest form.

Inputs			Output
X	Y	C	S
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Table 2(a)(iv)

(4 marks)

(b) Determine the input conditions needed to cause the output in Figure 2(b) to go to its active state, X = 1.

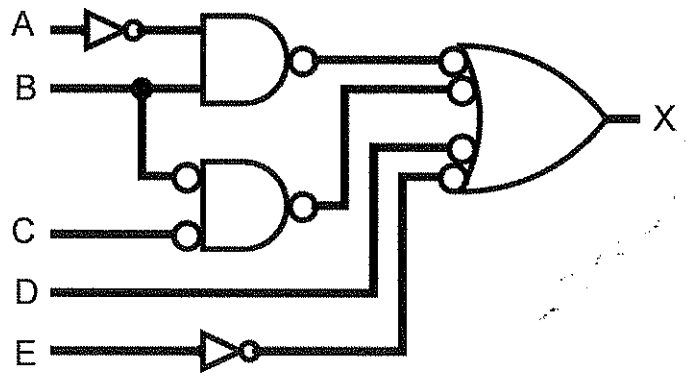

Figure 2(b)

(4 marks)

(c) A jet aircraft employs a system for monitoring the rpm, pressure, and temperature values of its engines using sensors that operate as follows:

RPM sensor output = 0 only when speed < 4800 rpm
P sensors output = 0 only when pressure < 220 psi
T sensor output = 0 only when temperature < 200°F

Figure 2(c) shows the logic circuit that controls a cockpit warning light for certain combinations of engine conditions. Assume that a HIGH at output, W activates the warning light.

i) Determine what engine conditions will give a warning to the pilot.
ii) Change this circuit to one using only SN7400N (2-input NAND gates) with minimum number of gate count.

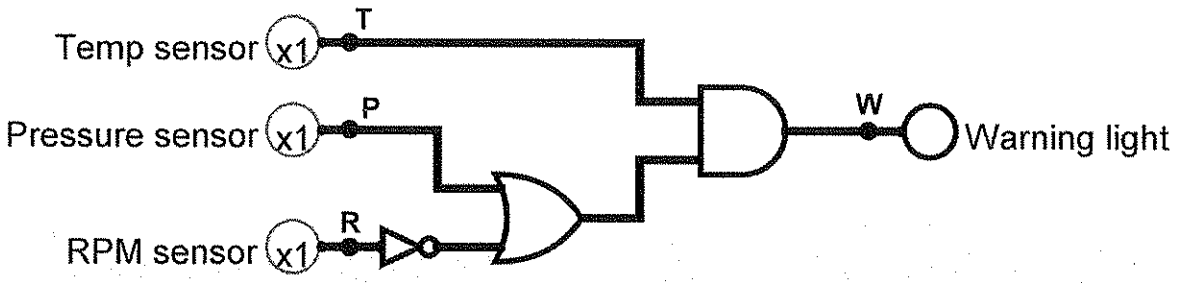

Figure 2(c)

(4 marks)

Question 3

(a) With the aid of diagram, differentiate between:

i) latch and flip-flop?

(2 marks)

ii) Mealy and Moore state machine?

(3 marks)

(b) Use Karnaugh map method to obtain the minimum

i) SOP expression for the function, $F(K,L,M,N)=\prod(2,6,8,9,10,11,14)$.

(4 marks)

ii) POS expression for the function, $F(W,X,Y,Z)=\sum(4,5,6,7,12)$.

(4 marks)

iii) SOP expression for the function, $F=\overline{A}\cdot\overline{B}\cdot D+\overline{A}\cdot C\cdot D+A\cdot C\cdot D$ with don't care conditions; $\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}$, $\overline{A}\cdot\overline{B}\cdot C\cdot\overline{D}$ and $\overline{A}\cdot B\cdot\overline{C}\cdot D$.

(4 marks)

(c) Figure 3(c) shows four switches that are part of the control circuitry in a copy machine. The switches are at various points along the path of the copy paper as the paper passes through the machine. Each switch is normally open, and as the paper passes over a switch, the switch closes. It is impossible for switches SW1 and SW4 to be closed at the same time. Design the logic circuit to produce a HIGH output whenever two or more switches are closed at the same time. Use Karnaugh mapping and take advantage of the don't care conditions.

(8 marks)

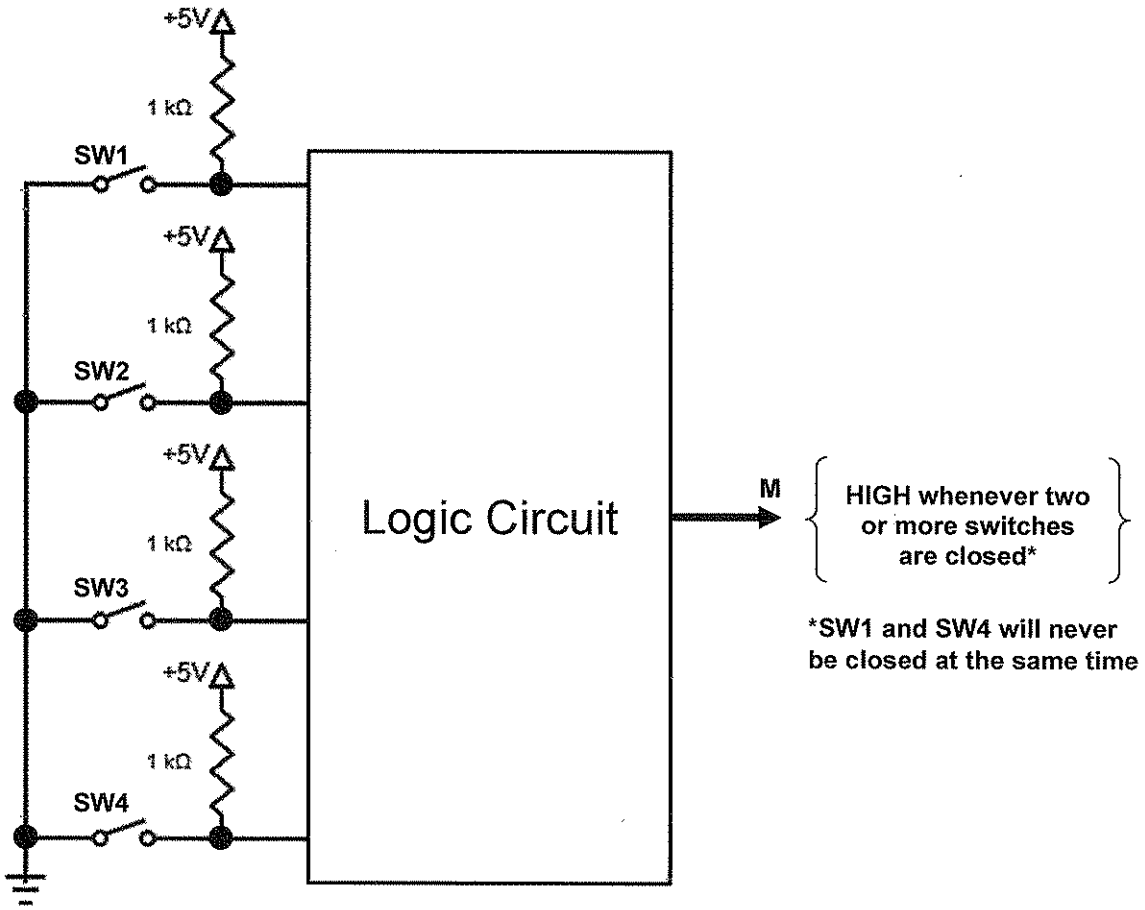

Figure 3(c)

Question 4

(a) Design a synchronous 3-bit up/down counter using positive edge-triggered T flip-flop for MSB, D flip-flop for second bit and JK flip-flop for LSB. Assume all unused states as don't care. Input Z will be used as the up/down control. The counter will count from 0 ⇨ 1 ⇨ 2 ⇨ 3 ⇨ 4 ⇨ 5 ⇨ 6 ⇨ 7 ⇨ 0 for count up when input, Z = 0 and 7 ⇨ 6 ⇨ 5 ⇨ 4 ⇨ 3 ⇨ 2 ⇨ 1 ⇨ 0 ⇨ 7 for counting down when input, Z = 1. Provide proper labelling for the designed logic circuit. Show all workings clearly including all excitation tables used. Also, provide the state diagram with up/down conditions.

(17 marks)

(b) Table 4(b) shows a portion of quadruple 2-input NAND gates (SN74ALS00A) datasheet. Determine the following parameters from this datasheet, show all working clearly:

i) Fan-out, a gate can safely drive.

(3 marks)

ii) Average Power dissipation, $P_{D(avg)}$ for one gate on a 74ALS00 IC.

(3 marks)

iii) Propagation delay, t_{PD}.

(2 marks)

recommended operating conditions

		SN54ALS00A			SN74ALS00A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8‡			0.8	V
				0.7§				
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

‡ Applies over temperature range −55°C to 70°C
§ Applies over temperature range 70°C to 125°C

electrical characteristics over recommended operating free-air temperature range unless otherwise noted

PARAMETER	TEST CONDITIONS		SN54ALS00A			SN74ALS00A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} −2			V_{CC} −2			V
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−20		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0		0.5	0.85		0.5	0.85	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.5	3		1.5	3	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§				UNIT
			SN54ALS00A		SN74ALS00A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	3	15	3	11	ns
t_{PHL}			2	9	2	8	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

Table 4(b)

Question 5

(a) An 10-bit DAC produces an output current in proportion to its digital input. For a digital input of 0000101000, an output current of 20mA is produced.

i) What will the output current be if the digital input is 1000111101?

(3 marks)

ii) What is the maximum output current produced by this DAC?

(3 marks)

iii) What should the digital input be if a 205mA output current is required?

(3 marks)

(b) Table 5(b) show a typical TTL series characteristics. Determine the noise margins when a 74LS device is driving a 74ALS input and when a 74ALS device is driving a 74LS input.

(4 marks)

What will be the overall noise margin of a logic circuit that uses 74LS and 74ALS circuits?

(2 marks)

A logic circuit has $V_{IL}(max) = 450mV$. Which TTL series can be used?

(2 marks)

	74	74S	74LS	74AS	74ALS	74F
Performance ratings						
Propagation delay (ns)	9	3	9.5	1.7	4	3
Power dissipation (mW)	10	20	2	8	1.2	6
Max. clock rate (MHz)	35	125	45	200	70	100
Fan-out (same series)	10	20	20	40	20	33
Voltage parameters						
$V_{OH}(min)$	2.4	2.7	2.7	2.7	2.7	2.7
$V_{OL}(max)$	0.4	0.5	0.5	0.5	0.5	0.5
$V_{IH}(min)$	2.0	2.0	2.0	2.0	2.0	2.0
$V_{IL}(Max)$	0.8	0.8	0.8	0.8	0.8	0.8

Table 5(b)

(c) Given a waveform shown in Figure Q5(c). If the waveform is applied to a sampling circuit and it is sampled every 3ms, determine the following:

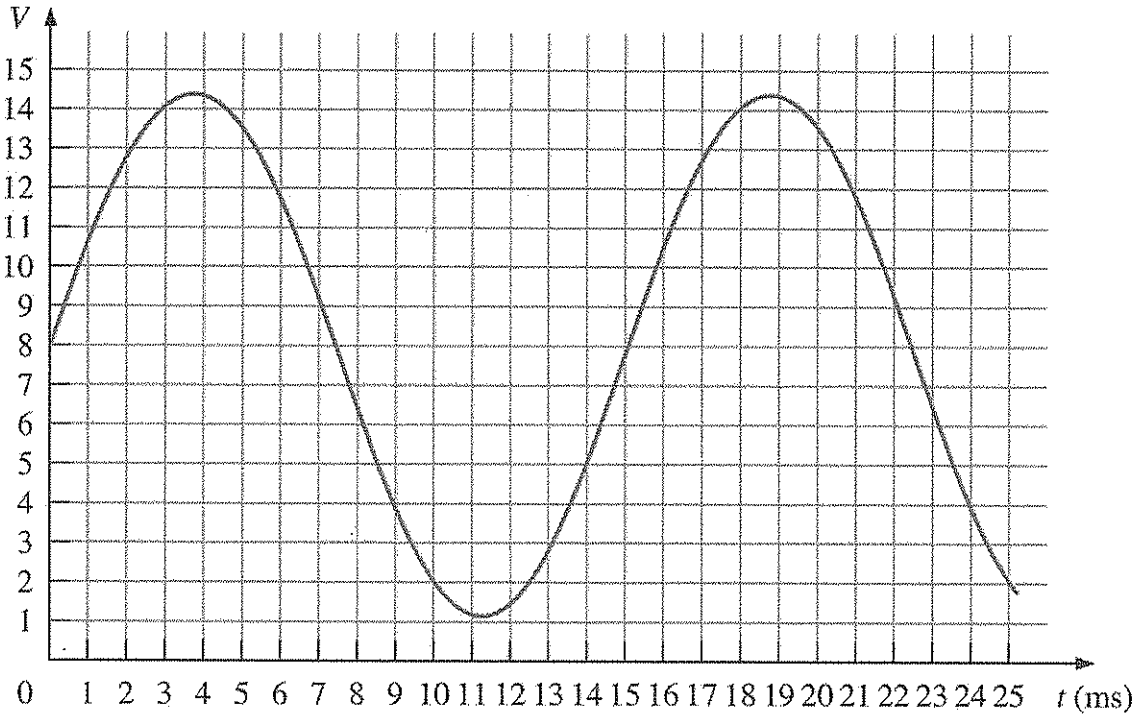

Figure Q5(c)

i) Draw the output of the sampling circuit. Assume a one-to-one voltage correspondence between the input and output.

(4 marks)

ii) If the output in part (i) is applied to a hold circuit, draw the output of the hold circuit.

(4 marks)

Question 6

a) Implement F(x,y,z) = Σ(1,2,6,7) using the following in the simplest form:

i) SN7408N (2-input AND gate), SN74ALS32N (2-input OR gate) and SN74ALS04BN (NOT gate).

(4 marks)

ii) SN7402N (2-input NOR gate) only.

(4 marks)

iii) SN74157N (2-to-1 Multiplexer) with x as select line and other logic gate(s).

(4 marks)

iv) SN74LS138N (3-to-8 Decoder) and other logic gate(s).

Inputs				Outputs							
E	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	X	X	X	1	1	1	1	1	1	1	1
1	0	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	0	1	1	1	1	1	1
1	0	1	0	1	1	0	1	1	1	1	1
1	0	1	1	1	1	1	0	1	1	1	1
1	1	0	0	1	1	1	1	0	1	1	1
1	1	0	1	1	1	1	1	1	0	1	1
1	1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	0

(4 marks)

b) Refer to Figure 6(b) where an analog-to-digital converter is monitoring the dc voltage of a 15V storage battery on an orbiting spaceship. The converter's output is a 4-bit binary number, RSTU, corresponding to the battery voltage in steps of 1V, with R as the MSB. The converter's binary outputs are fed to a logic circuit that is to produce a HIGH output as long as the binary value is greater than $0110_2 = 6_{10}$; that is, the battery voltage greater than 6V. Design this logic circuit using only SN7400N (2-input NAND gates) with minimum number of gate count. Also, provide a truth table. Show all working steps.

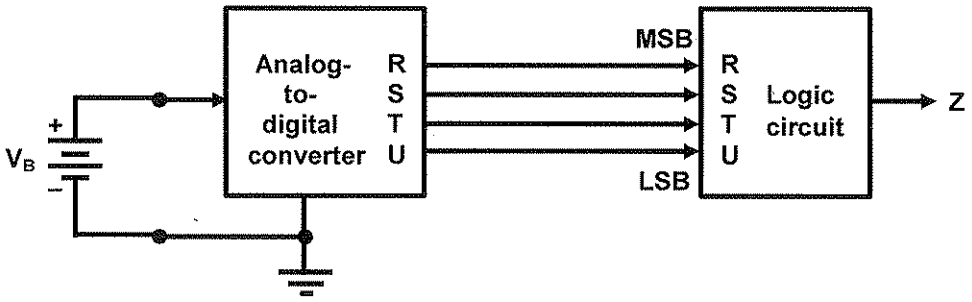

Figure 6(b)

(9 marks)

– THE END –

EEE2101(F)/Jan14/Steven Khoo/11/12/13