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FINAL
Examination Paper

(COVER PAGE)

Session	:	JANUARY 2014
Programmes	:	Diploma in Electrical and Electronic Engineering (DEEI)
Course	:	**ELECTRONIC DEVICES AND CIRCUIT THEORY 2 (EEE1103)**
Date of Examination	:	12 March 2014
Time	:	8.00am – 10.00am Reading Time: Nil
Duration	:	2 Hours
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Students are not allowed to remove this question paper from the examination venue.

Materials permitted : Non-programmable scientific calculator

Materials provided: **Worksheet for Q3(b)**

Examiner(s)	:	**Chan Tse Wei**
Moderator	:	**Dr. Ooi Beng Lee**

This paper consists of 10 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)

EEE1103 : ELECTRONIC DEVICES AND CIRCUIT THEORY 2
FINAL EXAMINATION : JANUARY 2014 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks. The marks allocated to each sub-question are shown in square brackets at the right-hand margin.

Question 1

a. i. A power amplifier delivers a peak-to-peak voltage swing of 12V across an 8Ω load. Determine the AC power delivered to the load. [3]

ii. If the input power drawn by the power amplifier in part (a)(i) is 8W, determine the power efficiency of the amplifier. [3]

b. i. State the limiting factor that forbids an op-amp-based non-inverting amplifier to drive a low impedance load such as an 8Ω speaker. [2]

ii. Figure-Q1(b) shows a solution to the problem in part (b)(i). State the type of amplifier that is used to drive the load. [2]

iii. Components R_1, R_2, D_1 and D_2 are there to provide a small amount of biasing to the two transistors Q_1 and Q_2. Explain why it is necessary for such an arrangement. [2]

iv. Explain how resistors R_3 and R_4 help to improve thermal stability of the circuit. [4]

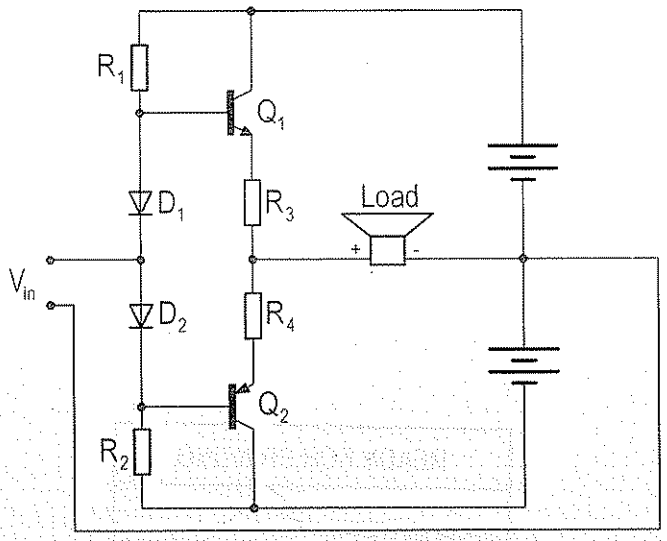

Figure-Q1(b)

c. Figure-Q1(c) shows an improved version of the circuit in Figure-Q1(b).

i. Explain how crossover distortion can be eliminated with such a configuration. [3]

ii. If $R_2 = 27k\Omega$ and $R_3 = 3k\Omega$, calculate the expected voltage across the load when a 0.2V peak-to-peak sinusoidal voltage is applied at the input. [3]

iii. State two advantages of the circuit configuration in Figure-Q1(c) as compared to the one in Figure-Q1(b) in terms electrical characteristic. [3]

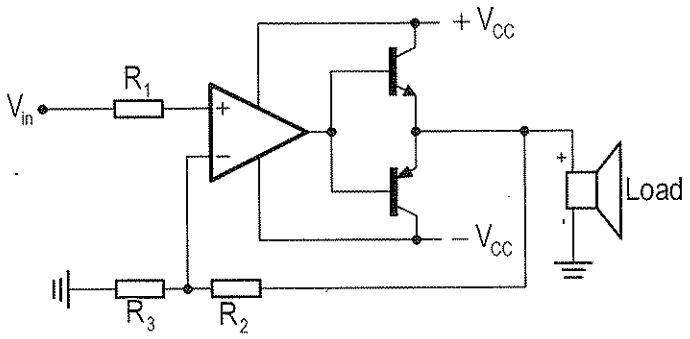

Figure-Q1(c)

Question 2

a. Figure-Q2(a) shows an AC circuit model of a single supply rail capacitive-coupled amplifier

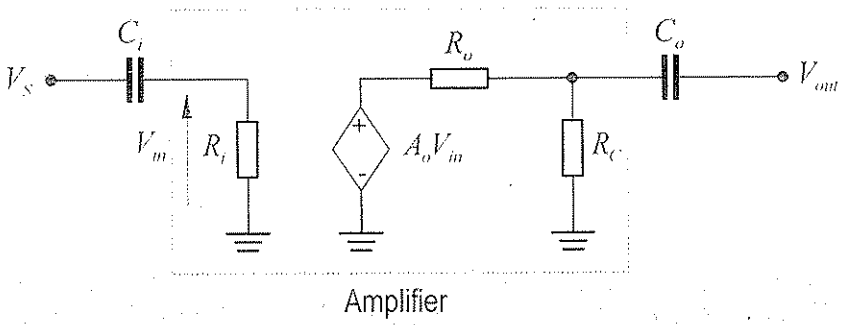

Figure-Q2(a)

i. State the function of the capacitors used in the circuit. [3]

ii. State one major limitation of this type of amplifier. [2]

iii. If the input frequency is below the mid-band frequency range, explain the behavior of the input RC network formed by C_i and R_i. [3]

iv. Draw the model of the circuit in Figure-Q2(a) at both mid-band and high-band frequency range. [3]

v. If a low resistance load is connected across the output terminal of the amplifier in Figure-Q2(a) and ground, how would it affect the frequency response of the amplifier? [3]

b. Figure Q2(b)(i) shows a FET based amplifier circuit. At the operating quiescent point, transistor Q_1 has a transconductance of 2mS.

The mid-band and low-band frequency response of the amplifier is shown in Figure-Q2(b)(ii). The corner frequencies, f_{C1}, f_{C2} and f_{C3} are contributed by capacitors C_G, C_D and C_S respectively.

i. Draw the low frequency band AC circuit equivalent circuit for the amplifier. [2]

ii. Determine the capacitance value for capacitor C_S [4]

iii. Determine the capacitance value for capacitor C_G [3]

iv. Determine the capacitance value for capacitor C_D [2]

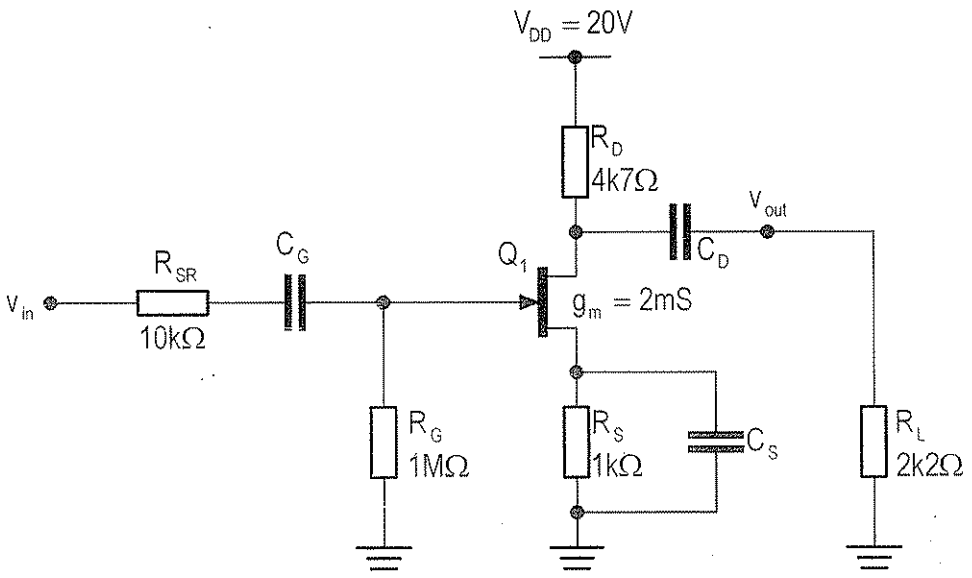

Figure-Q2(b)(i)

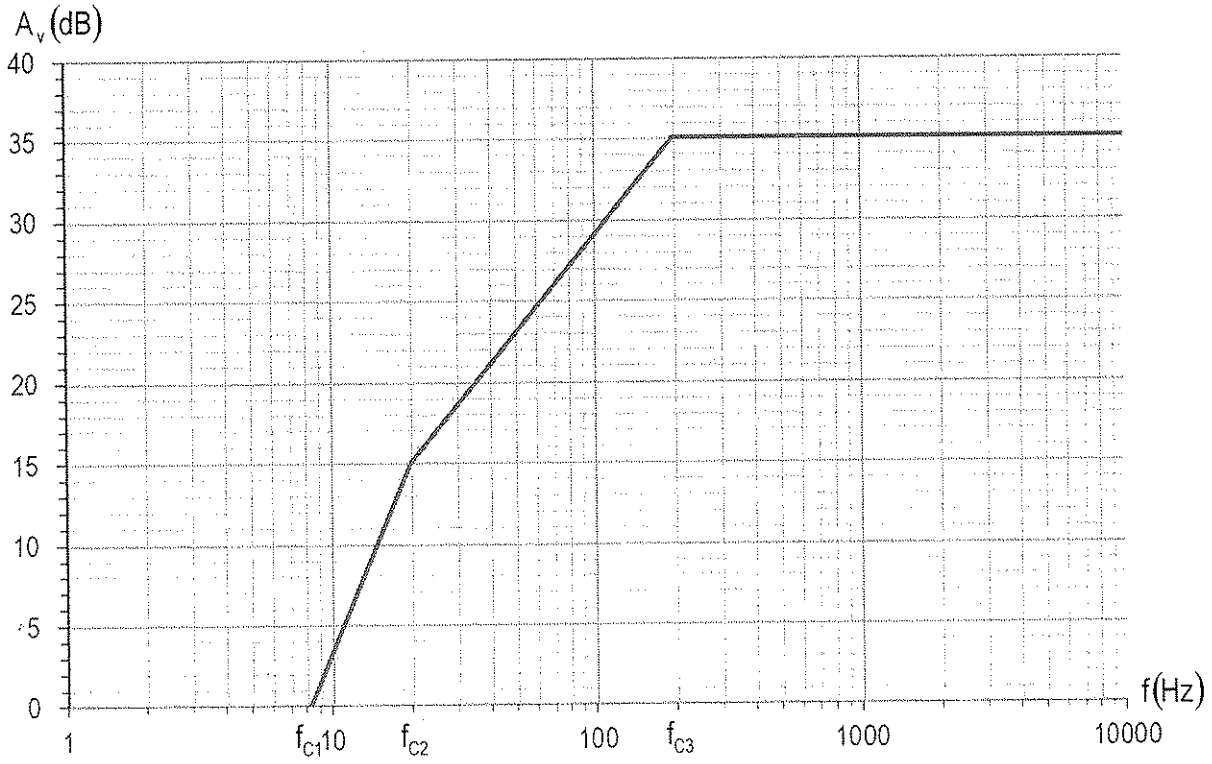

Figure-Q2(b)(ii)

Question 3

a. State the ideal value for the following op-amp characteristics:

i. Open-loop gain [1]

ii. Drift [1]

iii. Bandwidth [1]

iv. Input Impedance [1]

v. Output Impedance [1]

b. Make use of the given worksheet for this question, sketch the output voltage (V_{out}) timing diagram for the circuit shown in Figure-Q3(b). The input voltage V_{in} is as shown in the accompanied worksheet and assume ideal op-amp operation. [5]

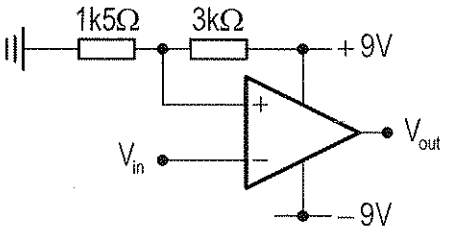

Figure-Q3(b)

c. i. Explain "slew rate" of an op-amp. [2]

ii. When a pulse is applied to an op-amp and its output voltage goes from −7V to +8V in 0.6μs, what is the slew rate of the op-amp? [3]

d. Figure-Q3(d) shows a non-inverting amplifier. The op-amp has the following characteristics:

Open-loop voltage gain = 90dB

Output impedance = 60Ω

Input impedance = 200MΩ

Derive the output impedance expression of the amplifier circuit seen from the output terminal and show that with negative feedback, the output impedance of the amplifier is very much less than the internal output impedance of the op-amp itself. [10]

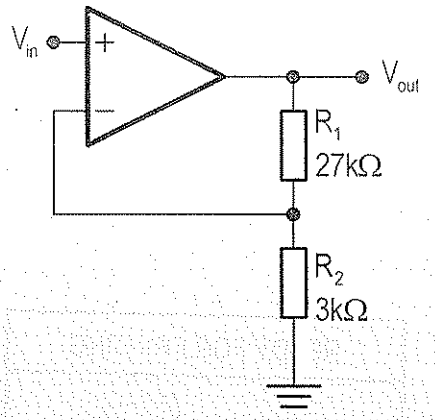

Figure-Q3(d)

Question 4

a. i. How are the Q-factor and the bandwidth of a band-pass filter related? [2]

ii. Explain how the selectivity of a band-pass filter is affected by the Q-factor. [2]

iii. What is the main purpose of cascading two low pass filters? [2]

b. i. Identify the type of filter implemented by the circuit in Figure-Q4(b). [2]

ii. Explain why the frequency response of the filter does not exhibit peaking. [5]

iii. Determine the maximum gain of the filter at pass-band frequency range. [2]

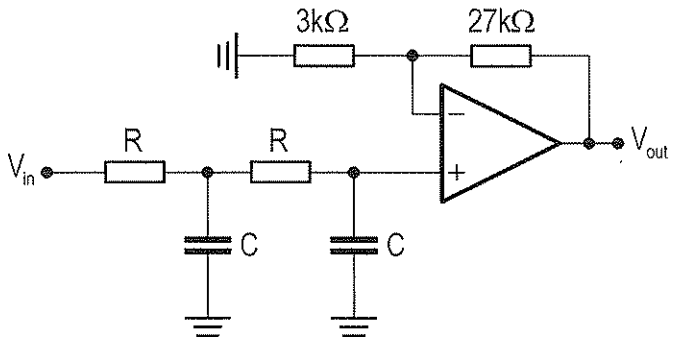

Figure-Q4(b)

c. i. Show that the voltage transfer function of the circuit in Figure-Q4(c) can be expressed as,

$$\frac{V_{out}}{V_{in}} = \frac{(K/CR)s}{s^2 + \frac{3-K}{CR}s + \frac{1}{C^2R^2}}$$, where $K = \frac{R_2}{R_1} + 1$ is the circuit gain value. [5]

ii. Hence identify the filter implemented by the circuit in Figure-Q4(c). [1]

iii. State one advantage of the circuit in terms of determining the Q-factor. [2]

iv. State one disadvantage of the circuit in terms of varying the gain value K. [2]

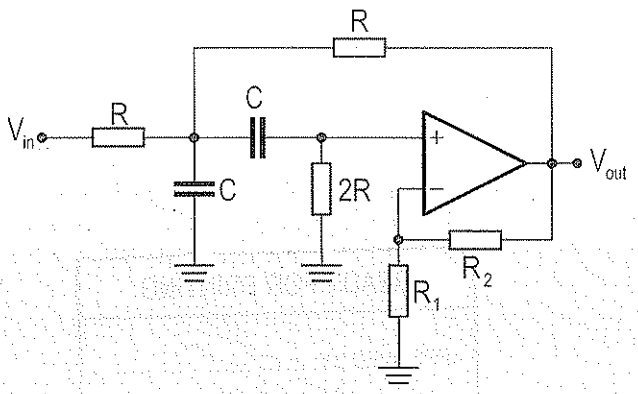

Figure-Q4(c)

Question 5

a. i. What type of input is required for an oscillator? [2]

ii. What are the basic circuit configurations of a feedback oscillator? [4]

b. Figure-Q5(b) shows a Wien Bridge oscillator circuit.

i. State the factor that limits the value of the circuit's oscillation frequency [2]

ii. State the main function of the two diodes in the circuit. [2]

iii. State the expression for the circuit's oscillation frequency in Hertz. [2]

iv. If $R_2 = 0.1R_1$ and $C_2 = 2C_1$, suggest appropriate values for R_1, R_2, C_1 and C_2 so that the oscillator produces a sinusoidal wave of 1kHz. [4]

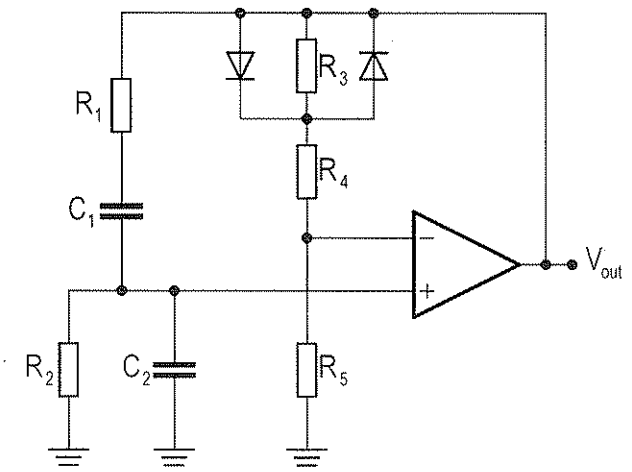

Figure-Q5(b)

c. i. Briefly explain the operation of the circuit in Figure-Q5(c). [4]

ii. Sketch the timing diagrams for V_a, V_b and V_{out} of the circuit in Figure-Q5(c) on common time axes. [6]

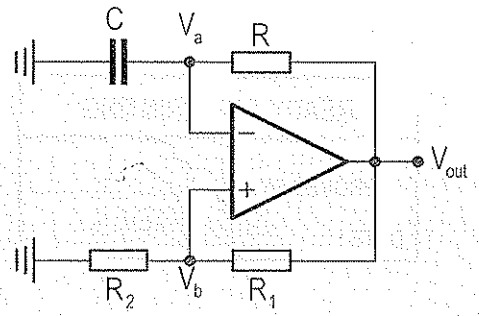

Figure-Q5(c)

Question 6

a. Figure-Q6(a) shows a voltage regulator circuit. Transistor Q_1 has a current gain, $\beta = 200$ and its B-E junction barrier voltage is 0.6V.

i. Identify the type of voltage regulator implemented. [2]

ii. State one major drawback of the voltage regulator. [2]

iii. State the function of zener diode D_1 [2]

iv. If 10V is to be regulated across resistor R_L, calculate the required resistance for R_S and the zener voltage for D_1, assume that the nominal current for the zener diode is 20mA. [6]

v. If 0.25W power rating is chosen for resistor R_S in the design in part (a)(iv), determine the smallest load resistance R_L that can be connected. Assume that transistor Q_1 does not saturate and the zener current remain unchanged. [4]

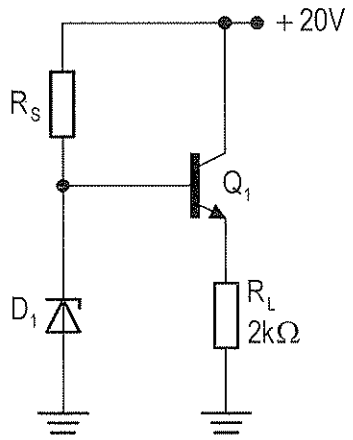

Figure-Q6(a)

b. Figure-Q6(b) shows extracts of the LM78L05 voltage regulator datasheet.

i. Determine the maximum dropout voltage of the device. [3]

ii. Determine the lowest resistance that can be connected across the device output terminal. [3]

iii. An inconsistent load draws current from the regulator ranging between 10mA to 40mA, determine the worst case output voltage of the regulator. [3]

LM78L05

Unless otherwise specified, V_{IN} = 10V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_O	Output Voltage		4.8	5	5.2	V
		7V ≤ V_{IN} ≤ 20V 1mA ≤ I_O ≤ 40mA (Note 3)	4.75		5.25	
		1mA ≤ I_O ≤ 70mA (Note 3)	4.75		5.25	
ΔV_O	Line Regulation	7V ≤ V_{IN} ≤ 20V		18	75	mV
		8V ≤ V_{IN} ≤ 20V		10	54	
ΔV_O	Load Regulation	1mA ≤ I_O ≤ 100mA		20	60	
		1mA ≤ I_O ≤ 40mA		5	30	
I_Q	Quiescent Current			3	5	mA
ΔI_Q	Quiescent Current Change	8V ≤ V_{IN} ≤ 20V			1.0	
		1mA ≤ I_O ≤ 40mA			0.1	
V_n	Output Noise Voltage	f = 10 Hz to 100 kHz (Note 4)		40		µV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz 8V ≤ V_{IN} ≤ 16V	47	62		dB
I_{PK}	Peak Output Current			140		mA
$\frac{\Delta V_O}{\Delta T}$	Average Output Voltage Tempco	I_O = 5mA		−0.65		mV/°C
V_{IN} (Min)	Minimum Value of Input Voltage Required to Maintain Line Regulation			6.7	7	V
θ_{JA}	Thermal Resistance (8-Bump micro SMD)			230.9		°C/W

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Dissipation (Note 5)	Internally Limited
Input Voltage	35V
Storage Temperature	−65°C to +150°C
ESD Susceptibility (Note 2)	1kV
Operating Junction Temperature	
SO-8, TO-92	0°C to 125°C
micro SMD	−40°C to 85°C
Soldering Information	
Infrared or Convection (20 sec.)	235°C
Wave Soldering (10 sec.)	260°C (lead time)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device outside of its stated operating conditions.

Note 2: Human body model, 1.5 kΩ in series with 100pF.

Note 3: Power dissipation ≤ 0.75W.

Note 4: Recommended minimum load capacitance of 0.01µF to limit high frequency noise.

Note 5: Typical thermal resistance values for the packages are:

Z Package: θ_{JC} = 60 °C/W, = θ_{JA} = 230 °C/W

M Package: θ_{JA} = 180 °C/W

micro SMD Package: θ_{JA} = 230.9°C/W

Figure-Q6(b)

– THE END –

Worksheet for Q3(b)

Student Name: _____ I/C No.: _____