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INTERNATIONAL COLLEGE PENANG (507232-U)
LAUREATE INTERNATIONAL UNIVERSITIES

FINAL
Examination Paper

(COVER PAGE)

Session : January 2014

Programme : DIPLOMA IN ELECTRICAL & ELECTRONIC ENGINEERING

Course : EEE1102: ELECTRONIC DEVICES AND CIRCUIT THEORY 1

Date of Examination : 11 March 2014

Time : 11:00am – 1:00pm Reading Time : Nil

Duration : 2 Hours

Special Instructions :

This paper consists of SIX (6) questions. Answer any FOUR (4) questions in the answer booklet provided. All questions carry equal marks.

Materials permitted :

Non-Programmable Scientific Calculator

Materials provided :

Examiner(s) : Liong Han Wen

Moderator : Chan Tse Wei

This paper consists of 8 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME
(DEEI)

EEE 1102: ELECTRONIC DEVICES AND CIRCUIT THEORY 1
FINAL EXAMINATION: JANUARY 2014 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks. The marks allocated to each sub-question are shown in brackets at the right-hand margin.

Question 1

- a. For Figure Q1(a), calculate V_{OUT} and the current flowing through the diode D1. Assume practical models for all the diodes. (5 marks)

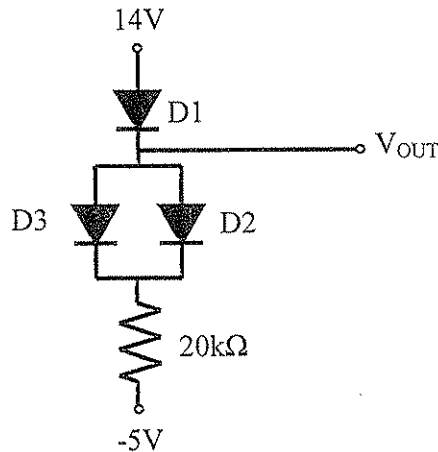


Figure Q1(a)

- b. What is the minimum value of V_{IN} to saturate the transistor circuit as shown in Figure Q1(b)? (6 marks)

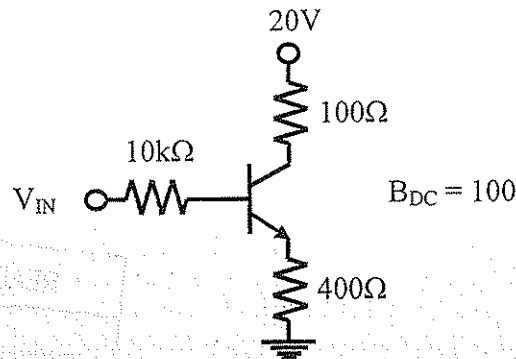


Figure Q1(b)

c. Sketch the output waveform of the following clipper circuits. The input waveform is shown in Figure Q1(c). Assume all the diodes in this part are ideal.

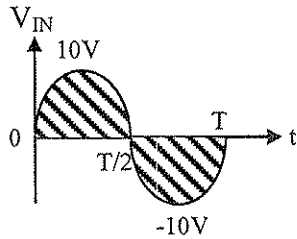
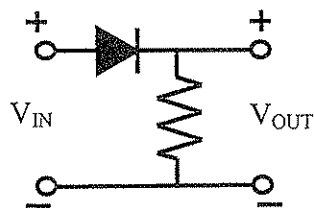
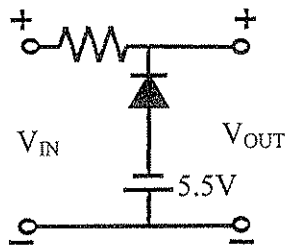


Figure Q1(c)

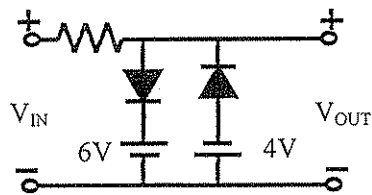
i. (3 marks)



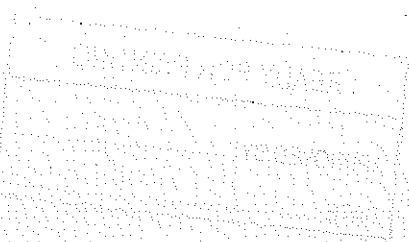
ii. (3 marks)



iii. (5 marks)



d. State the three modules for the basic DC power supply. (3 marks)



Question 2

a. Determine the I_{CQ} for the transistor circuit shown in Figure Q2(a). Given $\beta_{DC} = 150$.

(8 marks)

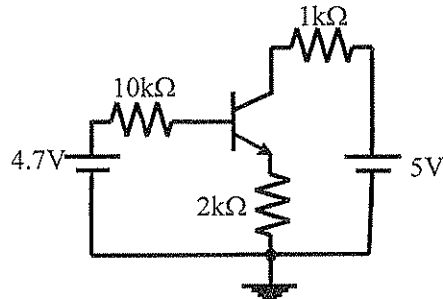


Figure Q2(a)

b. For the unloaded amplifier in Figure Q2(b),

i. Perform DC analysis and sketch the ac equivalent circuit with correct components value.

(7 marks)

ii. Find the total ac input resistance, $R_{in(tot)}$

(3 marks)

iii. Find the amplifier voltage gain, A_v

(4 marks)

iv. Find the new amplifier voltage gain if a $5k\Omega$ load resistor is capacitively coupled to the collector terminal.

(3 marks)

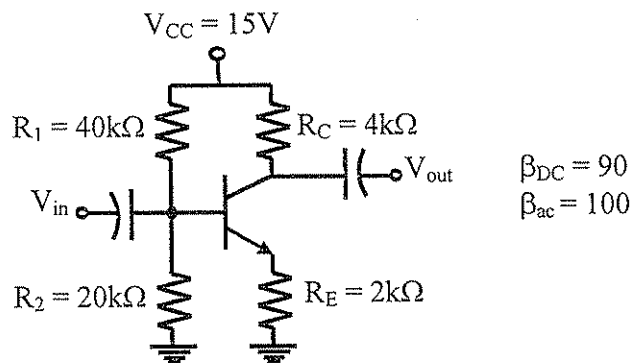


Figure Q2(b)

Question 3

- a. What is the power dissipation in the resistors and zener diode in Figure Q3(a). Given $V_s = 20V$, $R_s = 500\Omega$, $R_L = 2k\Omega$, $V_Z = 10V$. Assume the zener diode is ideal. (10 marks)

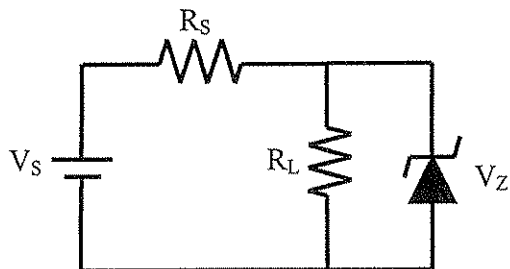


Figure Q3(a)

- b. For Figure Q3(b), find the minimum value of R_2 that will cause TR2 just saturate. The β_{DC} for both transistors is 50. (10 marks)

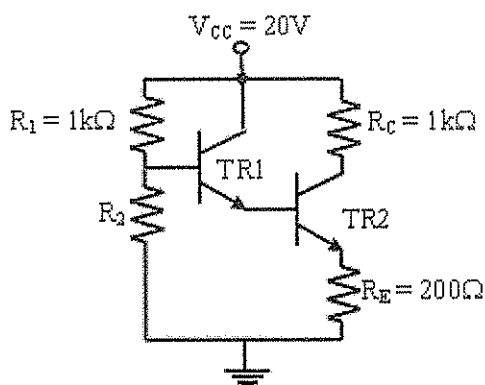


Figure Q3(b)

- c. Draw the DC load line for Figure Q3(c). Assume the $\beta_{DC} = 80$. (5 marks)

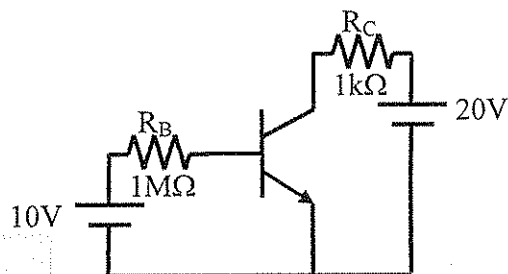


Figure Q3(c)

Question 4

- a. Figure 4(a) is a multistage amplifier which is driven by an ac source and the second stage is loaded with a load resistor, R_L of $18k\Omega$. Given $R_1=R_5=33k\Omega$, $R_2=R_6=8.2k\Omega$, $R_3=R_7=3.3k\Omega$, $R_4=R_8=1k\Omega$ and $\beta_{ac}=\beta_{DC}=170$. Determine
- (i) The voltage gain for each stage. (15 marks)
 - (ii) Overall voltage gain. (3 marks)

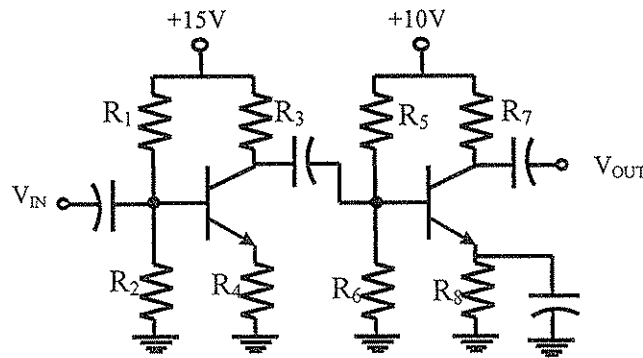


Figure 4(a)

- b. For an N-Channel JFET, $I_{DSS} = 7.5mA$, $V_p = 3V$ and $V_{GS} = -1V$. Find the values of
- i. I_D (3 marks)
 - ii. g_{mo} (2 marks)
 - iii. g_m (2 marks)

Question 5

- a. A load resistance(R_L) is capacitively coupled to the emitter in Figure Q5(a). Draw the ac equivalent circuit for the circuit in Figure Q5(a). What value of R_L will cause the voltage gain become 0.8? (12 marks)

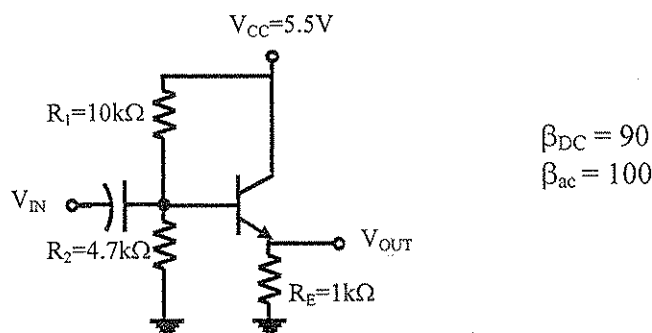


Figure Q5(a)

b. Sketch the output waveform of the clamper circuit as shown in Figure Q5(b) (5 marks)

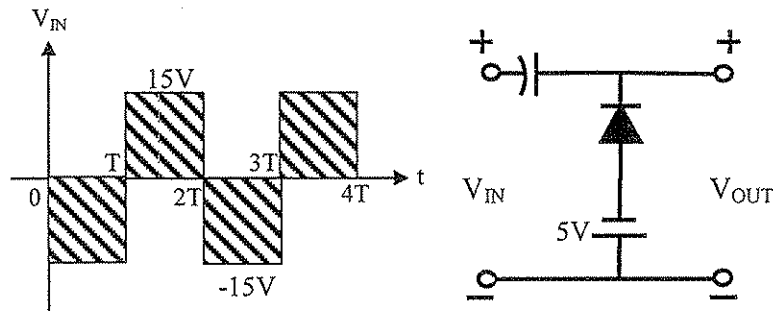


Figure Q5(b)

c. Sketch the collector characteristic curves of a typical NPN bipolar junction transistor. Label each region of the characteristics curve. What are the two regions that are use for switching purpose? (8 marks)

Question 6.

a. Find V_{GS} and V_{DS} for the E-MOSFET circuit in Figure Q6(a). Datasheet information is listed with the circuit. (6 marks)

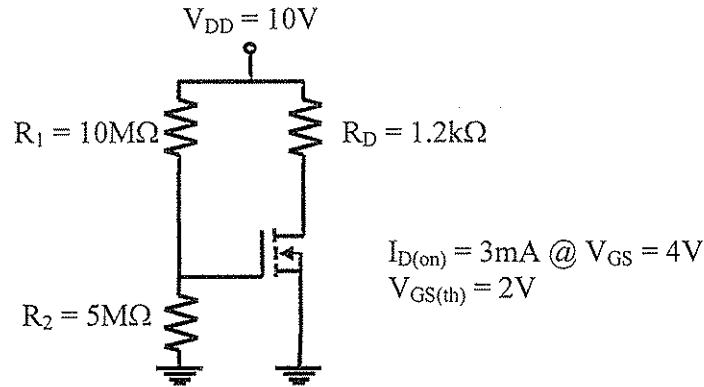


Figure Q6(a)

b. For the JFET amplifier of Figure Q6(b), $g_m = 2\text{mS}$, $r'_{ds} = 30\text{k}\Omega$, $R_s = 3\text{k}\Omega$, $R_D = R_L = 2\text{k}\Omega$, $R_1 = 800\text{k}\Omega$, $R_2 = 200\text{k}\Omega$ and $R_s = 5\text{k}\Omega$. Find

- i. DC value of R_{in} (3 marks)
- ii. Voltage gain, $A_v = V_L / V_i$ (8 marks)
- iii. Current gain, $A_v = i_L / i_i$ (8 marks)

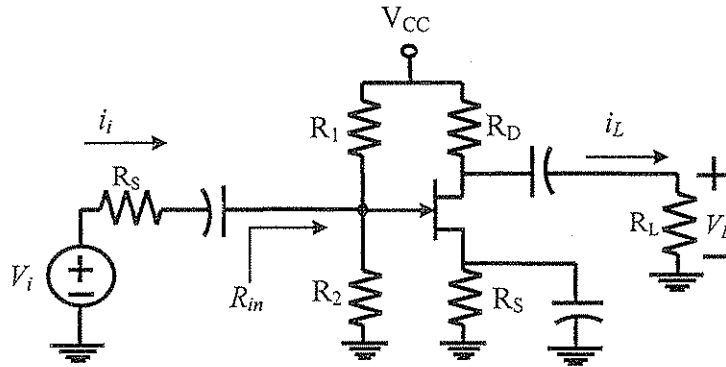


Figure Q6(b)

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<EEE 1102(F)/January 2014/Liong Han Wen /2-1-2014>

