



INTI
International College Penang
LAUREATE INTERNATIONAL UNIVERSITIES*

FINAL
Examination Paper

(COVER PAGE)

Session : January 2016

Programme : Diploma in Electrical and Electronic Engineering (DEEI)

Course : EEE 2101: Introduction to Digital Electronics

Date of Examination : 9 March 2016 (Wednesday)

Time : 8:00am – 10:00am Reading Time : Nil

Duration : 2 Hours

Special Instructions :

This paper consists of SIX (6) questions. Answer any FOUR (4) questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL

Materials permitted :
Non-Programmable Scientific Calculator

Materials provided :
A4 Size Graph Paper

Examiner(s) : Mr. Steven Khoo Boo Tap

Moderator : Mr. Kevin Tan

This paper consists of 10 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
 EEE2101: INTRODUCTION TO DIGITAL ELECTRONICS
 FINAL EXAMINATION: JAN2016 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

- (a) A combinational logic circuit is required, which accepts BCD inputs 0000 to 1001 and displays the letter A through J, respectively, as shown below in Figure 1(a-1). The BCD inputs are labelled as KLMN, K is the MSB and N is the LSB. Figure 1(a-2) shows a Common-Cathode 7 segment display. Assume all unused inputs as don't care.

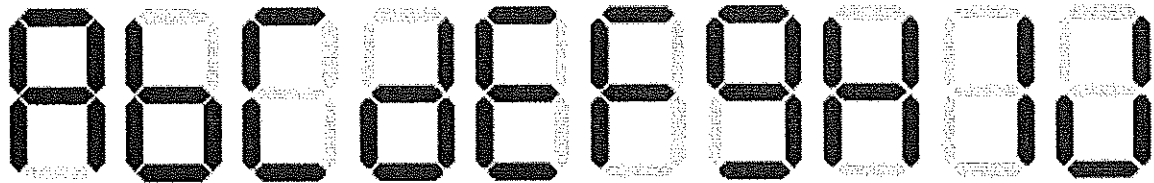


Figure 1(a-1)

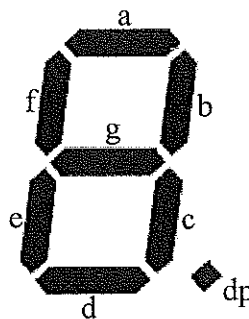


Figure 1(a-2)

- (i) Develop the truth table for the inputs to segments a through g of the 7 segment. (4 marks)
- (ii) Determine the SOP form of the logic expression for segments a and d. (6 marks)
- (iii) Implement the logic expression using only 2-input NOR gate with minimum IC consideration. State the number of ICs used. Show all working clearly. (7 marks)

(b) Using Boolean algebra only, simplify to the simplest SOP form:

(i) $S = ABC\bar{C} + A(\overline{B + C})(B + C)$ (4 marks)

(ii) $R = \bar{A} \cdot \bar{B} \cdot C + A \cdot B \cdot C + \bar{A} \cdot \bar{B} \cdot \bar{C} + \bar{A} \cdot B \cdot C + A \cdot \bar{B} \cdot C$ (4 marks)

Question 2

(a) If the waveform in Figure 2(a) is applied to a sampling circuit and is sampled at every 3ms, determine the following:

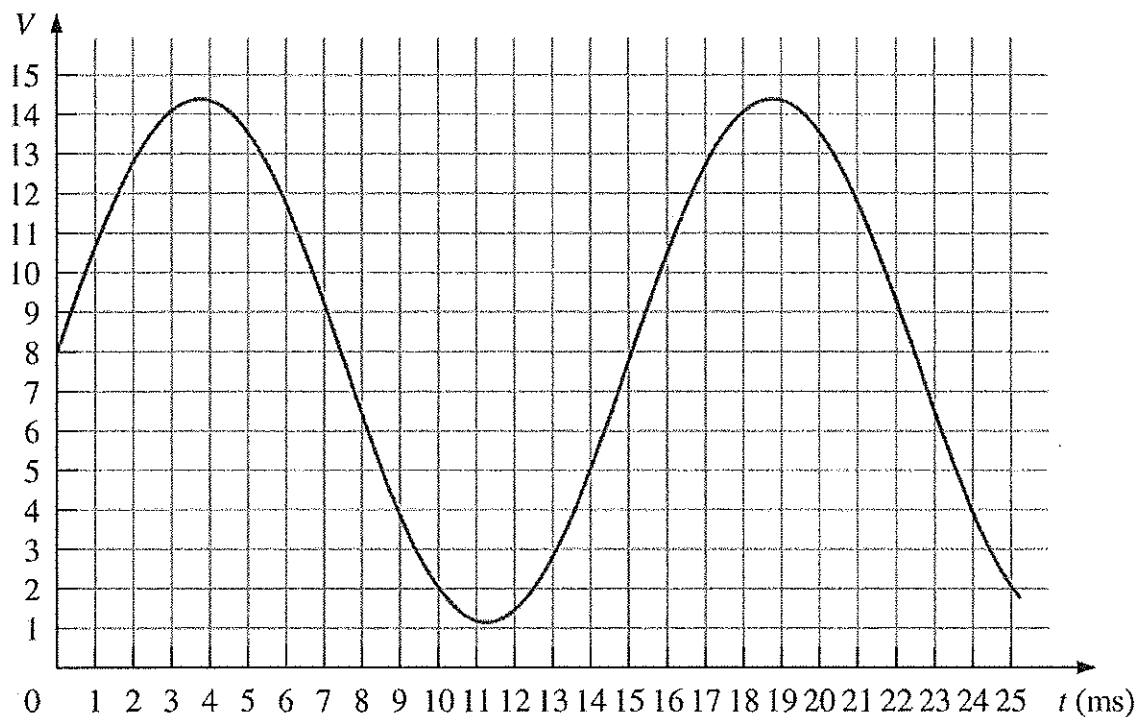


Figure 2(a)

- (i) Draw the output of the sampling circuit. Assume a one-to-one voltage correspondence between the input and output. (3 marks)
- (ii) If the output in part (i) is applied to a hold circuit, draw the output of the hold circuit. (3 marks)

- (iii) If the output in part (ii) is quantized using 4 bits, list the resulting sequence of binary codes.

(3 marks)

- (b) Figure 2(b) shows the logic symbol of full adder with an output sum (S) and a carry output (C_{out}) bit. A full adder is a device that performs binary addition of two single input bits (X , Y) and a carry input bit (C_{in}).

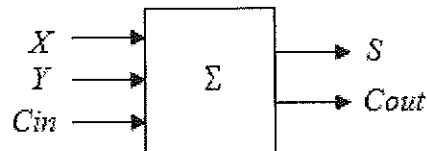


Figure 2(b)

- (i) Generate the truth table and hence derive the simplest Boolean expression of S and C_{out} .

(6 marks)

- (ii) Using X , Y , C_{in} as input and S and C_{out} as output, construct a Full Adder using two half adders and an OR gate.

(3 marks)

- (c) Perform the following number system transformation. Show all workings clearly.

- (i) $4A.4F_{16}$ to decimal equivalent with 8 decimal points accuracy.

(3 marks)

- (ii) $[10216.01_8 \times 16_8]$ to hexadecimal equivalent with 2 hexadecimal points accuracy.

(4 marks)

Question 3

- (a) Design a synchronous 3-bit counter using positive edge-triggered RS flip-flops. Assume all unused states as don't care. The counter will count from $000 \Rightarrow 111 \Rightarrow 101 \Rightarrow 010 \Rightarrow 000$. Use $Q_2Q_1Q_0$ outputs labelling for R_2S_2 , R_1S_1 and R_0S_0 inputs. Provide proper labelling for the designed logic circuit. Show all workings clearly.

- (i) Provide the excitation table used.

(1 mark)

- (ii) Provide the transition table/ next state table.

(3 marks)

- (iii) Simplify using Karnaugh map and Boolean algebra if necessary. (3 marks)
 - (iv) Draw the complete logic circuit diagram with proper label. (3 marks)
- (b) Design a synchronous 3-bit counter that counts in the sequence $101 \Rightarrow 010 \Rightarrow 000 \Rightarrow 111 \Rightarrow 101$. Choose a suitable type of flip flops to use for this design such as D flip flops only or T flip flops only or JK flip flops only. Also, use an appropriate control signal together with flip flops of your choice to load the initial value 101 for the counter using a single reset signal. Assume all unused states as don't care. Use $Q_2Q_1Q_0$ as output labelling. Provide proper labelling for the designed logic circuit. Show all workings clearly.
- (i) Provide the excitation table used. (1 mark)
 - (ii) Provide the transition table/ next state table. (3 marks)
 - (iii) Simplify using Karnaugh map and Boolean algebra if necessary. (3 marks)
 - (iv) Draw the complete logic circuit diagram with minimum components consideration. (4 marks)
 - (v) Comment and compare with the designed logic circuit in Question 3(a). (4 marks)

Question 4

- (a) Assume that the numbering system used is a 7-bit system. Show all working clearly. Express the decimal number +28 and -28 in the sign-magnitude, 1's complement and 2's complement form as shown in the Table 4(a).

	+28	-28
Sign-magnitude		
1's complement		
2's complement		

Table 4(a)

(6 marks)

- (b) Figure 4(b) below shows a 3-bit synchronous counter which is designed so that it performs a special counting sequence. Analyse its operation by determining its counting sequence. Switch S is a control signal used to control the sequence of the counting. Flip-flop FF2 is MSB and FF0 is LSB. Use $D_2T_1D_0$ inputs labelling for Q_2 , Q_1 and Q_0 outputs. Show all workings clearly.

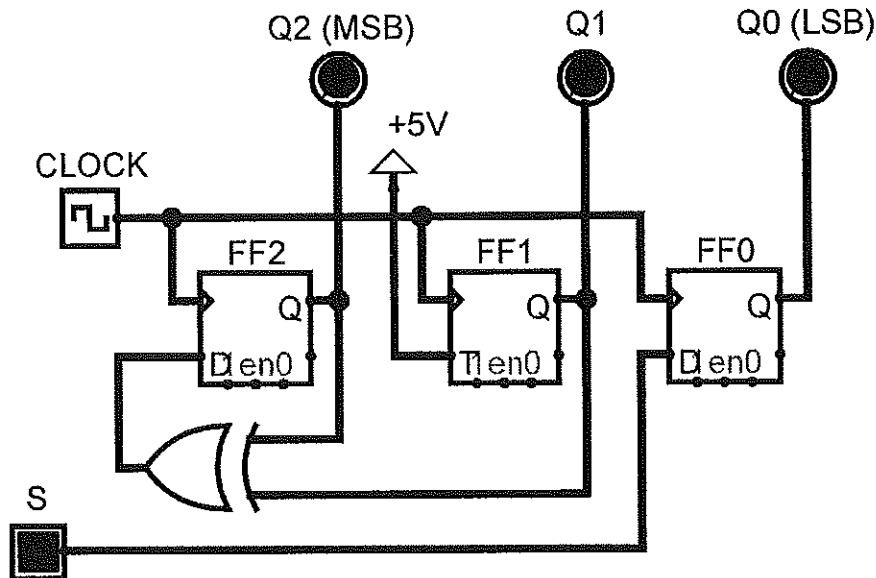


Figure 4(b)

- (i) Provide the Boolean expressions from the logic circuit. (1 mark)
 - (ii) Provide all Karnaugh maps according to the expressions. (3 marks)
 - (iii) Provide the transition table/ next state table with excitation table. (4 marks)
 - (iv) Draw the state diagram and comment on the outcome of the states obtained. What application can this circuit be used for? (4 marks)
- (c) A binary-weighted-input DAC is shown in Figure 4(c). If the LSB bit resistor has a value of $320\text{k}\Omega$, compute the values of the other input resistors. Also, calculate the V_{out} if the DAC has a binary input of 1011 with Logic 1 (HIGH) as $+3.0\text{V}$ and Logic 0 (LOW) as 0V . Assume that R_f equals to $12\text{k}\Omega$. What are the disadvantages of this method of DAC? (7 marks)

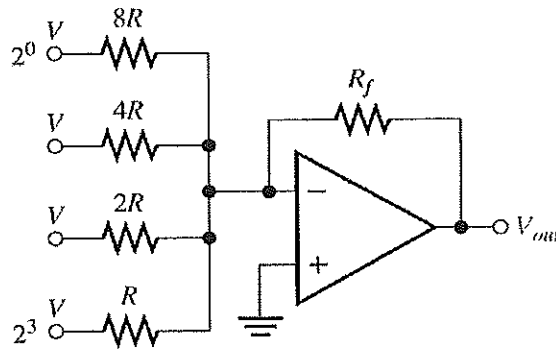


Figure 4(c)

Question 5

- (a) The four inputs (W, X, Y, Z) to a communication network system block diagram represent an 8421 BCD code as shown in Figure 5(a). The output (F) is 1 if the decimal number represented by the inputs is exactly divisible by 2. Assume that only valid 8421 BCD codes occur as inputs, other inputs will be treated as 0 for the output. Show all workings clearly.

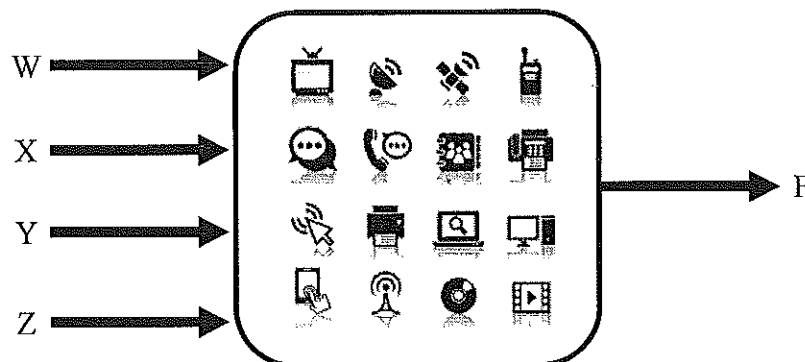


Figure 5(a)

- (i) Generate the complete truth-table of the network system. (3 marks)
- (ii) Use Karnaugh map to obtain the simplest expression for the network system. (3 marks)
- (iii) Draw the logic circuit for the network system using only NAND gates with minimum gates and IC consideration. Assume that the complements of the variables ARE available. (4 marks)
- (iv) Implement the expression obtained in Q5a(ii) using an 8-to-1 MUX with Z as the select line. (3 marks)

- (v) If the company had decided to use only NOR gates for the network design, generate the complete simplest circuit for the network with minimum gates consideration. Assume that the complements of the variables ARE NOT available.

(3 marks)

- (b) Use the given Karnaugh map and Boolean algebra to obtain the minimum

- (i) SOP expression for the function,
 $F(W, X, Y, Z) = \prod(0, 2, 3, 4, 6, 8, 10, 11, 12, 14)$.

(3 marks)

- (ii) POS expression for the function,
 $F(K, L, M, N) = \sum(0, 1, 4, 5, 6, 7, 11, 13)$.

(3 marks)

- (iii) POS expression for the function,
 $F(A, B, C, D) = \sum(0, 1, 2, 3, 5, 6, 7, 8) + d(10, 11, 12, 13, 14, 15)$.

(3 marks)

Question 6

- (a) Figure 6(a) has three inputs (A, B, C) and two outputs (Y, Z).
 Table 6a(i) shows a portion of quadruple 2-input AND gates datasheet.
 Table 6a(ii) shows a portion of quadruple 2-input OR gates datasheet.
 Table 6a(iii) shows a portion of quadruple 2-input XOR gates datasheet.

- (i) Using the datasheets given, determine the maximum propagation delay time. Show all working clearly.

(6 marks)

- (ii) What is minimum operating frequency that can be applied to this circuit without affecting the functionality of the circuit? State the function of this circuit.

(4 marks)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	$C_L = 15 \text{ pF}$ $R_L = 400\Omega$		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			19	ns

Table 6a(i) AND gate

Symbol	Parameter	$R_L = 2\text{ k}\Omega$				Units
		$C_L = 15\text{ pF}$		$C_L = 50\text{ pF}$		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	11	4	15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	11	4	15	ns

Table 6a(ii) OR gate

Symbol	Parameter	Conditions	$C_L = 15\text{ pF}, R_L = 400\Omega$		Units
			Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Other Input LOW		23	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			17	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Other Input HIGH		30	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			22	ns

Table 6a(iii) XOR gate

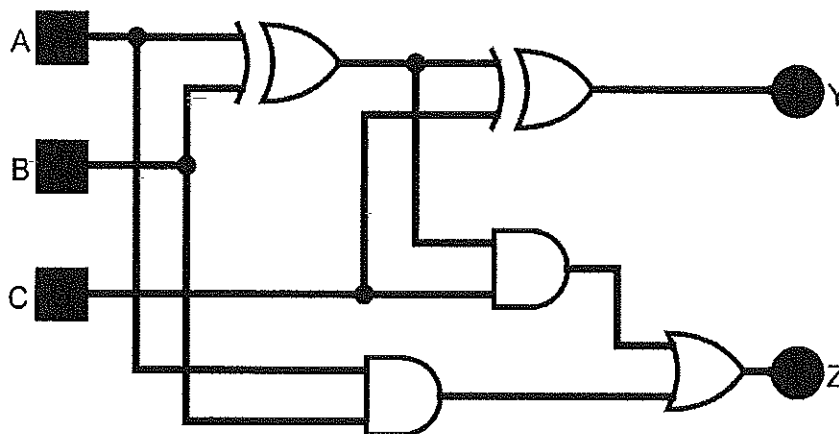


Figure 6(a)

- (b) An 10-bit DAC produces an output current in proportion to its digital input. For a digital input of 0000101000, an output current of 20mA is produced.
- (i) What will the output current be if the digital input is 1000111101? (3 marks)
 - (ii) What is the maximum output current produced by this DAC? (3 marks)
 - (iii) What should the digital input be if a 205mA output current is required? (3 marks)

- (c) Table 6(c) shows the current ratings of TTL series logic gates. A 74LS04 NOT gate output is driving 2 Standard TTL gate inputs, 3 Advanced Low-Power Schottky TTL gate inputs, 4 Fast TTL gate inputs and 1 Schottky TTL gate input as shown in Figure 6(c). Determine if there is a loading problem.

(6 marks)

TTL Series	Output Drive		Input Loading	
	I_{OH}	I_{OL}	I_{IH}	I_{IL}
74	400 μ A	16mA	40 μ A	1.6mA
74S	1.0mA	20mA	50 μ A	2.0mA
74LS	400 μ A	8mA	20 μ A	400 μ A
74AS	2.0mA	20mA	200 μ A	2.0mA
74ALS	400 μ A	8mA	20 μ A	100 μ A
74F	1.0mA	20mA	20 μ A	600 μ A

Table 6(c)

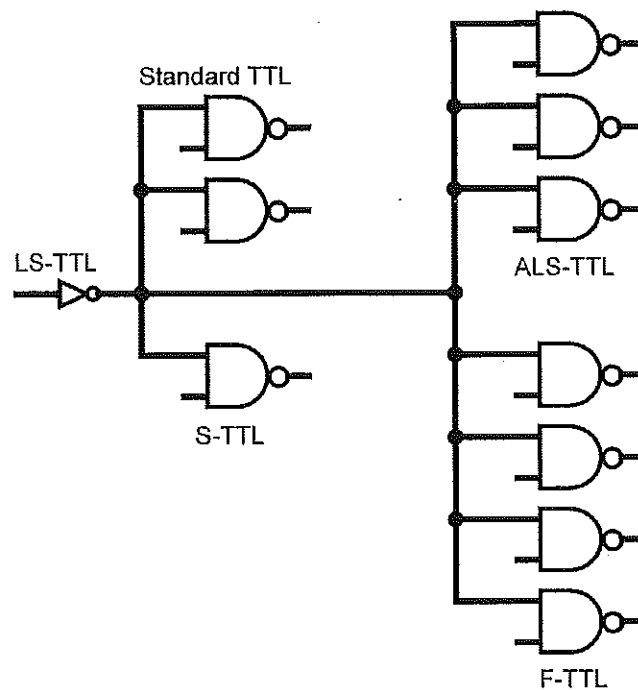


Figure 6(c)

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