INTI
International College Penang
LAUREATE INTERNATIONAL UNIVERSITIES

FINAL
Examination Paper

(COVER PAGE)

Session	:	**January 2016**
Programme	:	Diploma in Electrical and Electronic Engineering (DEEI)
Course	:	**EEE 1106: Analogue Electronics**
Date of Examination	:	10 March 2016 (Thursday)
Time	:	8.00am – 10.00am
Duration	:	2 Hours Reading Time : Nil
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : **THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL**

Materials Permitted :
Scientific Calculator (Model fx570 Series)

Materials Provided :
Worksheet for Question 3(a) & Worksheet for Question 3(b)

Examiner(s)	:	**Mr. Chan Tse Wei**
Moderator	:	Dr. Khoo Bee Ee

This paper consists of 8 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE1106: ANALOGUE ELECTRONICS
FINAL EXAMINATIONS: JANUARY 2016 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks. The marks allocated to each sub-question are shown in square brackets at the right-hand margin. The assessor reserves the rights to ignore your answers if they are ambiguous.

Question 1

a. Figure-Q1(a) shows an AC circuit model of a capacitor coupled amplifier. C_1 and C_2 are coupling capacitors of the amplifier, while C_b models the parasitic capacitance of the amplifying element that bridges its input and output terminals.

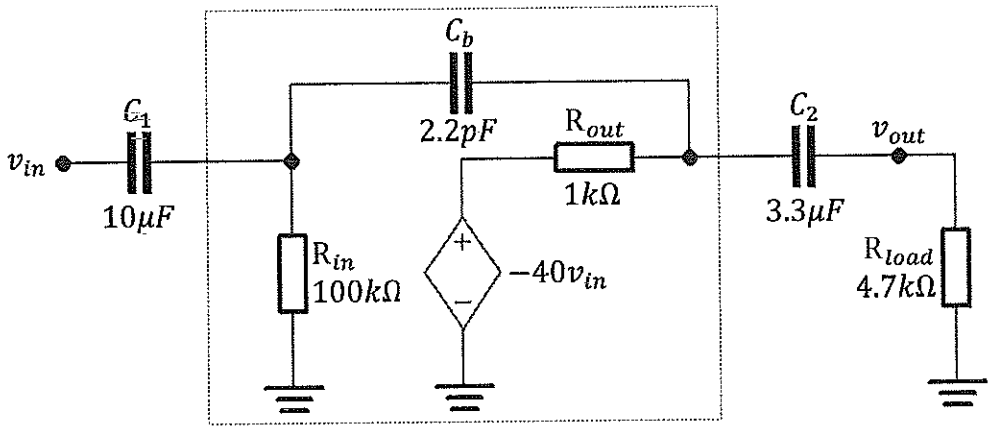

Figure-Q1(a)

i. Explain why capacitors C_1 and C_2 are needed in the amplifier. [3]

ii. Determine the maximum voltage gain, v_{out}/v_{in} of the amplifier circuit. [4]

iii. Based on the given component values, determine the lower cutoff and upper frequencies of the amplifier respectively. [8]

b. Figure-Q1(b) shows a BJT-based circuit, utilized as a phase-split amplifier. v_{in} is a sinusoidal signal of 2.4 V amplitude, at 1 kHz (mid-band frequency). The following characteristics of the 2N3904 transistor are assumed:

- The DC biasing base current, $I_{B_Q} \approx 0$.
- $V_{BE} = 0.6\,V$ for both DC and AC operations.
- $h_{fe} \gg 1$.
- h_{oe} and h_{re} can be ignored.

Sketch the timing diagram of the following signals using a common time scale. Show the maximum and minimum voltages clearly.

i. v_B [4]

ii. v_{out1} [3]

iii. v_{out2} [3]

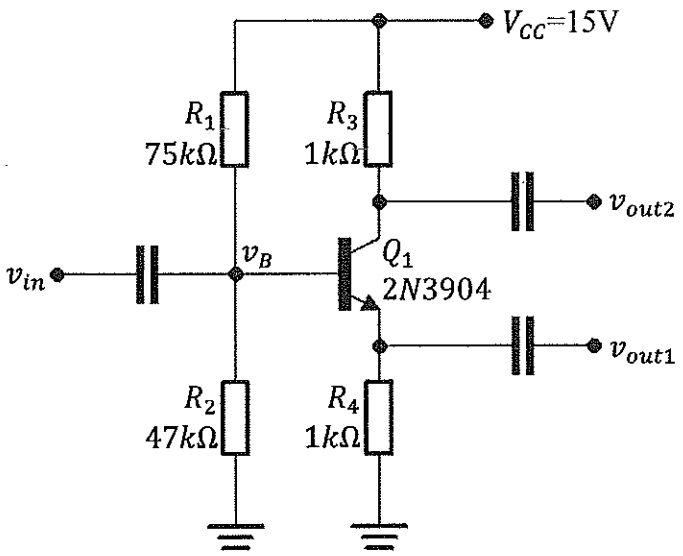

Figure-Q1(b)

Question 2

a. i. Differentiate the respective conduction angle of the amplifying component in class A, class B and class C power amplifiers. [6]

ii. A class A power amplifier converts 12 W of DC power to 8 W of AC power. Calculate the power amplifier's power efficiency in percentage. [3]

iii. State one advantage and one disadvantage of class A power amplifiers. [4]

iv. State one advantage and one disadvantage of class B power amplifiers. [4]

b. Figure-Q2(b) shows a basic circuit configuration of a class B power amplifier. Show that its idealized power conversion efficiency can be as high as 78.5% in respond to a sinusoidal input. [8]

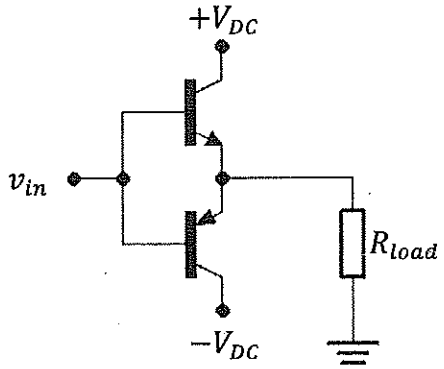

Figure-Q2(b)

Question 3

a. Figure-Q3(a) shows an op-amp circuit utilized as a comparator. Assume ideal op-amp operation, sketch the output signal on the provided worksheet, titled "Worksheet for Question-3(a)", based on the given input voltage, v_{in}. [4]

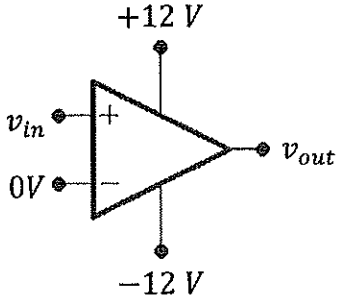

Figure-Q3(a)

b. The circuit in Figure-Q3(a) is modified as shown in Figure-Q3(b).

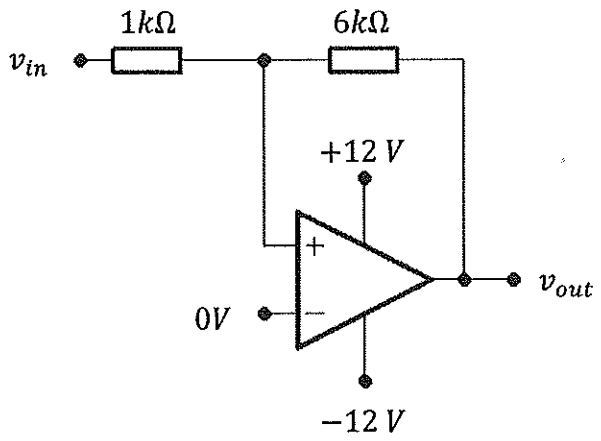

Figure-Q3(b)

i. Identify the name of the circuit shown in Figure-Q3(b). [2]

ii. Explain how does the circuit modification change the operation of the original circuit in Figure-Q3(a). [5]

iii. Assume ideal op-amp operation, sketch the output signal on the provided worksheet, titled "Worksheet for Question-3(b)", based on the given input voltage, v_{in}. [4]

c. Figure-Q3(c) shows the block diagram of a temperature measuring equipment.

v_{in} is the voltage signal that represents the actual temperature being measured. The Analog-to-Digital Converter converts the analog input voltage to its corresponding digital format. It is characterized to have a minimum input voltage of 0.2V. The Processor further decodes the digital signal so that the actual temperature can be displayed at the Display Unit.

A temperature sensor is selected to be used in association with the temperature measuring equipment. The sensor has a linear output characteristic defined as 10 mV/°C and its measurement ranges from 0°C to 200°C. It is obvious that the output voltage of the temperature sensor is not suitable for the application and needs to be further conditioned.

Design a circuit to condition the signal from the temperature sensor before it is applied to the temperature measuring equipment. [10]

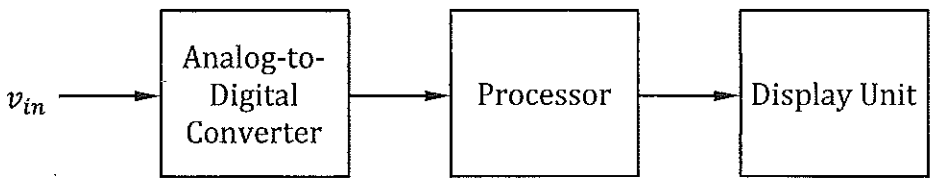

Figure-Q3(c)

Question 4

a. i. Sketch the frequency response of a first order passive low pass filter circuit. [2]

ii. Show how a first order passive low pass filter circuit can be implemented using one resistor and one capacitor. [2]

iii. State the cutoff frequency of the low pass filter circuit implemented in part (a)(ii). [2]

iv. If a cutoff frequency of 10 kHz is required for the circuit implemented in part (a)(ii), determine the required capacitance if a 4.7 kΩ resistor is used. [4]

b. i. If a better cutoff characteristic is required in a low pass filter circuit, suggest two different approaches to fulfill this requirement. Show schematic diagrams to aid understanding. [6]

ii. State one disadvantage for each of the approach suggested in part (b)(ii). [4]

c. Quantitatively explain how a basic integrator circuit can be used to convert a second order band pass filter circuit to a second order low pass filter circuit. [5]

Question 5

a. i. What is an oscillator circuit? [2]

ii. State one application of an oscillator circuit. [2]

iii. Sate the two board categories of oscillator circuit. [4]

iv. State two fundamental requirements of the oscillator circuit output signal. [4]

b. Figure-Q5(b) shows a oscillator circuit build from the popular 555 timer IC. Based on the circuit configuration,

i. determine the maximum and minimum output frequencies of the oscillator circuit. [4]

ii. determine the maximum and minimum duty cycle of the output signal. [4]

iii. suggest a simple approach to obtain an output signal from the 555 timer IC that is oscillating symmetrically along the 0V rail. [3]

iv. state one drawback of the circuit configuration. [2]

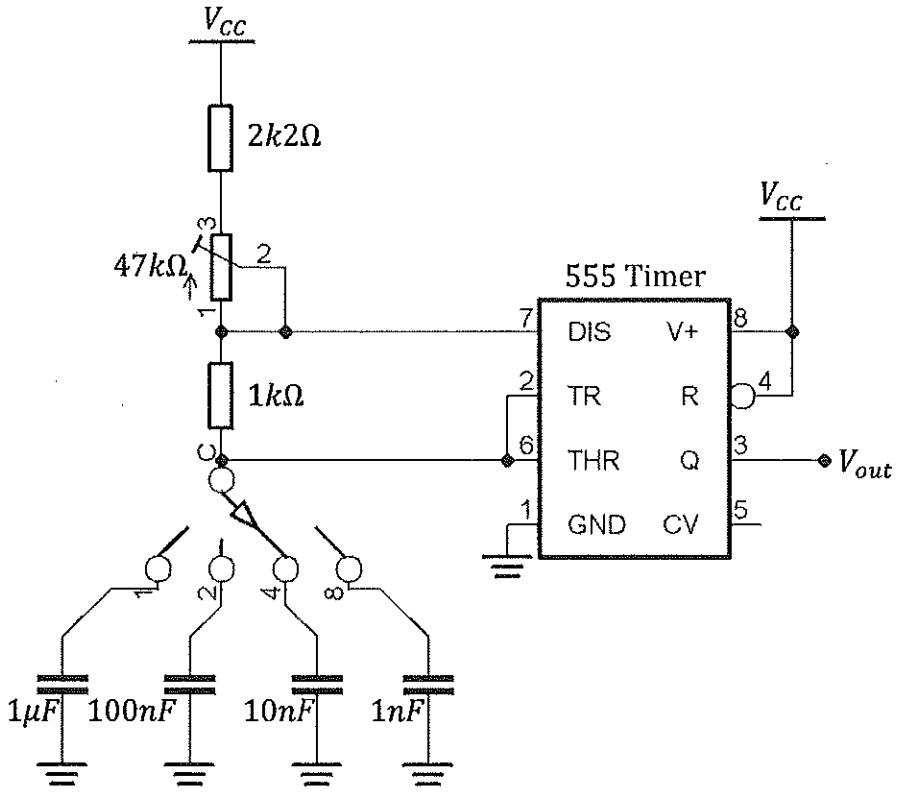

Figure-Q5(b)

Question 6

a. What is common about nodes W, X, Y and Z in the circuit shown in Figure-Q6? [2]

b. Identify the circuit formed by $IC1$, resistor R_1 and the two equivalue resistors R_2 in Figure-Q6. [2]

c. Identify the circuit formed by $IC3$, resistor R_5 and capacitor C in Figure-Q6. [2]

d. Derive the nodal equation for each node at W, X, Y and Z in s-domain. [8]

e. Based on the equations obtained in part (d), derive the expression for each output, V_{out1}, V_{out2}, V_{out3}, and V_{out4}, in terms of V_{in} and the relevant component values, in s-domain. [8]

f. Based on the answer obtained in part (e), state the application of the circuit in Figure-Q6. Justify your answer. [3]

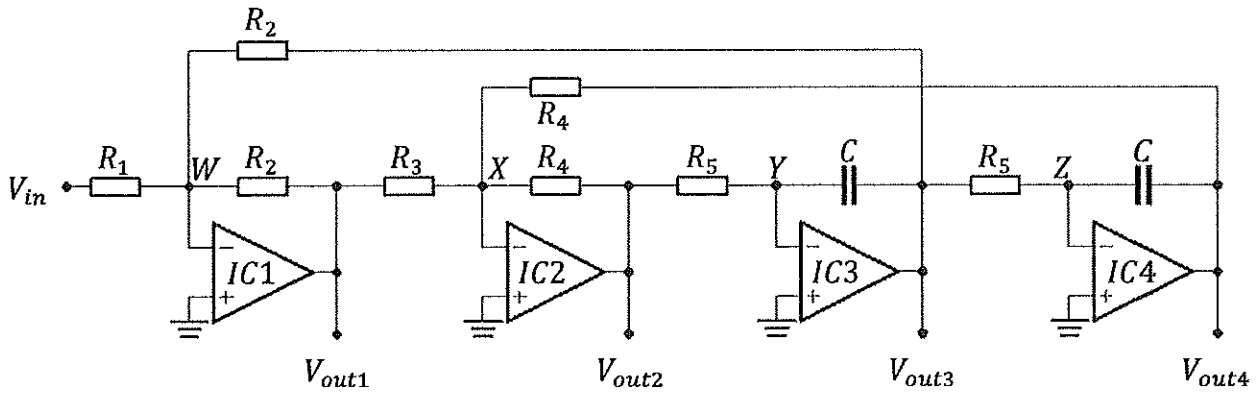

Figure-Q6

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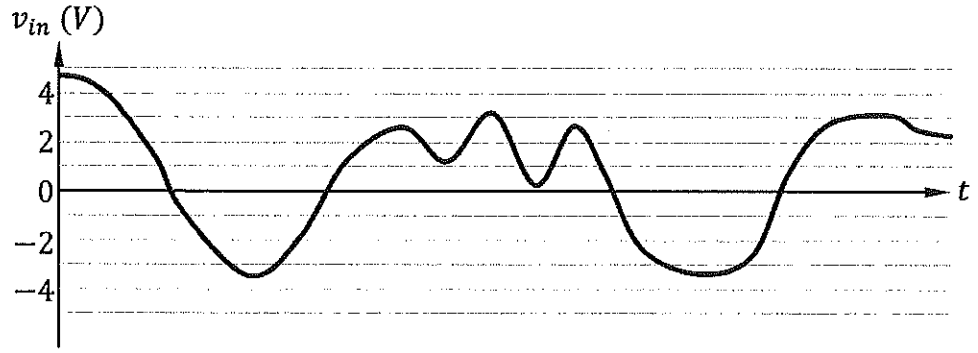
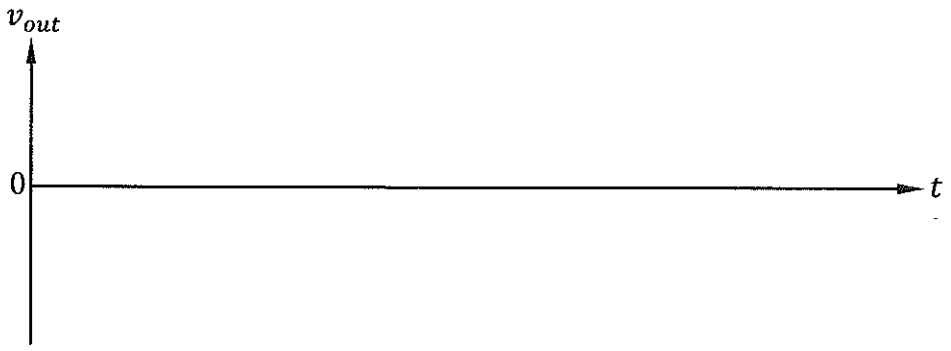
WORKSHEET FOR QUESTION 3(a)





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WORKSHEET FOR QUESTION 3(b)