INTI
International College Penang
LAUREATE INTERNATIONAL UNIVERSITIES

FINAL
Examination Paper

(COVER PAGE)

Session	:	**January 2016**
Programme	:	Diploma in Electrical and Electronic Engineering (DEEI)
Course	:	**EEE 1105: Circuit Theory & Electronic Devices**
Date of Examination	:	8 March 2016 (Tuesday)
Time	:	2:00pm – 4:00pm
Duration	:	2 Hours Reading Time : Nil
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : **THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL**

Materials Permitted : Non-Programmable Scientific Calculator

Materials Provided : Nil

Examiner(s) : **Ms. Shalyn Lim Sheue Hui**

Moderator : Mr. Kevin Tan

This paper consists of 11 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE 1105: CIRCUIT THEORY & ELECTRONIC DEVICES
FINAL EXAMINATION: JAN 2016 SESSION

Instructions: This paper consists of SIX (6) questions. Answer any FOUR (4) questions in the answer booklet provided. All questions carry equal marks.

Question 1

(a) With reference to Figure Q1(a) , calculate

(i) the total resistance.

(2 marks)

(ii) the voltages, V_X and V_Y.

(4 marks)

(iii) the currents, I_1 and I_2.

(4 marks)

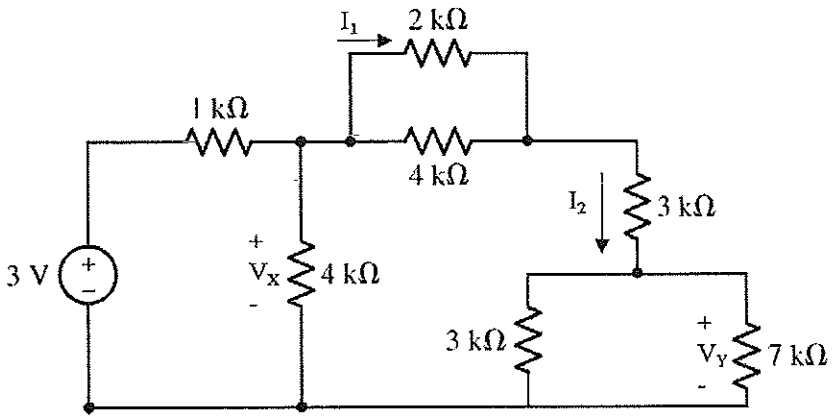


Figure Q1(a)

(b) Many years ago a string of Christmas tree lights was manufactured in the form shown in Figure Q1(b)(i). Today the lights are manufactured as shown in Figure Q1(b)(ii). Is there a good reason for this change?

(3 marks)

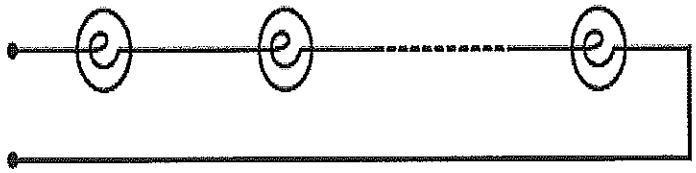


Figure Q1(b)(i)

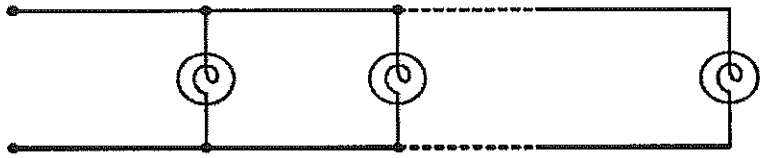


Figure Q1(b)(ii)

(c) With reference to Figure Q1(c). Calculate voltage, V_x using ***Nodal Analysis***.

(5 marks)

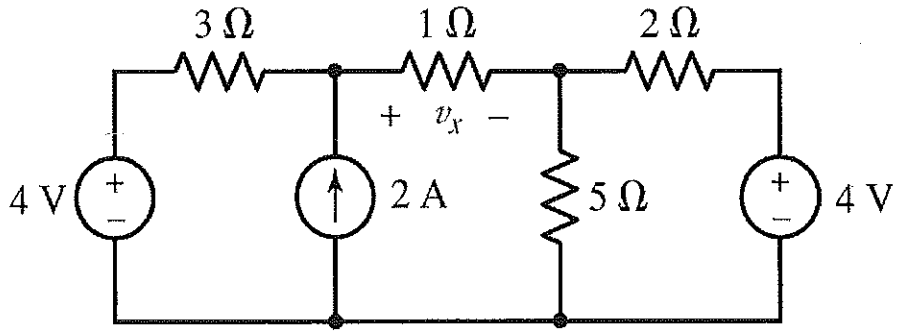


Figure Q1(b)

(d) Calculate the voltage drop across R_L= 4kΩ for the network shown in Figure Q1(d) using ***Thevenin's Theorem***.

(7 marks)

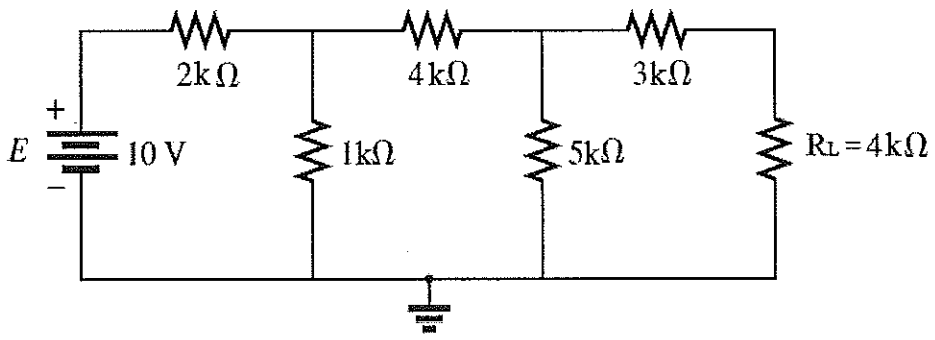


Figure Q1(d)

Question 2

(a) The current through a 0.1 H coil is provided as i = 7 sin (377t - 70°) A. Find the sinusoidal expression for the voltage across the coil. Sketch the v and i curves.

(4 marks)

(b) For the network of Figure Q2(b),given the rms of the supply voltage is 100 $\angle 0^{\circ}$ V determine

[Note: answer in polar form]

(i) the total impedance Z_T.

(3 marks)

(ii) the current I, I_1,I_2 and I_3.

(5 marks)

(iii) the branch which has the highest reactive power. (Verify your answer)

(4 marks)

(iv) the overall circuit's active power and power factor.

(4 marks)

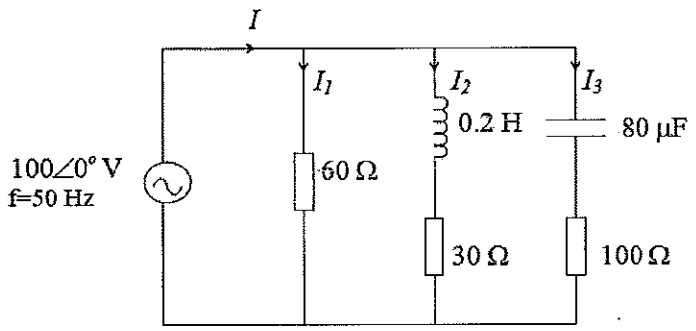


Figure Q2(b)

(c) Refer to the resonant network in Figure Q2(c).

(i) Find the value of L if the resonant frequency is 1800 Hz

(2 marks)

(ii) Find the Q factor of the network.

(3 marks)

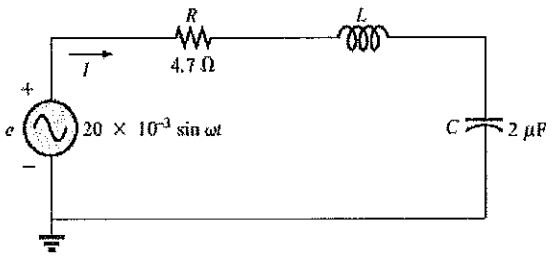


Figure Q2(c).

Question 3

(a) Sketch a graph showing the forward and reverse characteristics of a typical silicon diode and clearly label the relevant information.

(3 marks)

(b) Figure Q3 (b) shows the full wave rectifier circuit with the **input sine wave.**

(ii) Calculate the ripple factor.

(7 marks)

(iii) Determine the value of PIV.

(2 marks)

(iv) Sketch the output voltage at R_L

(2 marks)

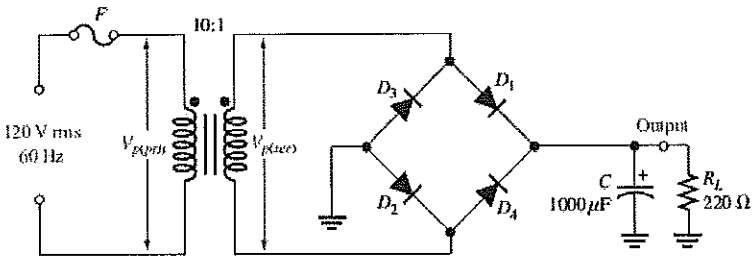


Figure Q3(b)

(c) For the diode network shown in Figure Q3(c), calculate I and V_o.

(5 marks)

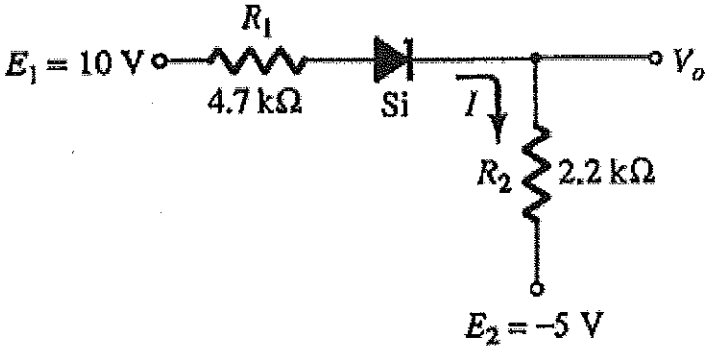
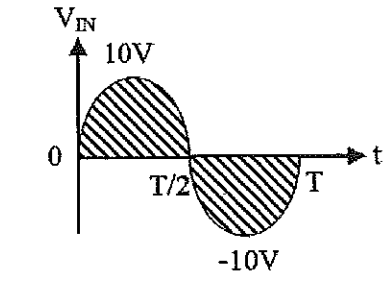


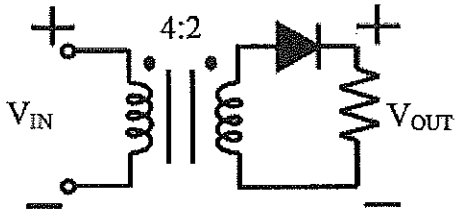
Figure Q3(c)

(d) Sketch the output waveform, V_{OUT} of the following rectifier circuits in Figure Q3(d)(ii) and (iii) . The input waveform, V_{IN} is shown in Figure Q3 (d)(i). Assume all the diodes are ideal.

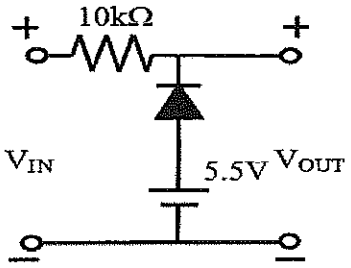
(6 marks)



(i)



(ii)



(iii)

Figure Q3(d)

Question 4

(a) Explain the purpose of dc biasing for a BJT Transistor.

(2 marks)

(b) Determine and sketch the Q-point for the network shown in Figure 4(b). Label the saturation and cut off point on the load line.

(7 marks)

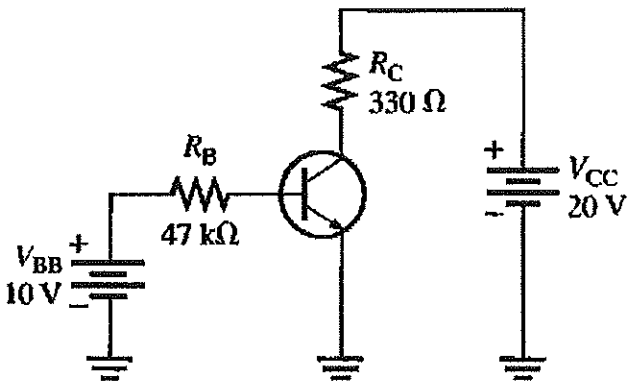


Figure 4(b)

(c) Given the emitter-bias configuration network of Figure Q4(c) with the load line analysis. Calculate the value of,

(i) R_C, R_B, and R_E.

(4 marks)

(ii) β

(2 marks)

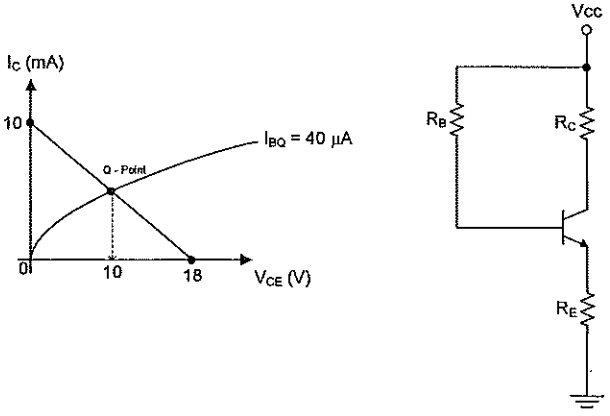


Figure Q4(c)

(d) Figure Q4(d) shows the voltage-divider biased transistor circuit with β=100. Calculate I_B using exact method, calculate

(i) I_B, I_c and I_E.

(6 marks)

(ii) V_B and V_{CE}.

(4 marks)

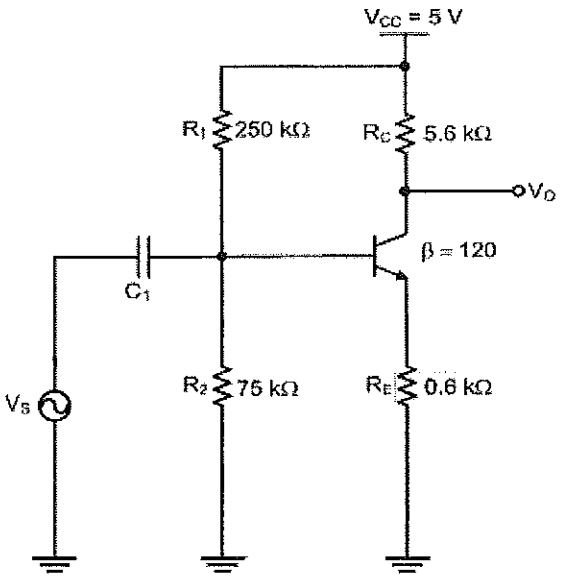


Figure Q4(d)

Question 5

(a) Sketch the D-MOSFET construction with clear labeling and describe the operation.

(5 marks)

(b) Determine I_D and V_{GS} for the JFET with voltage-divider bias in Figure Q5 (b), given that for this particular JFET the parameter values are such that V_D =7V.

(6 marks)

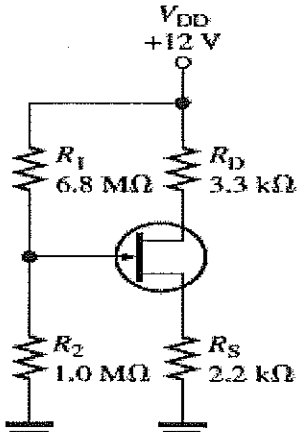


Figure Q5 (b)

(c) For the n – channel FET as shown in Figure Q5(c) it is desired to bias the circuit at I_D = 0.8 mA using V_{DD} = 24V. JFET used has the following parameters; R_D=8.7k Ω, R_G=1M Ω ,V_P = – 2V and I_{DSS} = 1.65 mA. Calculate

(i) R_S.

(6 marks)

(ii) V_{GS}.

(2 marks)

(iii) V_{DS}.

(2 marks)

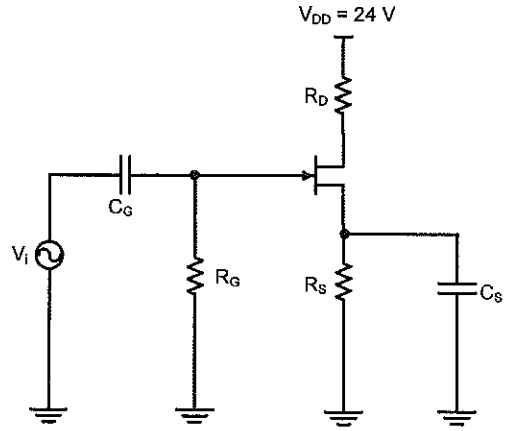


Figure Q5(c)

(d) Differentiate between BJT and FET characteristic.

(4 marks)

Question 6

(a) Refer to the circuit shown in Figure Q6 (a), find V_1 using superposition technique.

(7 marks)

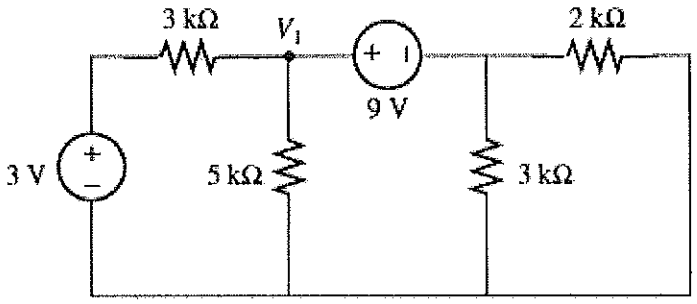


Figure Q6(a)

(b) Figure Q6(b) shows a simple block diagram of an elevator. The passenger selects a destination floor by pressing the floor button on the Input/Control. The Input/Control processes the message and "orders" the motor to "move" the elevator to the particular floor. The sinusoidal voltage source, $v_S(t) = 160 \sin(120\pi t)$ V , the input control has a resistance of 100Ω, and the motor has an impedance of $20 + j\,10$ Ω. Sketch the equivalent circuit and determine the current in the circuit (in time domain)

(7 marks)

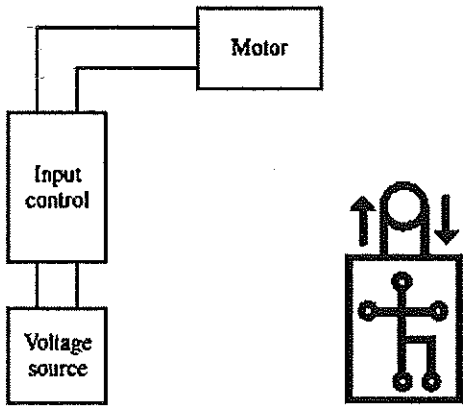


Figure Q6(b)

(c) The circuit as shown in Figure Q6 (c) contains two silicon diodes D1 and D2. Calculate the values of their respective currents, I_1, I_2 and I_3.

(5 marks)

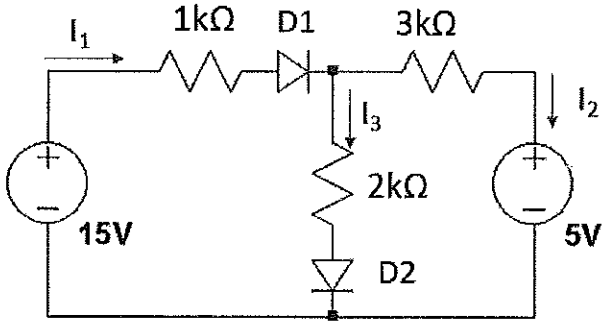


Figure Q6(c)

(d) Determine V_{GS} and V_{DS} for the E-MOSFET circuit in Figure Q6(d). This particular MOSFET has the values of $I_{D(on)} = 200$ mA at $V_{GS(on)} = 4$ V and $V_{GS(th)} = 2$ V.

(6 marks)

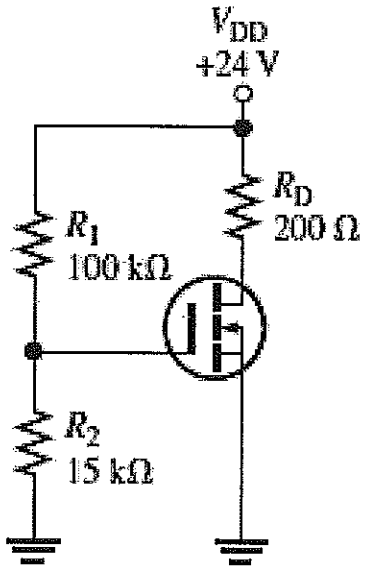


Figure Q6(d)

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