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FINAL
Examination Paper

(COVER PAGE)

Session	:	JANUARY 2015
Programmes	:	**DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING (DEEI)**
Course	:	**EEE2105: INTRODUCTION TO MICROPROCESSOR**
Date of Examination	:	9 March 2015
Time	:	2:00pm – 4:00pm Reading Time: Nil
Duration	:	2 Hours

Special Instructions :
This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Students are not allowed to remove this question paper from the examination venue.

Students are also not allowed to write anything on the Appendix handout given

Materials permitted:

Non Programmable Scientific Calculator

Materials provided:

Appendix A (8086 Instruction Set Summary), Appendix B (ASCII table), Appendix C (8255PPI), Appendix D (8253/8254 PIT), Appendix E (8259 PIC)

Examiner(s)	:	**Mr. Steven Khoo**
Moderator	:	**Dr. Mandeep Singh**

This paper consists of 11 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEE/I)

EEE2105: INTRODUCTION TO MICROPROCESSORS
FINAL EXAMINATION: JAN2015 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

(a) Find the address range for Y0, Y3 and Y6 of the 74LS138 active-low decoder for the following design.

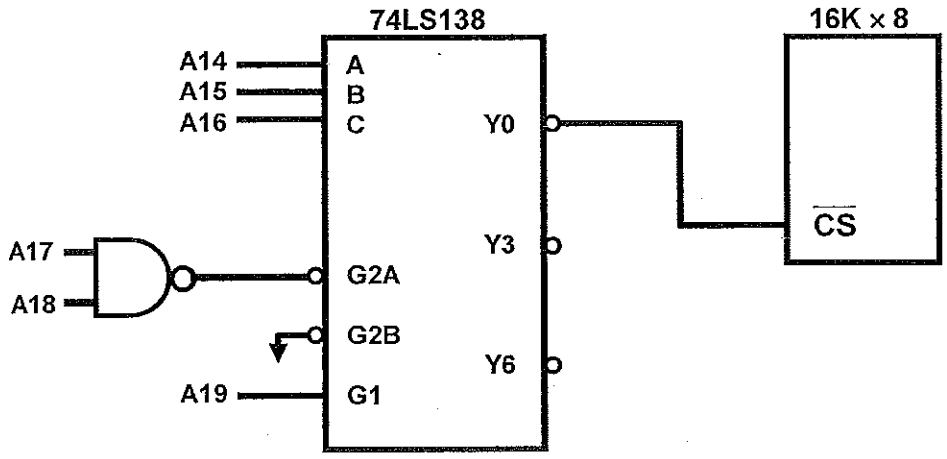


Figure 1a

(7 marks)

(b) A given 8086 microprocessor works with an 8MHz frequency. Calculate the memory bus bandwidth for the following:

(i) zero wait states

(2 marks)

(ii) two wait states

(2 marks)

Compare this with the performance of the 8088 with the same specification. What are the factors that influence the bus bandwidth?

(4 marks)

(c) Figure 1(c-1) shows a TM4100GAD8 Dynamic RAM Module pin configuration.
Figure 1(c-2) shows a TMS27PC240 FN UV Erasable PROM pin configuration.

Determine the following:

(i) total memory capacity from DRAM and EPROM in Kbits,

(4 marks)

(ii) individual memory organization,

(2 marks)

(iii) number of address pins and number of data pins of each memory module.

(4 marks)

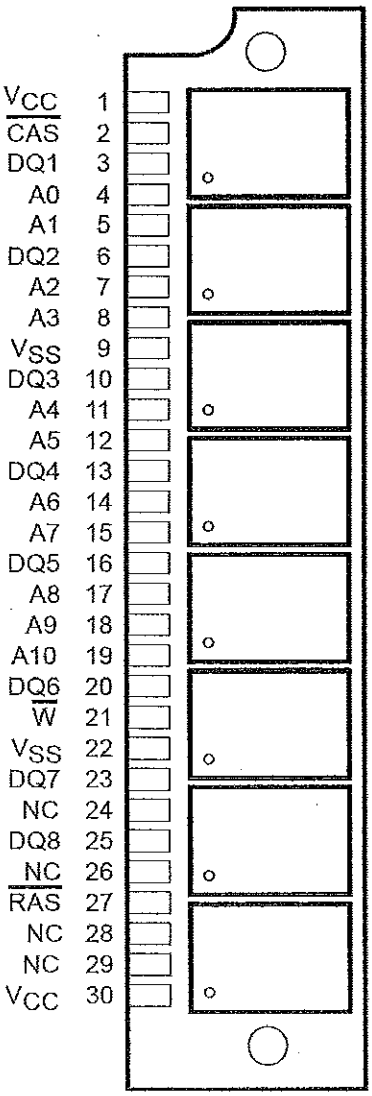


Figure 1(c-1) TM4100GAD8 Dynamic RAM Module pin configuration.

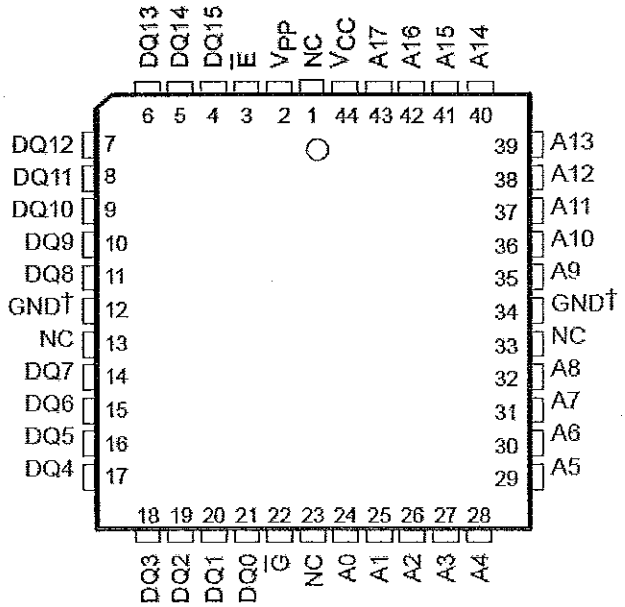


Figure 1(c-2) TMS27PC240 FN UV Erasable PROM pin configuration.

Question 2

Study and analyze the 8086 Assembly Language Codes below and answer the following questions. All values in the coding are in Hexadecimal.

Line 1	TITLE SAMPLE PROGRAM
Line 2	.MODEL SMALL
Line 3	.STACK 64
Line 4	.CODE
Line 5	.DATA
Line 6	MYCODE PROC
Line 7	MOV AX, 04
Line 8	MOV BX, 07DF
Line 9	CMP AX, BX
Line 10	JG testing1
Line 11	JLE testing
Line 12	testing1:
Line 13	ADD AL, 30
Line 14	JMP ending
Line 15	testing2:
Line 16	ADD BL, 20
Line 17	JMP ending
Line 18	ending:
Line 19	MOV AH, 4CL
Line 20	INT 21
Line 21	MYCODE ENDP
Line 22	END MYCODE

Table 2 Coding

(a) Identify THREE (3) errors in the above instructions. Briefly explain why it is incorrect and write the correct codes according to the Assembly Language.

(9 marks)

(b) What is the meaning of the instruction at Line 10 and 11? Can these instructions be reduced?

(6 marks)

(c) What is the meaning of the combined instructions at lines 18, 19 and 20?

(6 marks)

(d) Based on the assumption that all lines of codes are corrected, what is the final outcome of the above program?

(4 marks)

Question 3

(a) Describe the function of the following labels in Figure 3(a) as shown below.

(i) Label 1

(2 marks)

(ii) Label 3

(2 marks)

(iii) Label 5

(2 marks)

(iv) Label 9

(2 marks)

Name the type of microprocessor for Figure 3(a) block diagram.

(1 mark)

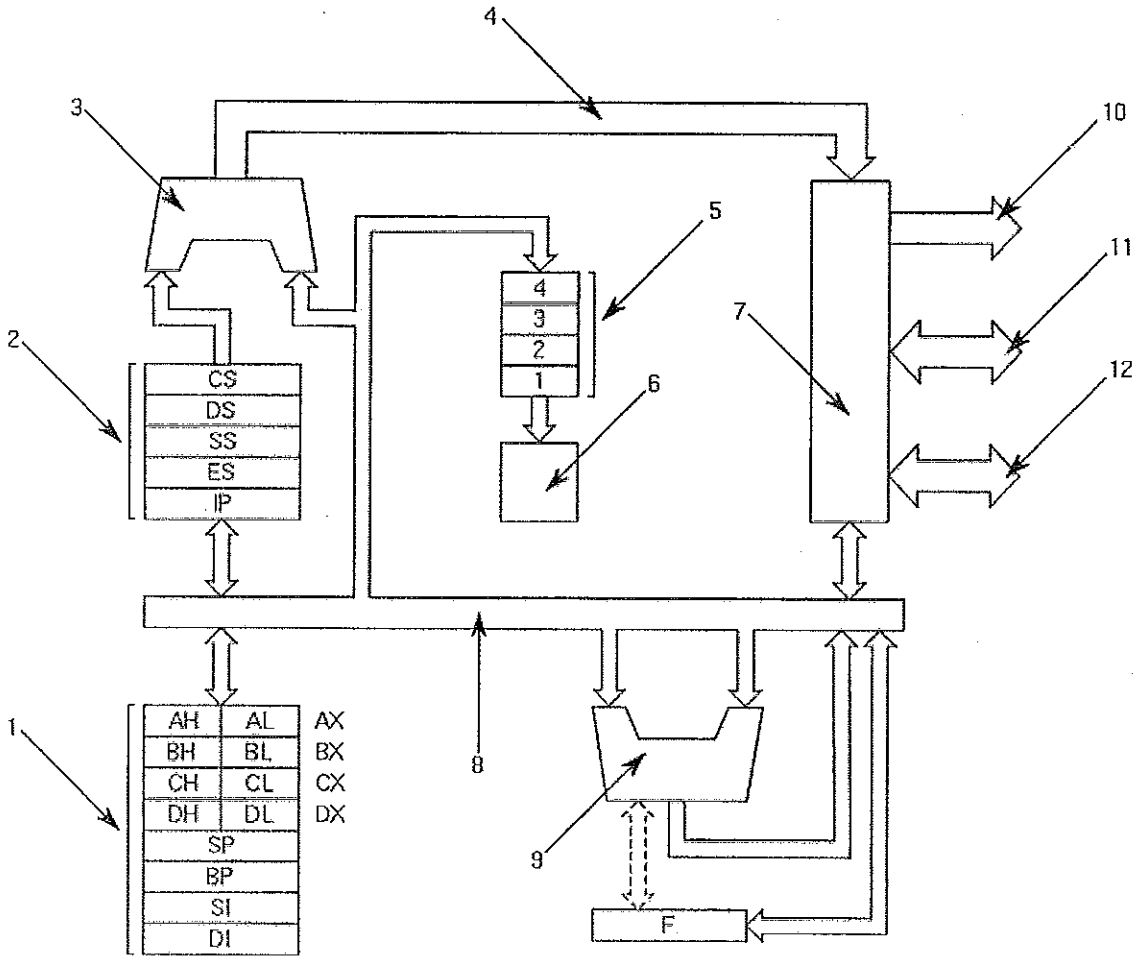


Figure 3(a)

(b) Write an 8086 program that finds out the largest number from a set of TEN 8-bit numbers stored in data segment of memory starting from address 2005H as shown below in Table 3(b). Store the result to address 200FH. Assume all ten data are unsigned numbers. The program length should be as minimum as possible.

(8 marks)

DS:	Offset	Data
0700H:	200FH	Result
0700H:	200EH	12H
0700H:	200DH	0DH
0700H:	200CH	84H
0700H:	200BH	59H
0700H:	200AH	3EH
0700H:	2009H	F1H
0700H:	2008H	48H
0700H:	2007H	7BH
0700H:	2006H	90H
0700H:	2005H	6CH

Table 3(b)

[Refer to Appendix A for 8086 instructions]

(c) The 8255 PPI is configured as shown in Figure 3(c). Write a program to count the number of '**one**' in the incoming data from port C continuously via 8255 PPI. The result will be sent to port A and port B. Also, include comments for any instruction used.

(8 marks)

Examples of incoming data and the respective action:

- 27_H (00100111_2) ⇨ send 04_H out to port A and port B
- FC_H ($\mathbf{11111100_2}$) ⇨ send 06_H out to port A and port B

[Refer to Appendix C for 8255 PPI Control Word]

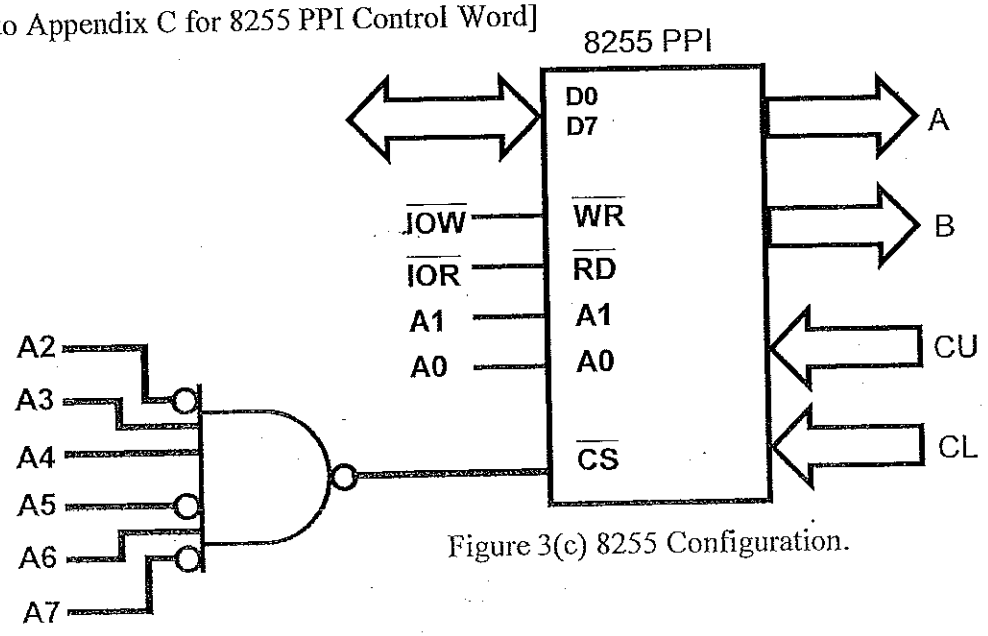


Figure 3(c) 8255 Configuration.

Question 4

(a) The 8259 PIC is configured as shown in Figure 4(a). Write a program to initialize the 8259 using the port addresses in Figure 4(a). Assume the ICW1 is 1BH, ICW2 is 38H, no ICW3 and ICW4 is 1FH. Also include comments for any instruction used.

(6 marks)

[Refer to Appendix E for 8259 PIC Control Words]

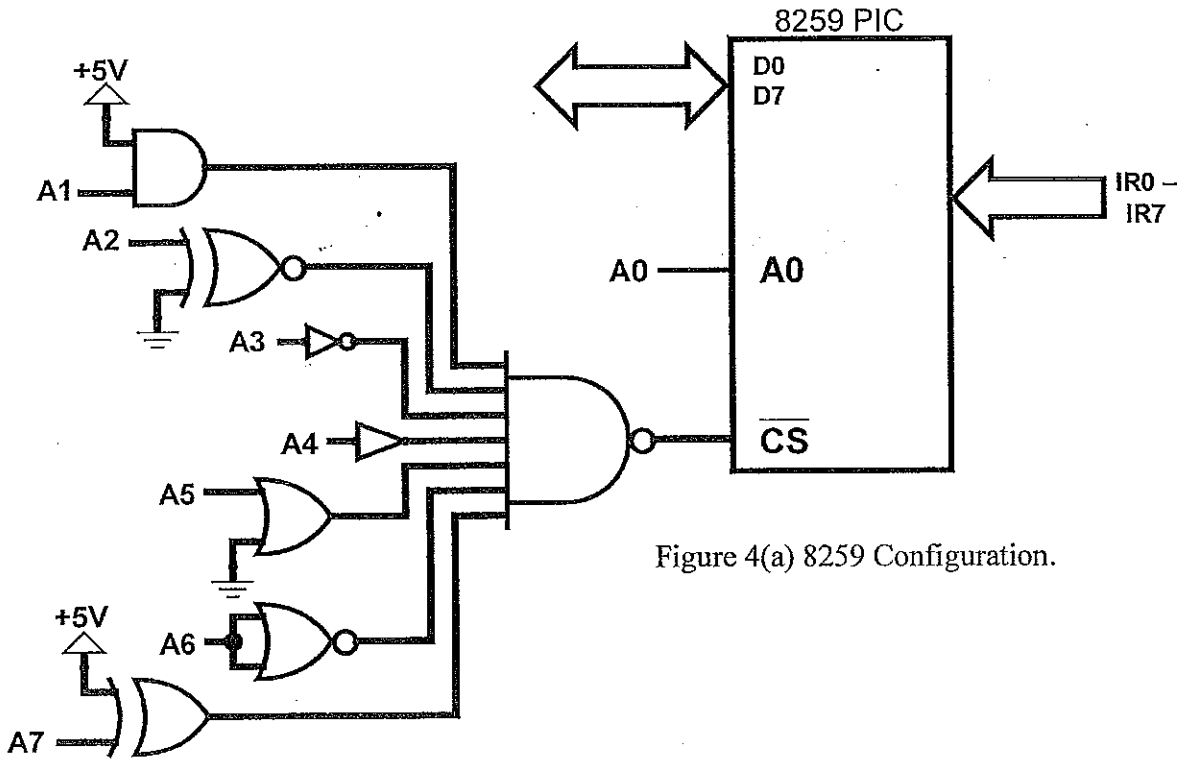


Figure 4(a) 8259 Configuration.

(b) Calculate the time delay taken for Program Q4(b) running on 8086 microprocessor at 8MHz. At a certain moment the state of an 8086 microprocessor based system is as follows: (All values are in Hexadecimal). Assume that DS register contains 0700H. Show all workings clearly for each instruction.

(13 marks)

[Refer to Appendix A for the cycle time]

	Memory															
	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
07700H	08	04	45	78	10	21	22	33	34	25	26	27	28	49	40	14
07800H	02	03	05	01	12	24	56	88	91	13	34	56	98	50	19	62
07900H	07	20	30	40	50	60	70	80	90	A0	B0	C0	D0	E0	F0	00
07A00H	1D	1C	1B	1A	19	18	55	66	47	46	45	44	43	42	41	0F
07B00H	18	19	23	48	25	26	27	58	29	31	32	35	36	37	38	39

Table 4(b) Random Address Memory

Program		
	MOV	AL, 01H
LOOP3:	MOV	BL, [0A03H]
LOOP2:	MOV	CX, [0802H]
LOOP1:	LOOP	LOOP1
	DEC	BL
	JNZ	LOOP2
	NOP	
	DEC	AL
	JNZ	LOOP3
	HLT	

Program Q4(b) Coding.

(c) A 10MHz 8086 based system is using ROM of 200ns speed. Calculate the number of wait states that the ROM selection circuitry must add if the delay due to data path and decoding circuitry (74LS244, 74LS138, and so on) is 40ns.

(6 marks)

Question 5

(a) The 8086 is at 8MHz and 3MHz for the 8237 DMA. The CPU bus cycle uses one wait state and the bus cycle for the DMA is 5 clocks. Calculate the DMA data transfer rate if the system bus is used alternately by the CPU and DMA. Express the answer in Kbytes/s.

(6 marks)

(b) A transmission system uses asynchronous serial data communication as shown in Figure 5(b) with **LSB** being transmitted first to transmit a passcode to the receiver via 8250 UART chip.

Decode the following serial data received in continuous ASCII characters message:
Incoming data:
00100110110100111111011010101100010110110101111011000011101 1

(i) What is the passcode transmitted and passcode solution?

(8 marks)

(ii) Also, calculate the total time wasted due to overhead when transmitting the above message.

(2 marks)

[Refer to Appendix B for ASCII codes]

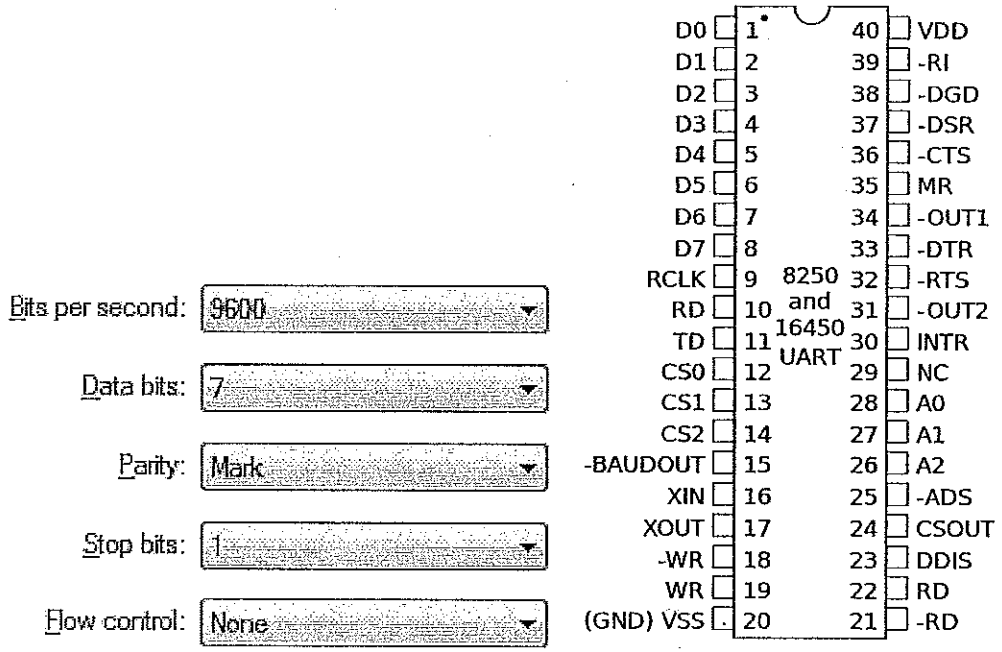


Figure 5(b) Serial communication settings.

(c) Perform the following number system transformation. Show all workings clearly.

i) $[3016.3016_{16} - 1001.1001_{16}]$ to decimal equivalent with 5 decimal points accuracy. (3 marks)

ii) $[225.225_8 \times 7_8]$ to hexadecimal equivalent with 3 hexadecimal points accuracy. (3 marks)

iii) $[01000110.0111_2 + 00110111.1001_2]$ to BCD equivalent. (3 marks)

Question 6

(a) A certain microprocessor allocates addresses 1000H to 1FFFH for RAM 1, 3000H to 5FFFH for RAM 2, 7000H to 9FFFH for I/O and C000H to FFFFH for ROM.

(i) Draw the memory map for this microprocessor. (2 mark)

(ii) Determine the total ROM & RAM capacity. (3 marks)

(iii) How many different input/output devices can the assigned I/O capacity area accommodate if an I/O device uses 3 KB of memory space?

(3 marks)

(iv) How many different input/output devices can this microchip accommodate if an I/O device uses 2 KB of memory space?

(3 marks)

(b) The 8254 PIT chip is configured as shown in Figure 6(b). CLK2 of counter 2 is 1.19318MHz and Gate2 is connected to high permanently. Counter 2 generates a periodic pulse every 30.176μs to refresh DRAM memory of the computer. Write assembly instructions to generate this periodic pulse through OUT2.

(5 marks)

[Refer to Appendix D for 8253/8254 PIT Control Word]

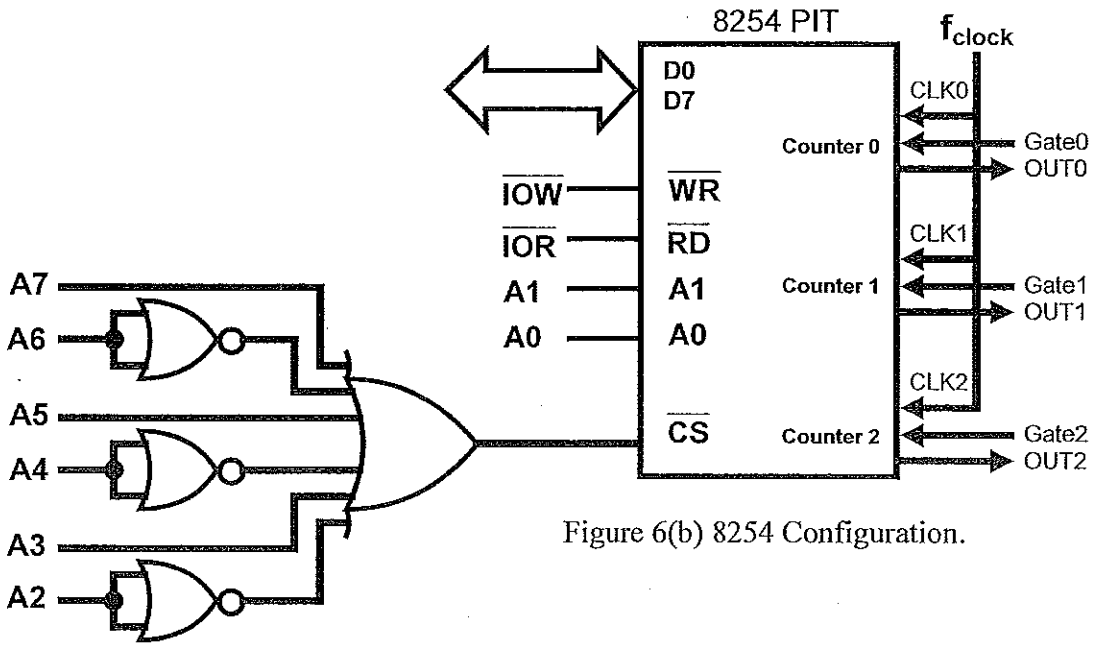


Figure 6(b) 8254 Configuration.

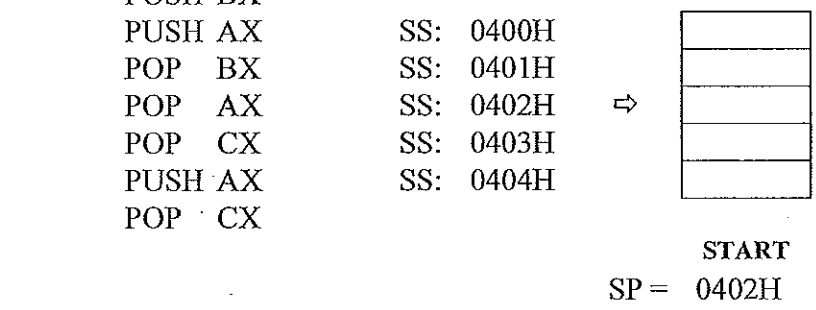
(c) Suppose that AX = 1C35H, BX = 6DBAH, CX = 789CH and SP = 0402H.

Determine the value of SP and the values of the data in the registers concerned as we progress through the following instructions. Show step-by-step after each instruction being executed using the aid of diagram as shown below to start with.

(9 marks)

```
PUSH BX
PUSH CX
PUSH BX
PUSH AX
POP  BX
POP  AX
POP  CX
PUSH AX
POP  CX
```

Stack Memory



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