

**INTI**  
**International College Penang**  
LAUREATE INTERNATIONAL UNIVERSITIES®

FINAL  
Examination Paper

(COVER PAGE)

Session : JANUARY 2015

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Programmes : DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING  
(DEED)

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Course : EEE2101: INTRODUCTION TO DIGITAL ELECTRONICS

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Date of Examination : 12 March 2015

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Time : 2:00pm – 4:00pm Reading Time: Nil

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Duration : 2 Hours

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Special Instructions :

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

**Students are not allowed to remove this question paper from the examination venue.**

Materials permitted : Non Programmable Scientific Calculator

Materials provided:

Examiner(s) : Mr. Steven Khoo

Moderator : Dr. Ooi Beng Lee

*This paper consists of 11 printed pages, including the cover page.*

**INTI INTERNATIONAL COLLEGE PENANG**

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEE/I)

**EEE2101: INTRODUCTION TO DIGITAL ELECTRONICS  
FINAL EXAMINATION: JAN2015 SESSION**

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

**Question 1**

- (a) Figure 1(a) shows the logic symbol of 74HC85 4-bit magnitude comparator with (pin numbers in parentheses). Use 74HC85 comparators to compare the magnitude of two 8-bit numbers. Show the comparators with proper interconnections. Indicate the MSB and LSB in details.

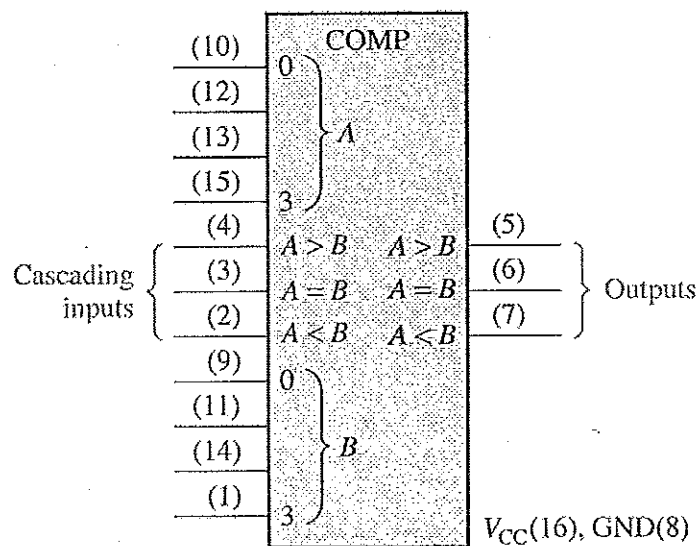


Figure 1(a)

(6 marks)

- (b) Perform the following number system transformation. Show all workings clearly.

- i)  $[3016.3016_{16} - 1001.1001_{16}]$  to decimal equivalent with 5 decimal points accuracy. (3 marks)
- ii)  $[225.225_8 \times 7_8]$  to hexadecimal equivalent with 3 hexadecimal points accuracy. (4 marks)
- iii)  $[01000110.01111_2 + 00110111.1001_2]$  to BCD equivalent. (3 marks)

(c) Design a circuit with the following requirements:

An input for tail lights both on.

An input for right turn that lets the signal "OSC" control right tail light.

An input for left turn that lets the signal "OSC" control left tail light.

Note: "OSC" will make the light flash on and off as a turn indicator.

AND and OR gates with inversion bubbles are allowed.

There are four inputs "TAIL", "RIGHT", "LEFT" and "OSC".

There are two outputs "RIGHT\_LEFT" and "LEFT\_RIGHT".

i) Draw the required logic circuit with clear labelling.

(5 marks)

ii) A new requirement is added, the flashers must over ride all other signals and make "OSC" drive both right and left tail lights. Use input "FLASH" to build on the existing design in Q1c(i).

(4 marks)

### Question 2

(a) Design a circuit to fit in the block of Figure 2(a) below that will cause the headlights of a vehicle to be turned off automatically 15s after the ignition switch is turned off, if the light switch is left on. Assume that a LOW is required to turn the lights off and the Timer block diagram is available.

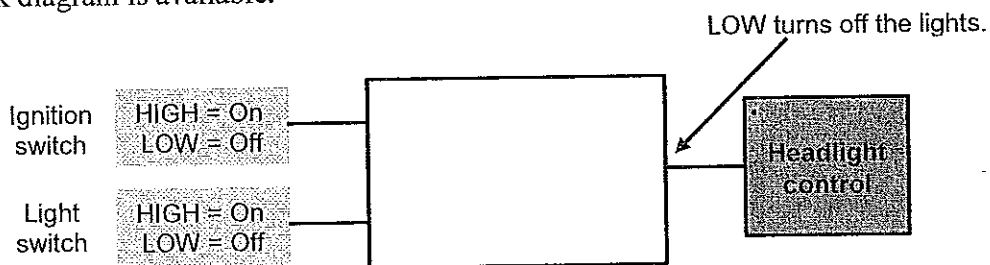


Figure 2(a)

(5 marks)

(b) Determine the input condition(s) needed to produce  $Z = 1$  in Figure 2(b).

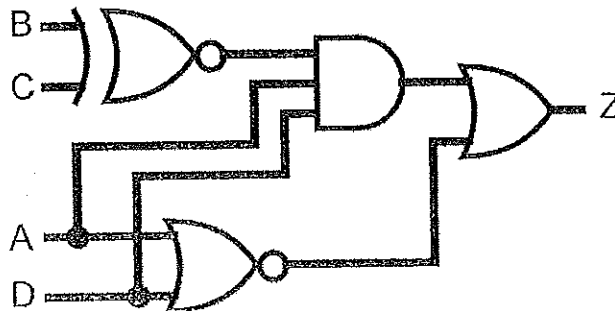


Figure 2(b)

(4 marks)

(c) Use the given Karnaugh map and Boolean algebra to obtain the minimum

i) SOP expression for the function,

$$F(K, L, M, N) = \sum (0, 2, 3, 4, 6, 8, 10, 11, 12, 14).$$

(3 marks)

ii) POS expression for the function,

$$F(A, B, C, D) = \sum (0, 1, 4, 5, 6, 7, 11, 13).$$

(3 marks)

iii) SOP expression for the function,

$$F(W, X, Y, Z) = \sum m(0, 2, 3, 5, 6, 7, 8, 9) + d(10, 11, 12, 13, 14, 15).$$

(3 marks)

(d) Figure 2(d) shows a simple DAC using an op-amp summing amplifier with binary-weighted resistors.

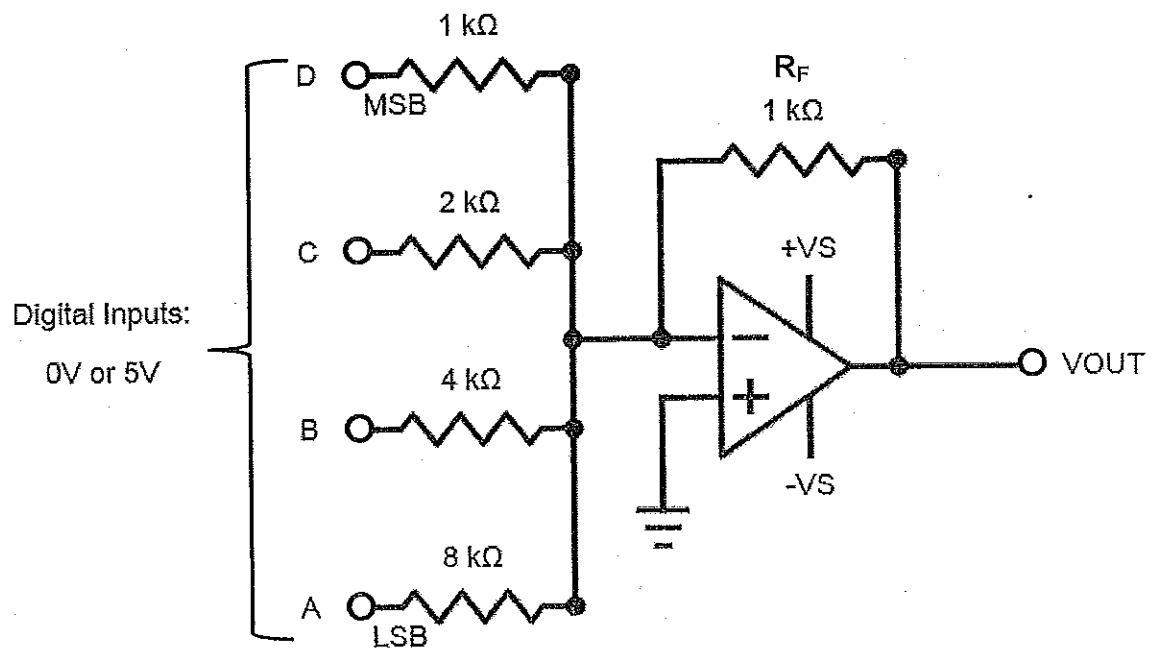


Figure 2(d)

i) Determine the weight of each input bit of Figure 2(d).

(4 marks)

ii) Change R<sub>F</sub> to 500Ω and determine the full-scale output.

(3 marks)

**Question 3**

- (a) The logic circuit of Table 3(a) generates two outputs, AB1 and AB2 that are used to activate the alarm buzzers in a particular security system as shown in the truth table below.

Inputs			Outputs	
W	X	Y	AB1	AB2
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	1	0
1	0	0	0	1
1	0	1	0	1
1	1	0	1	0
1	1	1	1	0

Table 3(a)

- i) Provide Boolean equations for outputs AB1 and AB2 in terms of W, X and Y. (2 marks)
  - ii) Draw the logic circuit to carry out this truth table with minimum number of gates. Determine which is the best implementation among NAND gates only, NOR gates only and basic logic gates (AND, OR, NOT) for this implementation. (6 marks)
- (b) Figure 3(b) below shows a 3-bit synchronous counter which is designed so that it performs a special counting sequence. Analyse its operation by determining its counting sequence. Assume that all flip-flops are initially in the 0 state. Flip-flop FF2 is MSB and FF0 is LSB. Show all workings clearly.

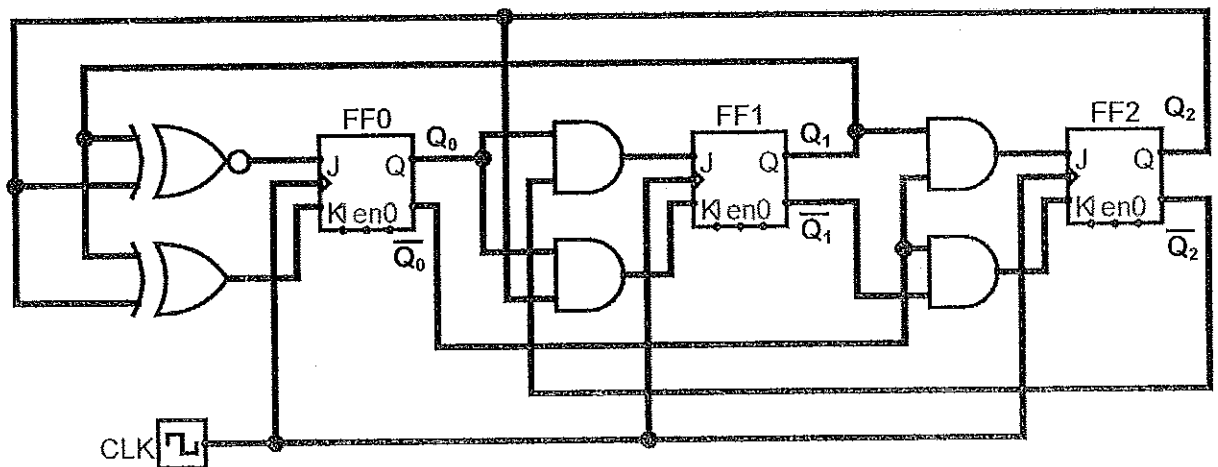


Figure 3(b)

- i) Provide the Boolean expressions from the logic circuit. (3 marks)
- ii) Provide all Karnaugh maps according to the expressions. (6 marks)
- iii) Provide the transition table/ next state table with excitation table. (4 marks)
- iv) Draw the state diagram and comment on the outcome of the states obtained. What application can this circuit be used for? (4 marks)

#### Question 4

(a) Design a synchronous 4-bit counter using positive edge-triggered JK flip-flop for MSB, T flip-flop for second bit, D flip-flop for third bit and RS flip-flop for LSB. Assume all unused states as don't care. The counter will count from  $0 \Rightarrow 3 \Rightarrow 5 \Rightarrow 7 \Rightarrow 9 \Rightarrow 0$ . Provide proper labelling for the designed logic circuit. Show all workings clearly.

- i) Provide all excitation tables used. (2 marks)
- ii) Provide the transition table/ next state table. (4 marks)
- iii) Simplify using Karnaugh map and Boolean algebra if necessary. (6 marks)
- iv) Draw the complete logic circuit diagram with proper label. (3 marks)

(b) Figure 4(b) has three inputs (A, B, C) and two outputs (Y, Z).

Table 4b(i) shows a portion of quadruple 2-input AND gates datasheet.

Table 4b(ii) shows a portion of quadruple 2-input OR gates datasheet.

Table 4b(iii) shows a portion of quadruple 2-input XOR gates datasheet.

- i) Using the datasheets given, determine the maximum propagation delay time. Show all working clearly. (6 marks)
- ii) What is minimum operating frequency that can be applied to this circuit without affecting the functionality of the circuit? (2 marks)

iii) State the function of Figure 4(b) circuit.

(2 marks)

Symbol	Parameter	Conditions	Min	Max	Units
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	$C_L = 15 \text{ pF}$ $R_L = 400\Omega$		27	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output			19	ns

Table 4b(i) AND gate

Symbol	Parameter	$R_L = 2 \text{ k}\Omega$				Units
		$C_L = 15 \text{ pF}$		$C_L = 50 \text{ pF}$		
		Min	Max	Min	Max	
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	3	11	4	15	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	3	11	4	15	ns

Table 4b(ii) OR gate

Symbol	Parameter	Conditions	$C_L = 15 \text{ pF}, R_L = 400\Omega$		Units
			Min	Max	
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	Other Input LOW		23	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output			17	ns
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	Other Input HIGH		30	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output			22	ns

Table 4b(iii) XOR gate

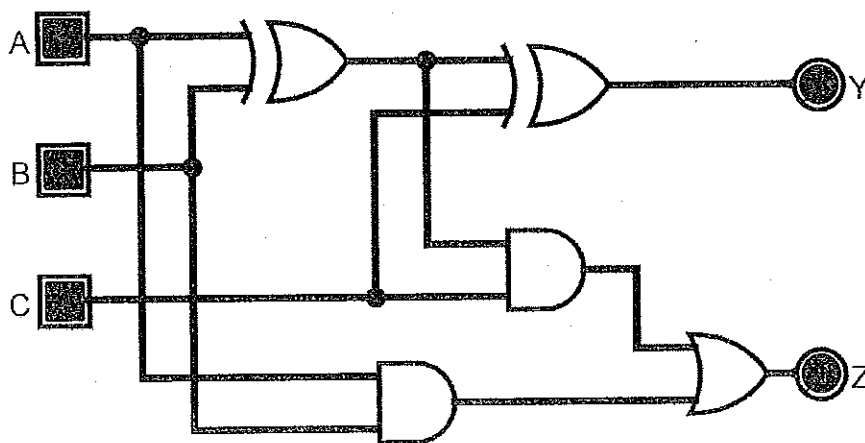


Figure 4(b)

Question 5

- (a) Figure 5(a) shows the logic symbol of 74HC154 4-bit (1-of-16) decoder with (pin numbers in parentheses). A certain application requires that a 5-bit number be decoded. Use 74HC154 decoders to implement the logic. The binary number is represented by the format  $A_4A_3A_2A_1A_0$ . Provide details explanation of the fifth bit,  $A_4$  implementation.

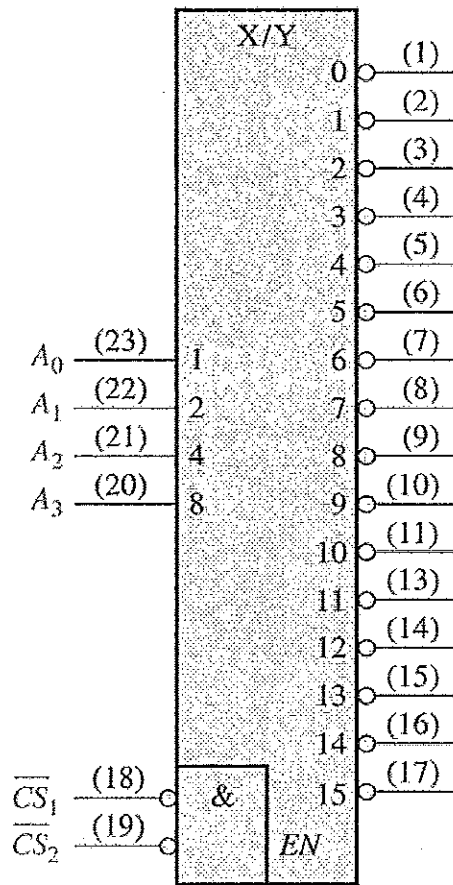


Figure 5(a)

(8 marks)

- (b) Determine the frequency of the pulse at point w, x, y and z in the circuit of Figure 5(b). Show all working clearly.

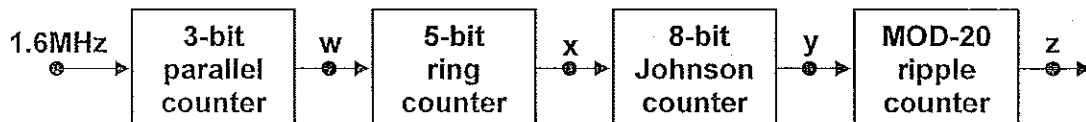


Figure 5(b)

(6 marks)

(c) Implement  $F(X,Y,Z) = \Sigma(0,3,4,5)$  using the following in the simplest form:

- i) SN7400N (2-input NAND gate) only. (4 marks)
- ii) SN74157N (2-to-1 Multiplexer) with X as select line and other logic gate(s). (3 marks)
- iii) SN74LS138N (3-to-8 Decoder) and other logic gate(s).

Inputs				Outputs							
E	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	O <sub>0</sub>	O <sub>1</sub>	O <sub>2</sub>	O <sub>3</sub>	O <sub>4</sub>	O <sub>5</sub>	O <sub>6</sub>	O <sub>7</sub>
0	X	X	X	1	1	1	1	1	1	1	1
1	0	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	0	1	1	1	1	1	1
1	0	1	0	1	1	0	1	1	1	1	1
1	0	1	1	1	1	1	0	1	1	1	1
1	1	0	0	1	1	1	1	0	1	1	1
1	1	0	1	1	1	1	1	1	0	1	1
1	1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	0

Table 5(c)(iii) 3-to-8 active-low Decoder truth table

(4 marks)

### Question 6

- (a) Table 6(a) shows the current ratings of TTL series logic gates. A 74LS04 NOT gate output is driving two Standard TTL gate inputs, three Advanced Low-Power Schottky gate inputs and one Schottky gate input as shown in Figure 6(a). Determine if there is a loading problem.

(4 marks)

TTL Series	Output Drive		Input Loading	
	I <sub>OH</sub>	I <sub>OL</sub>	I <sub>IH</sub>	I <sub>IL</sub>
74	400μA	16mA	40μA	1.6mA
74S	1.0mA	20mA	50μA	2.0mA
74LS	400μA	8mA	20μA	400μA
74AS	2.0mA	20mA	20μA	500μA
74ALS	400μA	8mA	20μA	100μA
74F	1.0mA	20mA	20μA	600μA

Table 6(a)

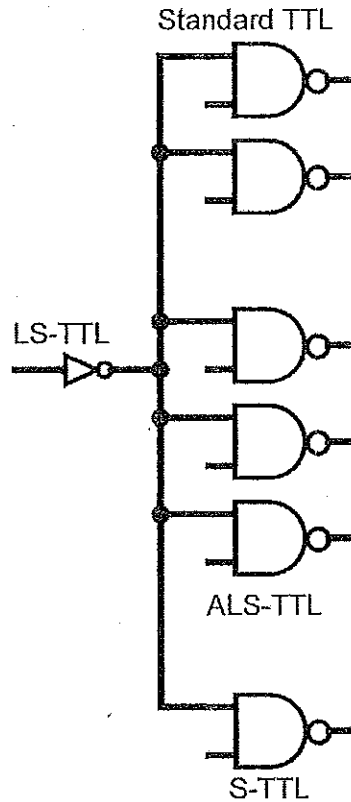


Figure 6(a)

The 74LS04 NOT gate output needs to be used to drive some 74F inputs in addition to the load inputs. How many additional 74F inputs could the output drive without being overloaded?

(4 marks)

- (b) A technician uses a logic probe to determine the conditions at the various IC pins as shown in Figure 6(b) and the results are recorded in Table 6(b). Examine these results and determine if the circuit is working properly. If not, identify some of the possible faults as details as possible that can cause this.

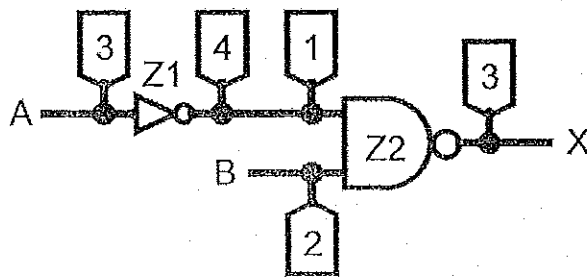


Figure 6(b)

Pin	Condition
Z1-3	Pulsing
Z1-4	LOW
Z2-1	LOW
Z2-2	HIGH
Z2-3	HIGH

Table 6(b)

(6 marks)

(c) Figure 6(c) shows a BCD counter that produces a four-bit output representing the BCD code for the number of pulses that have been applied to the counter input. For example, after four pulses have occurred, the counter outputs are DCBA =  $0100_2 = 4_{10}$ . The counter resets to 0000 on the tenth pulse and starts counting over again. In other words, the DCBA outputs will never represent a number greater than  $1001_2 = 9_{10}$ . The logic circuit that produces a HIGH output whenever the count is 2, 3, 7 or 9. Take advantage of the don't-care conditions. Show all working steps clearly.

- i) Provide a truth table for the logic circuit. (3 marks)
- ii) Simplify the Boolean expression using Karnaugh map and/or Boolean Algebra to the simplest form. (3 marks)
- iii) Design the logic circuit using minimum number SN7402 (2-input NOR gates) only. (5 marks)

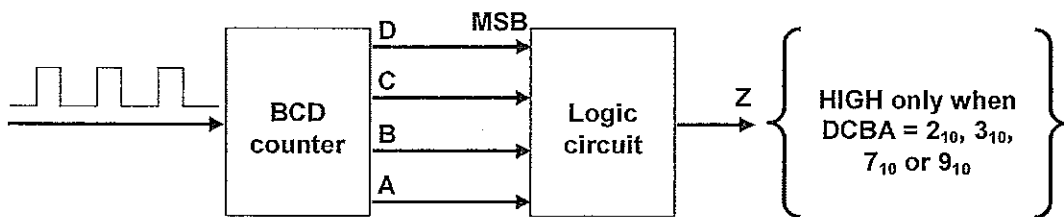


Figure 6(c)

– THE END –

EEE2101(F)/Jan15/Steven Khoo/2/1/15

