INTI International College Penang
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FINAL
Examination Paper
(COVER PAGE)

Session	:	JANUARY 2015
Programmes	:	**DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING (DEED)**
Course	:	**EEE1105: CIRCUIT THEORY & ELECTRONIC DEVICES**
Date of Examination	:	9 March 2015 (Monday)
Time	:	11:00am – 1:00pm Reading Time: Nil
Duration	:	2 Hours
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Students are not allowed to remove this question paper from the examination venue.

Materials permitted : Non Programmable Scientific Calculator

Materials provided: Graph paper with diode characteristic (for Question 3(C))

Examiner(s) : **Ms. Shalyn Lim Sheue Hui**

Moderator : **Dr. Cheah Kean Seng**

This paper consists of 12 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)

EEE 1105: CIRCUIT THEORY & ELECTRONIC DEVICES
FINAL EXAMINATION: JAN 2015 SESSION

Instructions: This paper consists of SIX (6) questions. Answer any FOUR (4) questions in the answer booklet provided. All questions carry equal marks.

Question 1

(a) With reference to Figure Q1(a).

(i) Calculate the currents I_1, I_2, and I_3. (3 marks)

(ii) Determine the values of the unknown resistors R_2 and R_3. (3 marks)

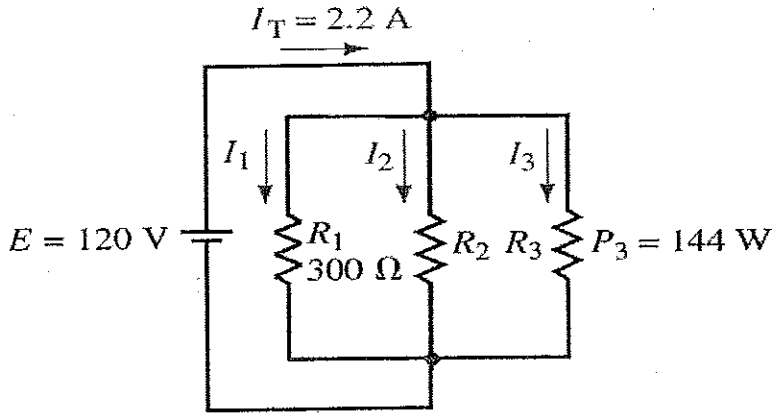

Figure Q1(a)

(b) Refer to Figure Q1(b) ,using nodal analysis calculate

(i) V_1 and V_2.

(5 marks)

(ii) I_1 and I_4.

(3 marks)

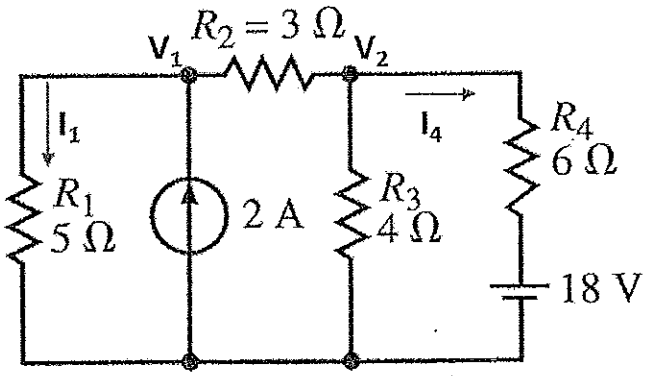

Figure Q1(b)

(c) For the circuit shown in Figure Q1(c),calculate

(i) Thevenin resistance R_{Th}.

(2 marks)

(ii) open terminal voltage V_{Th} using Thevenin's theorem.

(3 marks)

(iii) short circuit current I_N using Northan's theorem

(4 marks)

(iv) the maximum power transfer to the load , R across terminal a and b.

(2 marks)

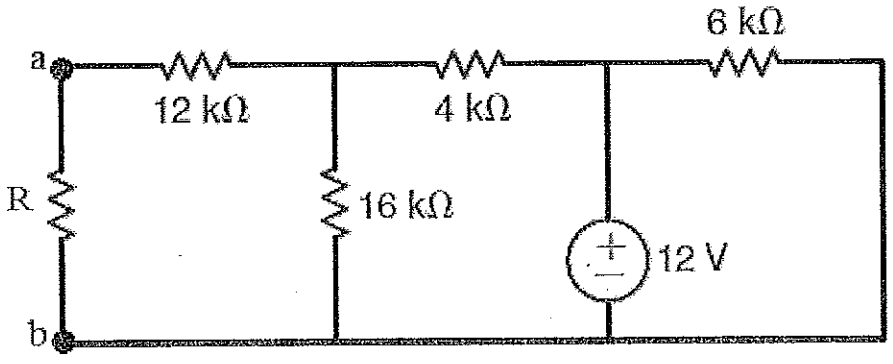

Figure Q1(c)

Question 2

(a) Voltage and current are out of phase by 40°, and voltage lags. Using current as the reference, sketch the phasor diagram and the corresponding waveforms.

(3 marks)

(b) For the network of Figure Q2(b),calculate
[* answer in polar form]

(i) the total impedance Z_T..

(3 marks)

(ii) the voltage V_2 and the current I_L.

(6 marks)

(iii) the power factor of the network.

(2 marks)

(iv) the active and reactive power of the network.

(3 marks)

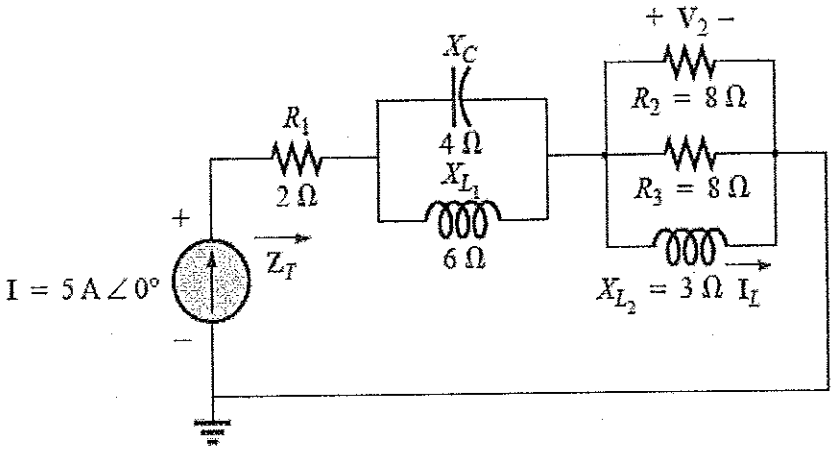

Figure Q2(b)

(c) Refer to the resonant network in Figure Q2(c),

(i) Find the value of L if the resonant frequency is 1800 Hz.

(2 marks)

(ii) Find the magnitude of the current I_{rms} at resonance.

(3 marks)

(iii) Find the Q factor of the network.

(3 marks)

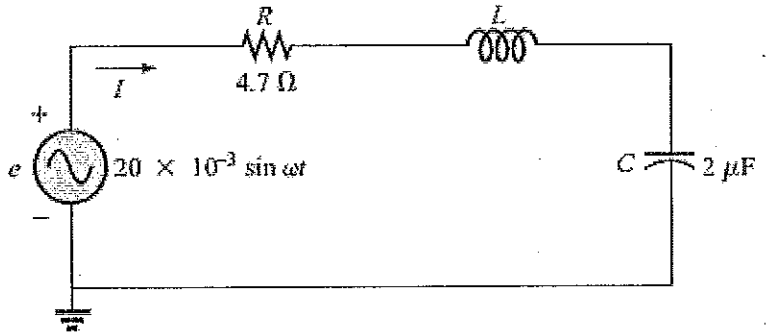

Figure Q2(c)

Question 3

(a) Sketch and label the output waveform for the clamper circuit shown in Figure Q3(a).Assume ideal diode and $RC >> \frac{T}{2}$.

(3 marks)

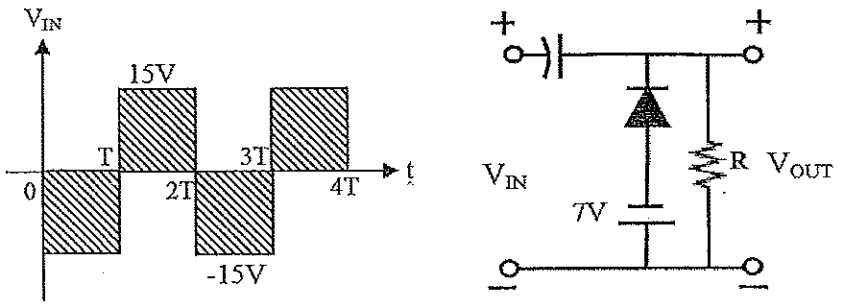

Figure Q3(a)

(b) Refer to the half wave rectifier circuit shown in Figure Q3(b),

(i) sketch the output waveform across R_L with proper labeling.

(2 marks)

(ii) calculate the average output voltage.

(4 marks)

(iii) what minimum PIV rating must the diodes have?

(2 marks)

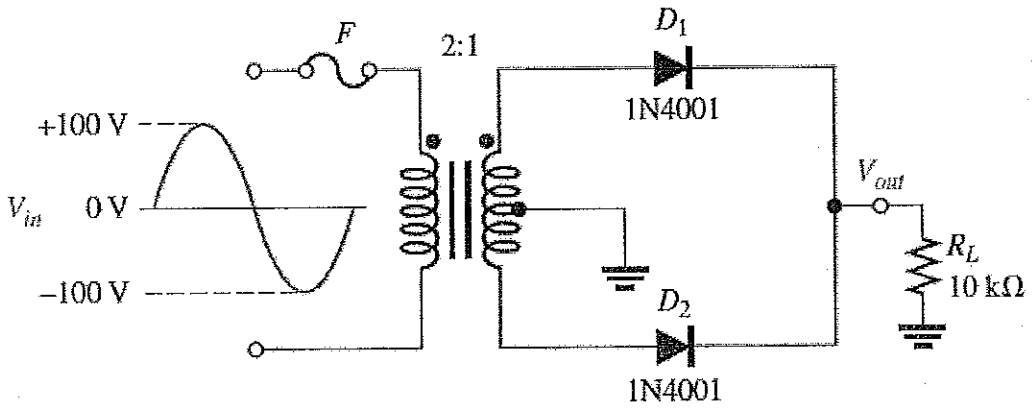

Figure Q3(b)

(c) For the series diode configuration of Figure Q3(c) (i) and the characteristic in Figure Q3(c) (ii) , determine

(i) V_{DQ} and I_{DQ} using the given graph paper with diode characteristic **(please attach with the answer script)**.

(7 marks)

(ii) V_R

(2 marks)

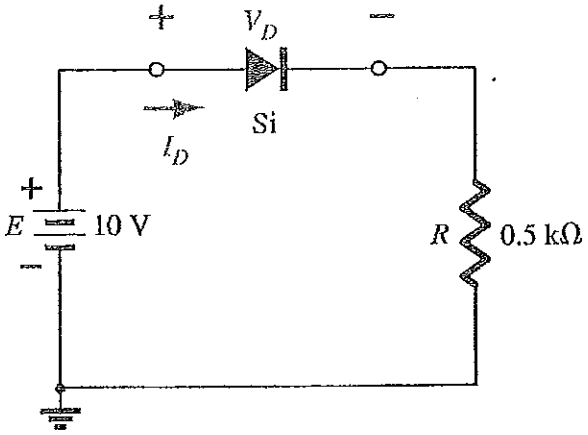

Figure Q3(c) (i)

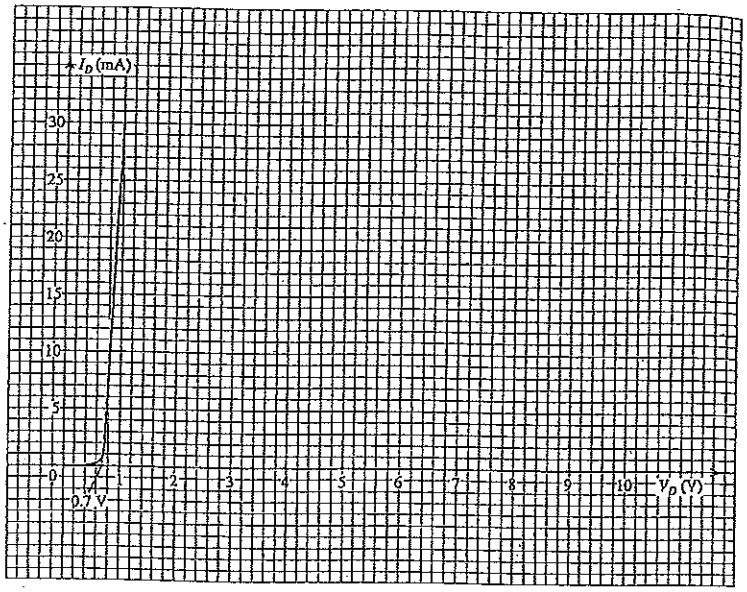

Figure Q3(c) (ii)

(d) Determine the power dissipation of the resistors and zener diode in Figure Q3(d). Given $V_S = 15V$, $R_S = 560\Omega$, $R_L = 2k\Omega$, $V_Z = 10V$. Assume the zener diode is ideal. Also, calculate the total power delivered by V_S.

(6 marks)

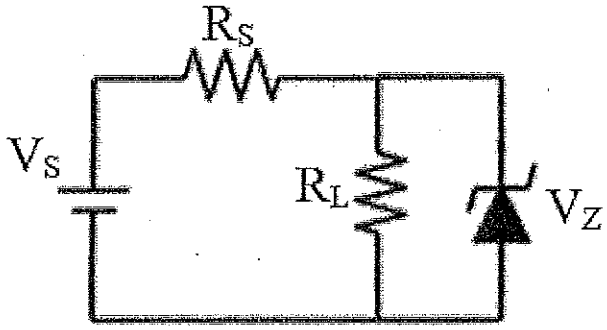

Figure Q3(d)

Question 4

(a) Briefly describe how to operate BJT as an amplifier.

(3 marks)

(b) The biasing circuit of Figure Q4 (b) has current gain, $\beta=200$. Assume $V_{BE}=0.7V$.

(i) Calculate the quiescent operating point.

(5 marks)

(ii) Sketch the load line with the proper labeling of saturation and cut off point.

(4 marks)

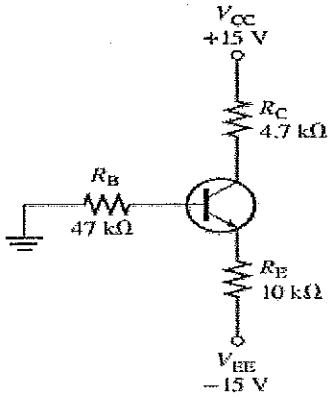

Figure 4(b)

(c) Given the information provided in Figure Q4(c), assume determine

(i) β (3 marks)

(ii) Vcc (3 marks)

(iii) R_B (2 marks)

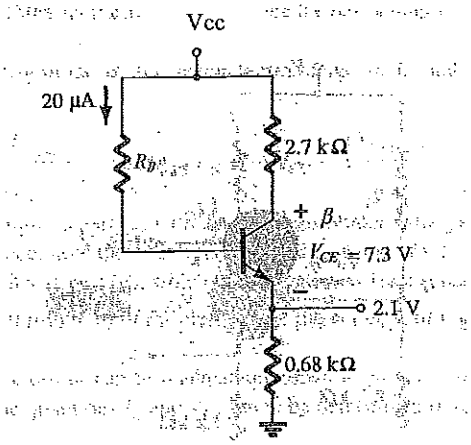

Figure Q4(c)

(d) Given the voltage-divider configuration network shown in Figure Q4(d). By using exact method, calculate

(i) I_C (4 marks)

(ii) V_{CE} (2 marks)

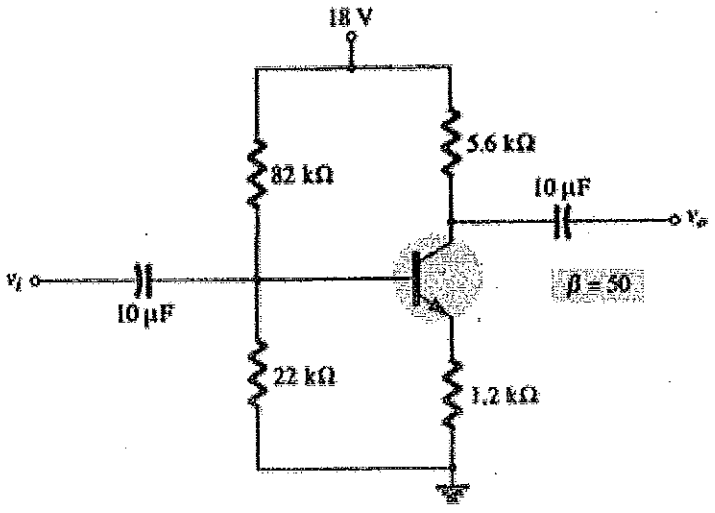

Figure Q4(d)

Question 5

(a) Sketch the construction of D-MOSFET and E-MOSFET (n-channel). What is the difference between the operation of D-MOSFET and E-MOSFET?

(5 marks)

(b) For the JFET biasing network in Figure Q5(b),

(i) identify the type of network configuration.

(2 marks)

(ii) determine I_{DQ} and V_{GSQ}.

(5 marks)

(iii) determine V_{DS}.

(2 marks)

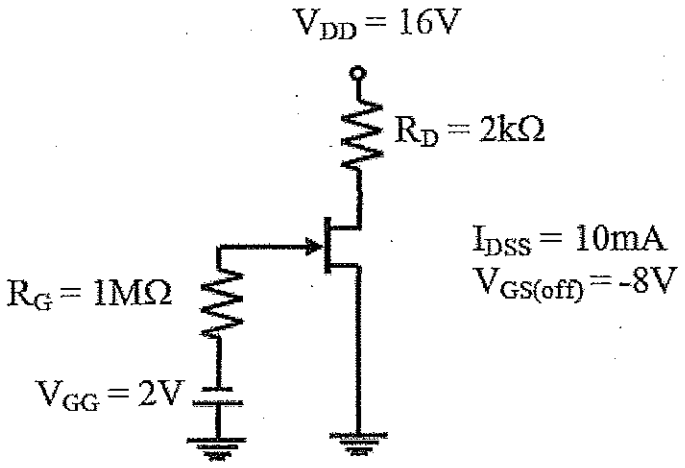

Figure Q5(b)

(c) Find V_{GS} and V_{DS} for the E-MOSFET circuit in Figure Q5(c). Datasheet information is listed with the circuit.

(7 marks)

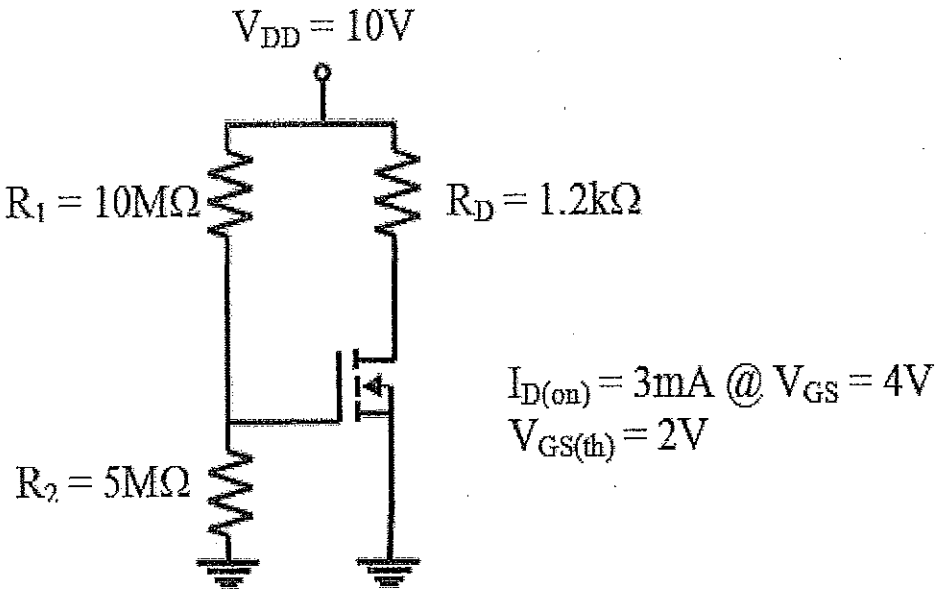

Figure Q5(c)

(d) Sketch the transfer characteristics for an n-channel enhancement type MOSFET from the drain characteristic given in Figure Q5 (d).

(4 marks)

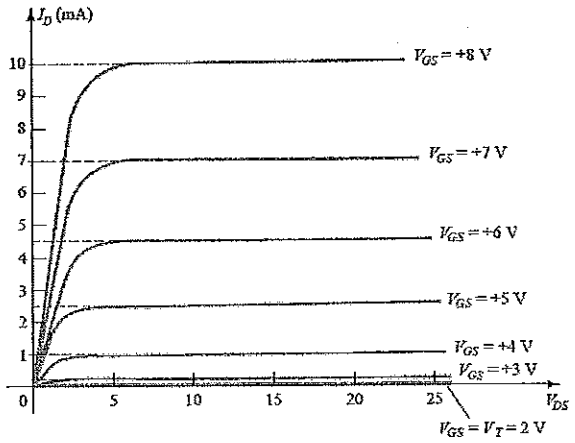

Figure Q5(d)

Question 6

(a) Construct the block diagram of a basic DC voltage power supply with ac input voltage. Describe the function and sketch of output waveform of each module.

(9 marks)

(b) For the network of Figure Q6(b),calculate

(i) the overall active, reactive and apparent power.

(4 marks)

(ii) the power factor.

(2 marks)

(iii) the total current , I_s.

(3 marks)

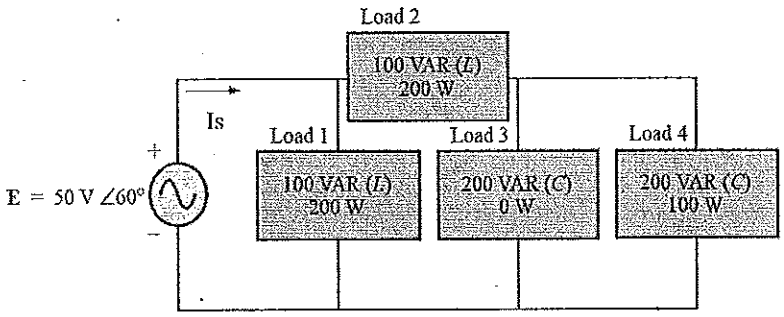

Figure Q6(b)

(c) The base bias circuit in Figure Q6 (c) is subjected to a temperature variation from 0°C to 70°C. The β decrease by 50 percent at 0°C and increase by 75 percent at 70°C from its nominal value of 110 at 25°C. What are the % of changes in I_C over the temperature change from 0°C to 70°C?

(7 marks)

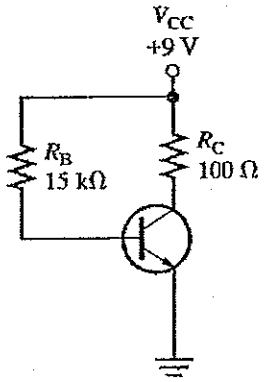

Figure Q6(c)

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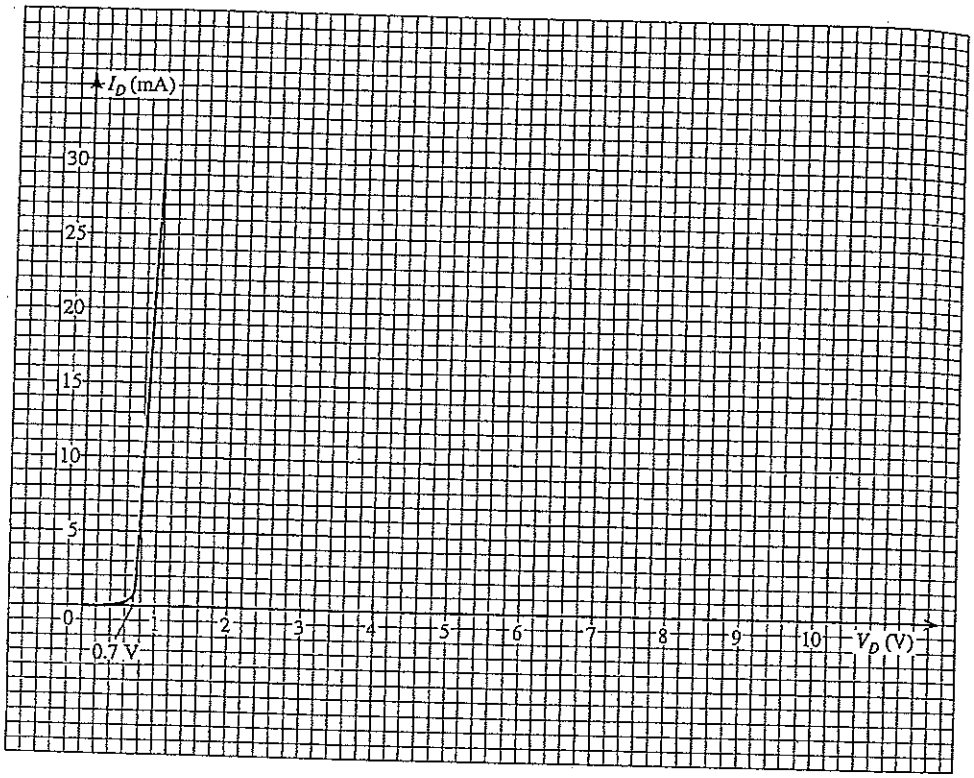
I_D (mA)
30
25
20
15
10
5
0
1
2
3
4
5
6
7
8
9
10
V_D (V)
0.7 V