INTI
INTERNATIONAL COLLEGE PENANG (507232-U)
LAUREATE INTERNATIONAL UNIVERSITIES

FINAL
Examination Paper

(COVER PAGE)

| | | |
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| Session | : | JAN 2013 |
| Programme | : | DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING |
| Course | : | **EEE 2105: INTRODUCTION TO MICROPROCESSORS** |
| Date of Examination | : | 6 March 2013 |
| Time | : | 11a.m. – 1p.m. Reading Time : Nil |
| Duration | : | 2 Hours |
| Special Instructions | : | |

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

**Students are not allowed to remove the question papers from the examination venue.**

Materials permitted :

NON-PROGRAMMABLE SCIENTIFIC CALCULATOR

Materials provided :

APPENDIX A (8086 Instruction Set Summary), APPENDIX B (ASCII Table), APPENDIX C (8255 PPI) and APPENDIX D (8253/8254 PIT)

Examiner(s) : **STEVEN KHOO**

Moderator : **CHAN TSE WEI**

*This paper consists of 7 printed pages, including the cover page.*

# INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEE/I)

## EEE2105: INTRODUCTION TO MICROPROCESSORS
## FINAL EXAMINATION: JAN2013 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

### Question 1

(a) Perform the following number system transformation. Show all workings clearly.

(i) $41.6875_{10}$ to binary

(3 marks)

(ii) $CAFE.BABE_{16}$ to octal

(4 marks)

(b) Give ONLY one line alternative instruction that will perform the same outcome for each of the following instructions:

(i) XOR AL, AL

(2 marks)

(ii)
```
MOV AL, 01H
MOV BL, 02H
MUL BL
```

(2 marks)

(iii) OR AX, 0FFH

(2 marks)

(iv)
```
MOV BL, CL
MOV CL, AL
MOV AL, BL
```

(2 marks)

(c) Find the organization and bit capacity of the following memory chips.

(i) 8 address pins, CAS, RAS, 8 data pins DRAM

(3 marks)

(ii)

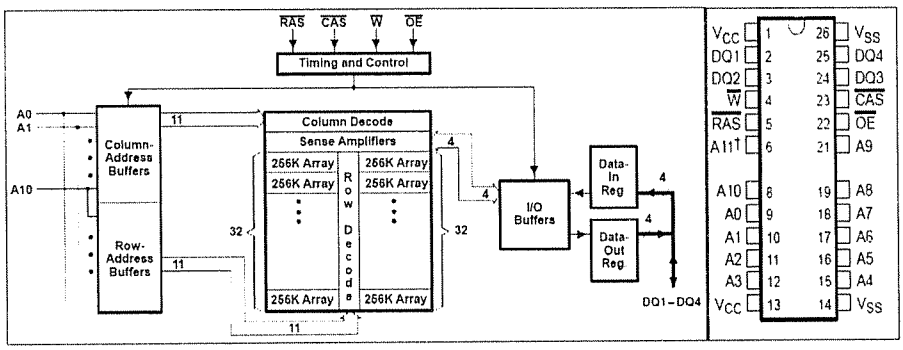


Figure 1c(ii) Block diagram and pinout of DRAM chip. (3 marks)

(d) Comment on the validity of the following instructions. Explain if it is not valid.
(i) MOV BX, [AX]

(ii) MOV BL, [BP][BX][DI][SI] 22H

(4 marks)

**Question 2**

(a) Explain the difference between RCL and ROL instructions. Illustrate how a microprocessor rotates twice the data 5AH using these types of instruction with the aid of diagrams. Assume that the data is in register AL and carry flag (CF) is reset initially.

(8 marks)

(b) At a certain moment the state of an 8086 microprocessor based system is as follows: (All values are in Hexadecimal)

**Registers**

| | H | L |
|---|---|---|
| AX | 2C | 12 |
| BX | 00 | 14 |
| CX | 10 | 01 |
| DX | 2B | 33 |
| CS | 01 | 00 |
| DS | 80 | 00 |
| SS | 40 | 10 |
| ES | 61 | 20 |
| BP | 00 | 1F |
| SP | 01 | 08 |
| IP | 07 | 00 |
| SI | 21 | 34 |
| DI | FF | FF |

**Memory**

| | |
|---|---|
| 8000B | 12 |
| 8000A | 34 |
| 80009 | 56 |
| 80008 | 78 |
| 80007 | 9A |
| 80006 | BC |
| 80005 | DE |
| 80004 | F0 |
| 80003 | 21 |
| 80002 | 43 |
| 80001 | 09 |
| 80000 | 67 |
| 7FFFF | 54 |
| 7FFFE | DF |
| 7FFFD | 3C |

| | |
|---|---|
| 4010E | 6F |
| 4010D | 2D |
| 4010C | C1 |
| 4010B | 25 |
| 4010A | 3F |
| 40109 | 12 |
| 40108 | FF |
| 40107 | FC |
| 40106 | E1 |
| 40105 | 10 |
| 40104 | 00 |
| 40103 | 36 |
| 40102 | 21 |
| 40101 | 88 |
| 40000 | 99 |

Table 2(b) Registers & Memory.

(i) What of the physical address of the top of the stack?

(2 marks)

(ii) Draw a memory map for the 8086 microprocessor, indicating clearly the start and end addresses of the segments including unused areas.

(4 marks)

(iii) Provide the registers and memory locations that are affected, and their new values after the execution of ADD [BX – 0AH], AX, also state the number of bytes used for this instruction.

(6 marks)

(c) Assume that AX = 0500H and BX = 0005H. Will the division operation successfully take place when the following commands execute? Justify your answer.

DIV BL

Operation (byte): AL = AX ÷ operand, AH = remainder

(5 marks)

**Question 3**

(a) Calculate the time delay taken for Program 3(a) running on 8086 microprocessor at 10MHz. Show all workings clearly for each instruction.

(6 marks)

```
        MOV  CL, 04H
        AND  [1234H], BX
LOOP1:  INC  DL
        DEC  CL
        JNZ  LOOP1
        JMP  LOOP2
        ADD  AL, AL
LOOP2:  HLT
```

Program 3(a) Coding.

[Refer to APPENDIX A for the cycle time and bytes count]

(b) Also, calculate the number of bytes used to store Program 3(a) in the memory location. Show all working clearly for each instruction.

(6 marks)

[Refer to APPENDIX A for the cycle time and bytes count]

(c) Referring to Program 3(a), the equivalent machine code for JNZ LOOP1 is 75 FA. If JNZ operation code is 75, explain how the LOOP1 is equivalent to FA. Justify your answer with the aid of diagram. Show all workings clearly.

(5 marks)

[Refer to APPENDIX A for the cycle time and bytes count]

(d) Differentiate the following arithmetic instructions with the aid of calculation. Assuming AX = 53FCH and BX = 7A86H. Show all workings clearly including the result.

(i) MUL BL

(4 marks)

(ii) IMUL BH

(4 marks)

Operation (byte): AX = AL × operand

Operation (word): DX:AX = AX × operand

**Question 4**

(a) The 8255 PPI is configured as shown in Figure 4(a).

(i) Find the respective addresses for the I/O ports and the control register. Thus, program the PPI to set PC5 to high. Also include comments for any instruction used.

(6 marks)

(ii) Design approximately 1.5ms delay using the below DELAY subroutine program with a clock frequency of 5MHz. Also, provide the actual time delay of your design. Show all workings clearly.

```
        MOV CX, N
BACK:   NOP
        LOOP BACK
```

Program 4(a) DELAY subroutine.

(7 marks)

(iii) Write a program to generate a square wave of 25% duty cycle continuously by using bit 1 port C. Assume that the DELAY subroutine program is 1.5ms as designed in Q4(a)(ii) above. Also include comments for any instruction used.

(5 marks)

[Refer to Appendix C for 8255 PPI Control Word]

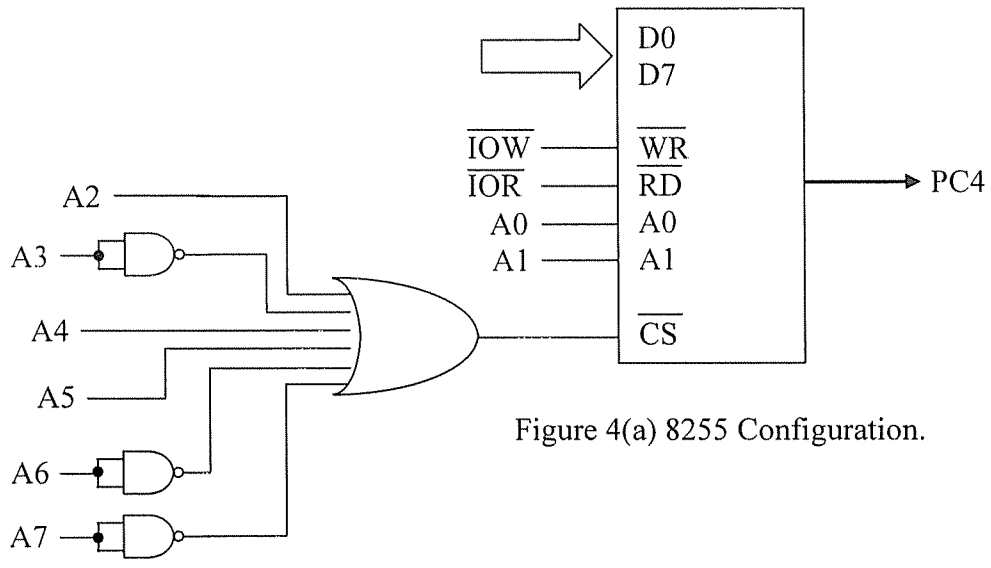


Figure 4(a) 8255 Configuration.

(b) Assume SP = FF2EH, AX = 1239H, BX = F53CH, CX = 123FH
With the aid of a memory map, show the content of stack and stack pointer after the execution of the following sequence of instructions:

```
PUSH AX
PUSH BX
PUSH CX
```

(3 marks)

(c) A transmission system uses asynchronous serial data communication as shown below in Figure Q4(c) via 9600 bps speed. What is the character and parity transmitted? Also, calculate how long it takes to transfer 2 pages with 80 × 25 characters.

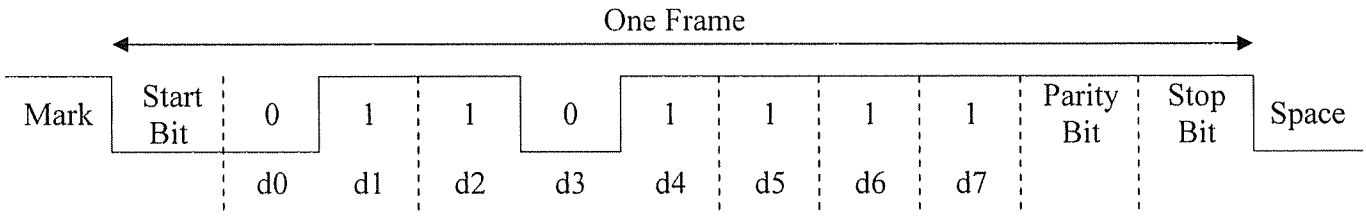


Figure Q4(c) Data Frame.

(4 marks)

[Refer to Appendix B for ASCII Codes]

**Question 5**

(a) With the aid of a suitable diagram, illustrate step-by-step how DMA can be used to speed up CPU operation during the transfer of data from memory to an I/O device.

(11 marks)

(b) The bus cycle of the 8086/88 microprocessors consists of at least four clock periods, namely $T_1$, $T_2$, $T_3$ and $T_4$. Discuss in details what is happening in each T-state for a read bus cycle of memory in 8088.

(9 marks)

(c) Pin $\overline{CS}$ of a given 8253/8254 is activated by binary address A7 – A2 = 101010. Find the port addresses assigned to this 8253/8254 and the configuration for this PIT if 0011 0110 is written into the control register.

```
MOV  AL, 00110110
OUT  CONTREG, AL
```

(5 marks)

[Refer to Appendix D for 8253/8254 PIT Control Word]

**Question 6**

A certain microprocessor allocates addresses 1000H to 1FFFH for RAM 1, 3000H to 5FFFH for RAM 2, 7000H to 9FFFH for I/O and C000H to FFFFH for RAM.

(a) Draw the memory map for this microprocessor.

(1 mark)

(b) Determine the total ROM & RAM capacity.

(3 marks)

(c) How many different input/output devices can the assigned I/O capacity area accommodate if an I/O device uses 3 KB of memory space?

(2 marks)

(d) How many different input/output devices can this microchip accommodate if an I/O device uses 2 KB of memory space?

(4 marks)

(e) Using combination of logic gates and decoders, design the address decoding circuitry for the above memory and I/O devices. All design steps must be shown. All devices, memory chips and buses involved must be included and labeled.

(15 marks)

**– THE END –**

*EEE2105(F)/Jan13/Steven Khoo/10/01/13*