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FINAL
Examination Paper

(COVER PAGE)

Session : JANUARY 2013

Programmes : Diploma in Electrical and Electronic Engineering (DEEI)

Course : **ELECTRONIC DEVICES AND CIRCUIT THEORY 2 (EEE1103)**

Date of Examination : 7 March 2013

Time : 11 a.m. – 1p.m. Reading Time: Nil

Duration : 2 Hours

Special Instructions :

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Students are not allowed to remove this question paper from the examination venue.

Materials permitted : Non-programmable scientific calculator

Materials provided: NIL

Examiner(s) : **Chan Tse Wei**

Moderator : Cheah Kean Seng

This paper consists of 2 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)

**EEE1103 : ELECTRONIC DEVICES AND CIRCUIT THEORY 2
FINAL EXAMINATION : JANUARY 2013 SESSION**

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks. The marks allocated to each sub-question are shown in square brackets at the right-hand margin.

Question 1

- a. Why common collector circuit and common emitter circuit with step down transformer are very popular in power amplifier design? [4]
- b. Figure-Q1(b) shows an AC load line of a class A power amplifier powered by a 20V DC voltage supply.

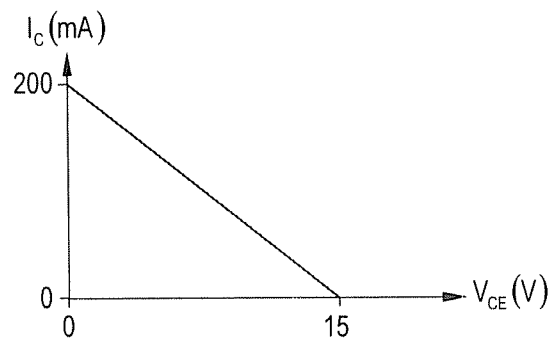


Figure-Q1(b)

- i. State the ideal quiescent point, V_{CEQ} and I_{CQ} for the power amplifier. [2]
- ii. Determine the ideal maximum AC output power of the power amplifier. [4]
- iii. Determine the ideal DC input power of the power amplifier. [3]
- iv. Determine the ideal maximum efficiency of the power amplifier. [3]

- c. Figure-Q1(c) shows an emitter follower class A power amplifier.

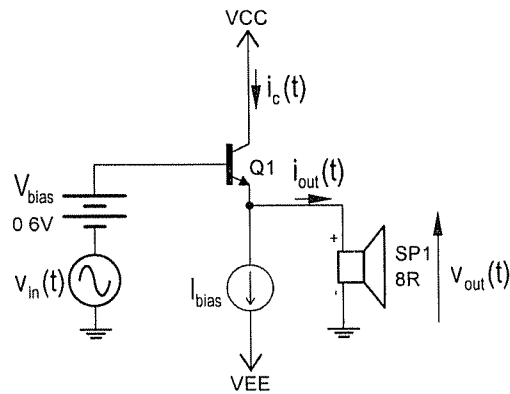


Figure-Q1(c)

- i. State the purpose of the bias voltage source, V_{bias} in the power amplifier circuit. [2]
- ii. Assume that $v_{in}(t)$ is a 1kHz sinewave, $|VCC| = |VEE|$, $V_{CE(sat)} = 0.2V$ and 10W of average AC power is to be delivered to the 8Ω speaker, SP1. Calculate suitable values of VCC and I_{bias} . [5]
- iii. Determine the power delivered by VCC . [2]

Question 2

Figure-Q2 shows a capacitively coupled multistage amplifier circuit.

Transistors Q1 and Q2 have the following AC parameters:

$$h_{ie} = 1\text{k}\Omega, h_{fe} = 100, h_{oe} = 25\mu\text{S}$$

Resistors R_1, R_2, R_5 and R_6 have resistances very much exceeding $20\text{k}\Omega$.

Assume capacitors C_1, C_2, C_3 and C_4 have negligible reactances for all operating frequencies.

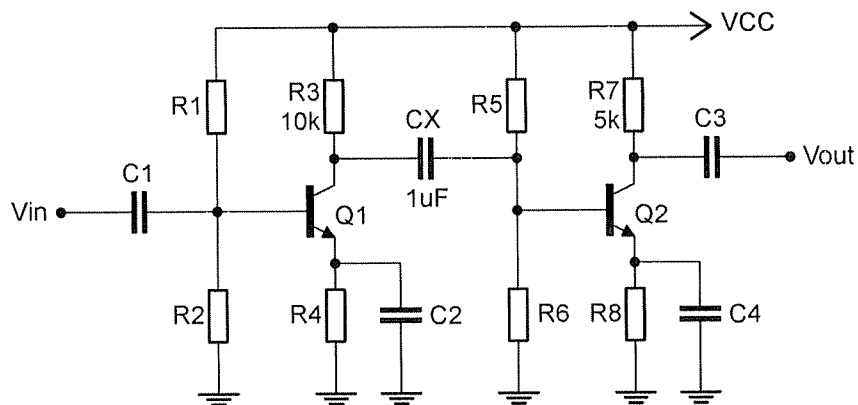


Figure-Q2

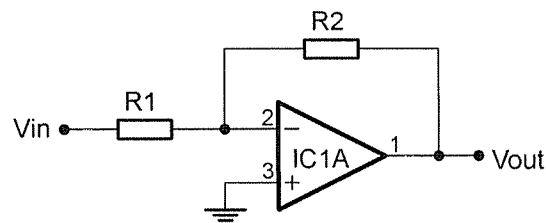
- a. Draw the AC equivalent circuit for the amplifier circuit in Figure-Q2 with the inclusion of capacitor CX. [6]

- b. Hence, estimate the followings:
 - i. The input resistance of the amplifier circuit. [3]
 - ii. The overall mid-band voltage gain in decibels (dB). [6]
 - iii. The output resistance of the amplifier circuit. [3]
 - iv. The 3dB lower-cutoff frequency. [5]

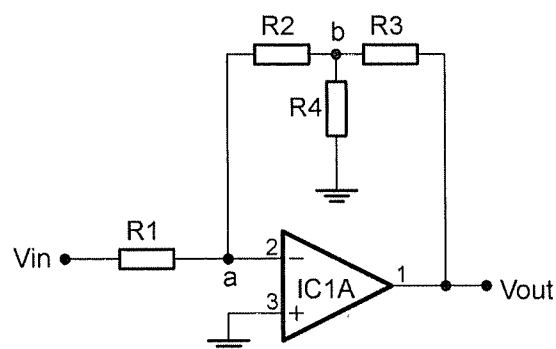
- c. How does the mid-band voltage gain of the amplifier circuit being affected when a grounded $1\text{k}\Omega$ load is connected at the output terminal? [2]

Question 3

- a. i. Write the node voltage equation at the inverting input terminal of the op-amp in Figure-Q3(a) in terms of V_{in} and V_{out} . Hence, determine the voltage transfer function expression, V_{out}/V_{in} of the op-amp circuit. Assume ideal op-amp operation. [5]
- ii. If $R_2 = 1\text{k}\Omega$ in Figure-Q3(a), determine the value of R_1 for a 41.584dB voltage gain. [5]
- iii. What is the drawback of the design in part (a)(ii)? [2]

**Figure-Q3(a)**

- b. i. Write the node voltage expressions at node-a and node-b respectively. Assume ideal op-amp operation. [4]
- ii. Hence, determine the voltage transfer function expression, V_{out}/V_{in} of the op-amp circuit. [4]
- iii. If $R_1 = R_4 = 1\text{k}\Omega$ and $R_2 = R_3 = 10\text{k}\Omega$, determine the voltage gain of the op-amp circuit in dB. [3]
- iv. What is the advantage of the design in Figure-Q3(b) as compare to the one in Figure-Q3(a)? [2]

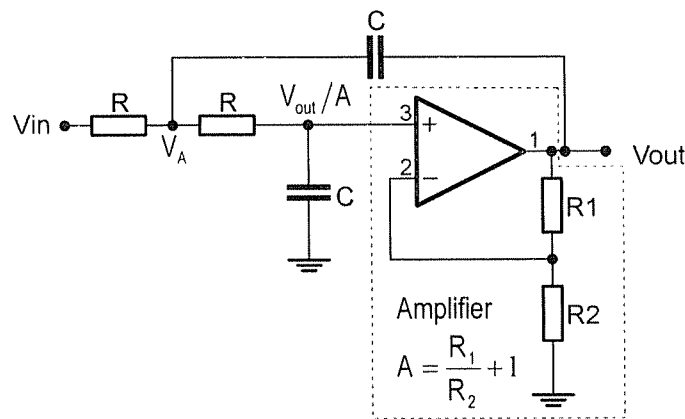
**Figure-Q3(b)**

Question 4

- a. The voltage transfer function of an active filter circuit is given by,

$$T(s) = \frac{500}{s^2 + bs + 100}$$

- i. State the type of active filter given. [2]
- ii. What is the expected output voltage if a DC voltage is applied to this filter circuit? Justify your answer quantitatively. [4]
- iii. If $b = 2$ in the transfer function expression, how does it affect the frequency response of the active filter? Justify your answer quantitatively. [4]
- iv. For $b = 2$, what is the phase difference between the input and output signals if a 2 Hz sine wave is applied to this filter? [5]

**Figure-Q4(b)**

- b. Figure-Q4(b) shows a Sallen-and-Key active filter circuit. V_A and V_{out}/A shown in Figure-Q4(b) are the respective node voltages.
- i. Write a node equation for node- V_A . [2]
 - ii. Write a node equation for node- V_{out}/A . [2]
 - iii. Making use of the equations in part Q4(b)(i) and (ii), formulate the voltage transfer function of the filter circuit. [3]
 - iv. Hence, determine the maximum gain value for A to ensure the filter circuit is stable. [3]

Question 5

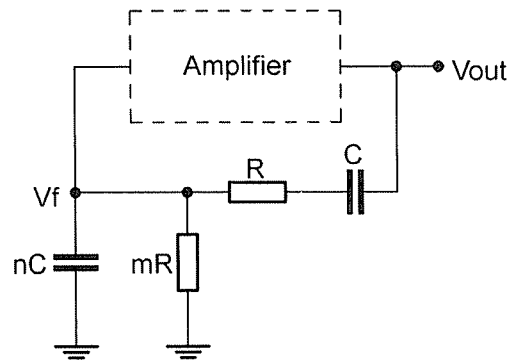


Figure-Q5

- Derive the transfer function polynomial expression V_f / V_{out} in Figure-Q5. State the assumption made. m and n shown in Figure-Q5 are the respective ratios of the resistors and capacitors. [6]
- Determine the operating frequency value of the RC feedback circuit in Figure-Q5, in which V_f is in-phase with V_{out} . [7]
- Draw the circuit configuration of the amplifier in Figure-Q5 so that the whole circuit operates as a harmonic oscillator, sustaining an oscillating frequency value identical to the one found in part (b). [4]
- Suggest appropriate component values for the amplifier circuit drawn in part (c) if $m = 3$ and $n = 5$. [6]
- What is the main factor that limits the oscillation frequency of the circuit? [2]

Question 6

a. Draw the basic block diagram of a series linear voltage regulator. [6]

b. i. Define line regulation of linear voltage regulator. [2]

ii. A voltage regulator has the following specifications:

Regulated output voltage: 5V

Nominal input voltage: 7V

Line regulation: 600mV/V

If the input voltage fluctuation to this voltage regulator is as shown in Figure-Q6(b), sketch the timing diagram of the corresponding output voltage. Label all the relevant output voltage values clearly. [6]

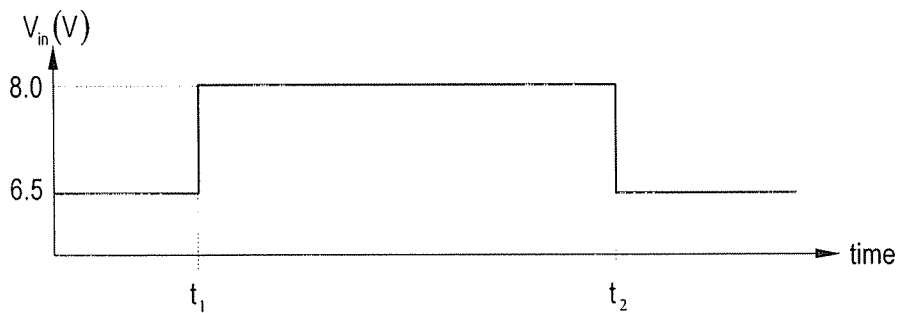


Figure-Q6(b)

c. Figure-Q6(c) shows a voltage regulator circuit. Assume V_{BE} for transistors T1 and T2 are 0.75V. Potentiometer VR1 adjusts the required output voltage.

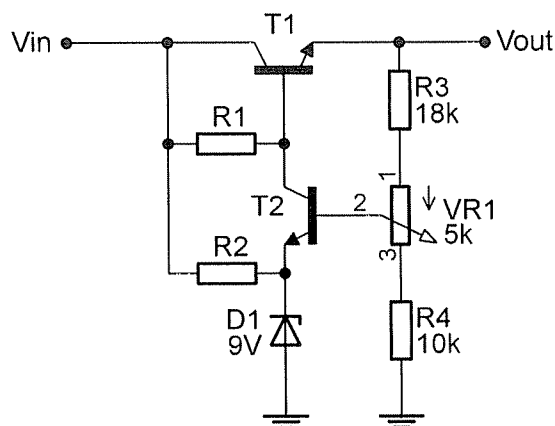


Figure-Q6(c)

- i. Estimate the maximum output voltage of the circuit in Figure-Q6(c). [4]
- ii. Estimate the minimum output voltage of the circuit in Figure-Q6(c). [4]
- iii. Explain how the circuit regulates the output voltage in the event of an increment in output voltage. [3]

– THE END –