INTI
INTERNATIONAL COLLEGE PENANG (507232-U)
LAUREATE INTERNATIONAL UNIVERSITIES

FINAL
Examination Paper

(COVER PAGE)

Session : January 2012

Programme : DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING (DEEI)

Course : **EEE1102 : ELECTRONIC DEVICES AND CIRCUIT THEORY I**

Date of Examination : 6 March 2012

Time : 11a.m. – 1p.m. Reading Time : Nil

Duration : 2 Hours

Special Instructions :

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Materials permitted :

Non Programmable Scientific Calculator

Materials provided :

Nil

Examiner(s) : **Liong Han Wen**

Moderator : **Shalyn Lim Sheue Hui**

This paper consists of 7 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEE/I)

EEE 1102 : ELECTRONIC DEVICES AND CIRCUIT THEORY 1
FINAL EXAMINATION : JANUARY 2012 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks. The marks allocated to each sub-question are shown in brackets at the right-hand margin.

Question 1

a. Sketch a graph showing the forward and reverse characteristics of a typical silicon diode. (4 marks)

b. Find the average value of the voltage waveform as shown in Figure Q1(b) (5 marks)

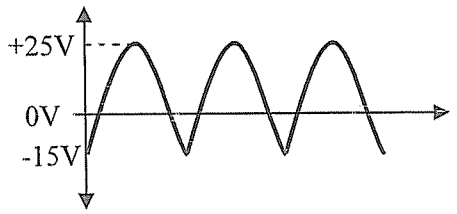


Figure Q1(b)

c. Determine the power dissipation of the resistors and zener diode in Figure Q1(c). Given Vs = 15V, Rs = 560Ω, R_L = 2kΩ, V_Z = 10V. Assume the zener diode is ideal. Also, calculate the total power delivered by V_S. (8 marks)

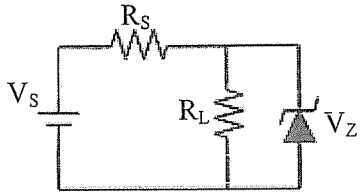
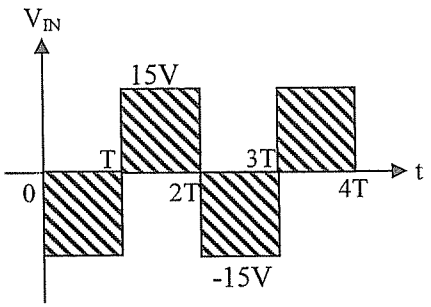


Figure Q1(c)

d. Sketch a half wave voltage multiplier by using diode(s) and capacitor(s). Identify the input and output terminals. (4 marks)

e. Sketch the output waveform for the clamper circuit shown in Figure Q1(e).Assume ideal diode. (4 marks)



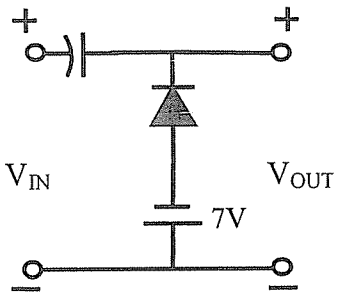


Figure Q1(e)

Question 2

a. Sketch the output waveform of the following rectifier circuits. The input waveform is shown in Figure Q2(a). Assume all the diodes in this part are ideal.

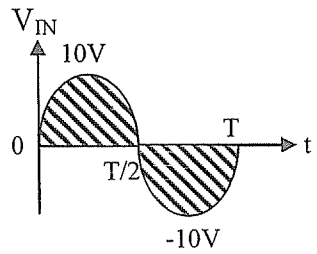
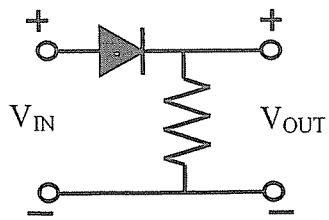
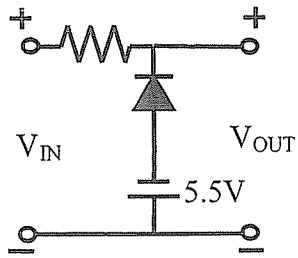


Figure Q2(a)

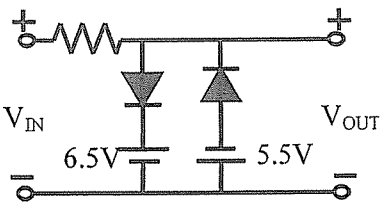
(i) (3 marks)



(ii) (5 marks)



(iii) (6 marks)



b. For the circuit shown in Figure Q2(b), D_1 and D_2 are practical diodes. Find I_{D1} and I_{D2}.
(6 marks)

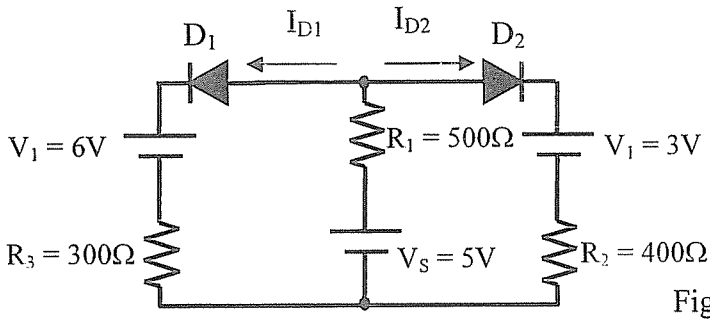


Figure Q2(b)

c. Design a clamper to perform the function indicated in Figure Q2(c). Assume practical diodes.
(5 marks)

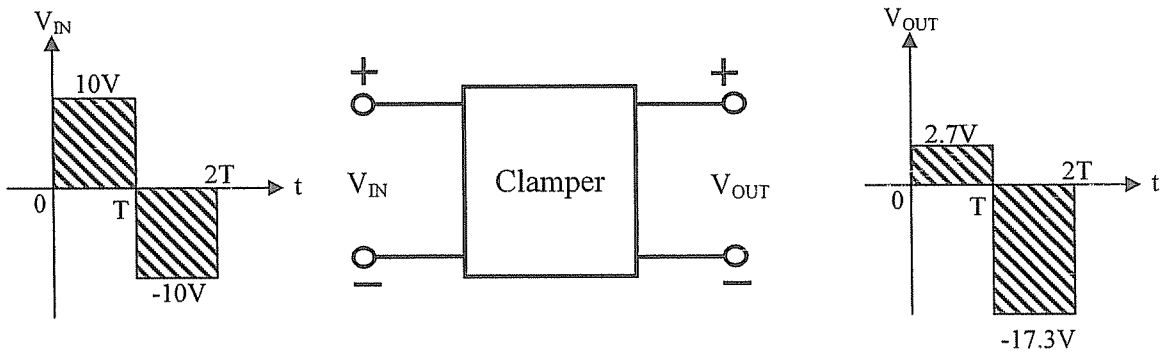


Figure Q2(c)

Question 3

a. Determine the I_{CQ} for the transistor circuit shown in Figure Q3(a). Given $\beta_{DC} = 150$.
(8 marks)

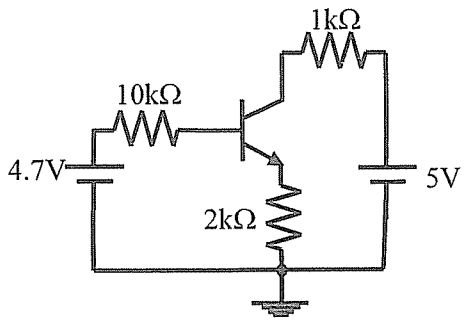


Figure Q3(a)

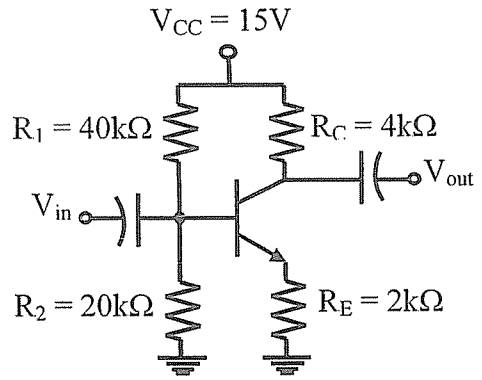
b. For the unloaded amplifier in Figure Q3(b),

(i) Perform DC analysis and sketch the ac equivalent circuit with correct components value. (7 marks)

(ii) Find the total ac input resistance, $R_{in(tot)}$ (3 marks)

(iii) Find the amplifier voltage gain, A_V (4 marks)

(iv) Find the new amplifier voltage gain if a 5kΩ load resistor is capacitively coupled to the collector terminal. (3 marks)



$\beta_{DC} = 90$
$\beta_{ac} = 100$

Figure Q3(b)

Question 4

a. For the transistor circuit shown in Figure Q4(a), determine the DC value of :

(i) I_E (4 marks)

(ii) V_C (3 marks)

(iii) V_{CE} (4 marks)

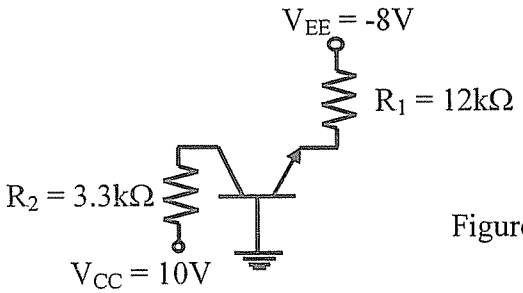
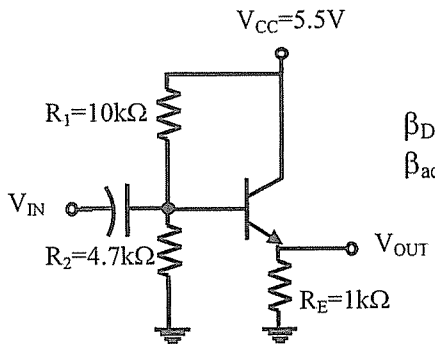


Figure Q4(a)

b. A load resistance(R_L) is capacitively coupled to the emitter in Figure Q4(b). What value of R_L will cause the voltage gain become 0.85? (14 marks)

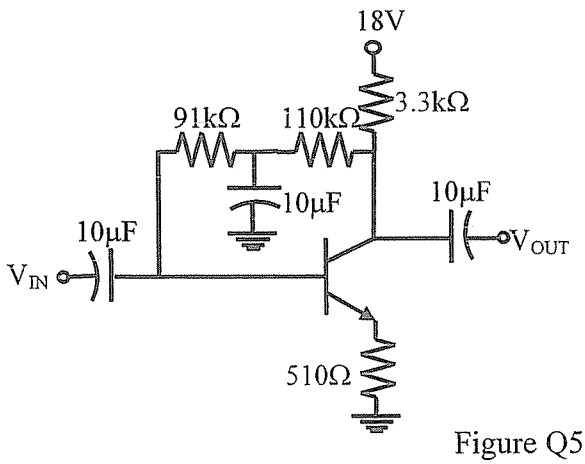


$\beta_{DC} = 90$
$\beta_{ac} = 100$

Figure Q4(b)

Question 5

a. Determine the dc level of I_B and V_C for the circuit shown in Figure Q5(a). (12 marks)



$\beta_{DC} = 75$

Figure Q5(a)

b. Determine the terminal voltages (V_C,V_B and V_E) of the transistor in Figure Q5(b). Also determine the values of V_{CE}, V_{BE} and V_{BC}. (13 marks)

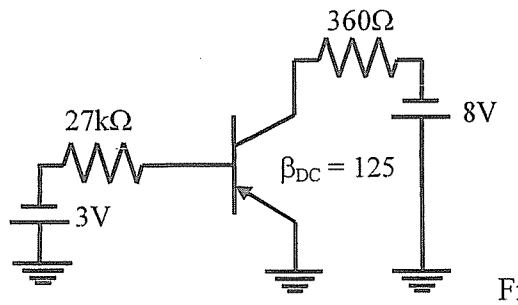


Figure Q5(b)

Question 6

a. Sketch the construction of Depletion MOSFET(both p and n channel). What is the difference between the operation of D-MOSFET and E-MOSFET? (6 marks)

b. Given a D-MOSFET with I_{DSS} = 10mA and $V_{GS(off)}$ = -8V.

(i) What type of the D-MOSFET is? Why? (2 marks)

(ii) Calculate I_D at V_{GS} = -3V (2 marks)

(iii) Calculate I_D at V_{GS} = +3V (2 marks)

c. What is the total ac output voltage of the unloaded amplifier shown in Figure Q6(c). Given $I_D = 1.96mA$. For this particular JFET, I_{DSS} is 12mA and $V_{GS(off)}$ is -3V. (8 marks)

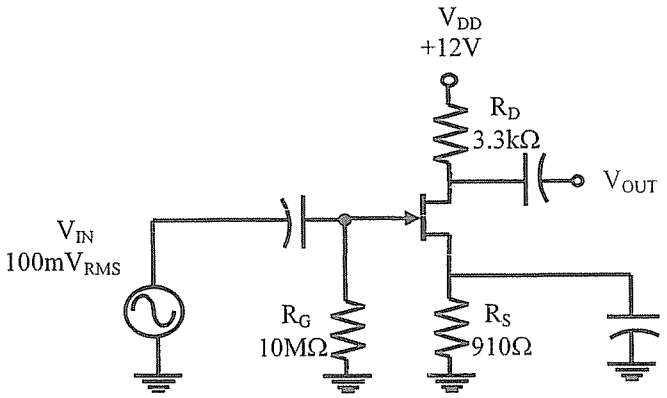


Figure Q6(c)

d. Find V_{GS} and V_{DS} for the E-MOSFET circuit in Figure Q6(d). Datasheet information is listed with the circuit. (5 marks)

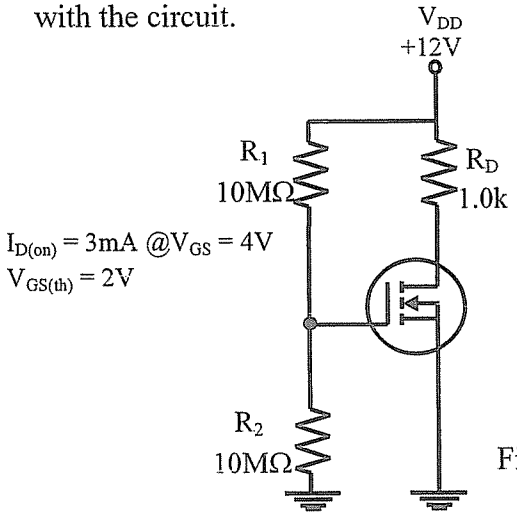


Figure Q6(d)

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