INTI
INTERNATIONAL COLLEGE PENANG (507232-U)
LAUREATE INTERNATIONAL UNIVERSITIES

FINAL
Examination Paper

(COVER PAGE)

Session : JANUARY 2012

Programme : DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING

Course : **EEE2101: INTRODUCTION TO DIGITAL ELECTRONICS.**

Date of Examination : 5 March 2012

Time : 11a.m. – 1p.m. Reading Time : Nil

Duration : 2 Hours

Special Instructions :

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Materials permitted :

NON PR0GRAMMABLE CALCULATOR

Materials provided :NIL

Examiner(s) : **V.MEENAKSHI SUNDARAM**

Moderator : **KHOO BOO TAP**

This paper consists of 5 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONICS ENGINEERING (DEE)

EEE 2101: INTRODUCTION TO DIGITAL ELECTRONICS
FINAL EXAMINATION: JANUARY 2012 SESSION

Instructions: This paper consists of SIX (6) questions. Answer any FOUR (4) questions in the answer booklet provided. All questions carry equal marks.

Question 1

(a) (i) Subtract 33_H from $B8_H$, express the answer in binary number.

(2 marks)

(ii) Determine the decimal value of given signed binary number expressed in sign magnitude: 10010101.

(3 marks)

(iii) Convert 0.12_{10} to hexadecimal number.

(3 marks)

(b) Convert the decimal number 0.3112_{10} into binary number.

(3 marks)

(c) Perform the following subtraction of the signed binary numbers using 2's complement method:
$0000\ 1000_2 - 00000011_2$

(4 marks)

(d) (i) Inputs A and B are applied to a NOR gate. Inputs B and C are applied to a second NOR gate. The outputs of the two NOR gates are then applied to a NAND gate. Determine the Boolean equation of the output F of the circuit.

(4 marks)

(ii) Use De Morgan's rules to prove that a coincidence gate provides the inverse function to an exclusive OR gate.

(6 marks)

Question 2

(a) Using Boolean Algebra simplify the following Boolean expression:
$F = \overline{AB + AC + \overline{A}BC}$.

(4 marks)

(b) (i) Design the logic circuit for the following equation by using NOR gates only.
$F = A\overline{B} + \overline{A}B$.

(4 marks)

(ii) Inputs A and B are applied to the inputs of a 2-input NAND gate. Inputs C and B are applied to the inputs of another 2-input NAND gate. The outputs of the two NAND gates are applied to a NOR gate. Show that the circuit could be replaced by one 3-input AND gate.

(6 marks)

(c) (i) Draw and explain the half adder circuit.

(4 marks)

(ii) Define Demultiplexers.

(3 marks)

(iii) Prove that $A + \overline{A}B = A + B$

(4 marks)

Question 3

(a) (i) Convert the following SOP expression to an equivalent POS expression
$\overline{A}\overline{B}\overline{C} + \overline{A}B\overline{C} + \overline{A}BC + A\overline{B}C + ABC$.

(4 marks)

(ii) Reduce to its simplest form

$$F = \overline{(A + \overline{B} + C) + (\overline{A} + \overline{B} + C + D) + (\overline{A} + B + \overline{C} + \overline{D}) + (A + C)}$$

(6 marks)

(iii) Use a K-map to minimize the following SOP expression:
$\overline{B}\overline{C}D + \overline{A}B\overline{C}D + AB\overline{C}D + \overline{A}\overline{B}CD + A\overline{B}CD + \overline{A}\overline{B}C\overline{D} + \overline{A}BC\overline{D} + ABC\overline{D} + A\overline{B}C\overline{D}$.

(4 marks)

(b) Draw the logic circuit diagram for the following expression

(i) AB+A(B+C)+B(B+C) (3marks)

(ii) B+AC also prove that these two equations are equivalent.

(2marks)

(c) Design the logic circuit for the following equation by using NOR gates only.
$F = A\overline{B} + \overline{A}B$.

(6 marks)

Question 4

(a) Define

(i) Word capacity expansion.

(3 marks)

(ii) Word length expansion.

(3 marks)

(b) Design a decoder using the 16×8 PROM which accepts BCD inputs 0000 through 1001, and displays the letter A through J, respectively on a common cathode 7-segment display.

(15 marks)

(c) Define PROM.

(4 marks)

Question 5

(a) (i) How many conditional flags associated with the 8085 microprocessor? Explain them with examples.

(5 marks)

(ii) Write a program to subtract 04_H in the B register from 08_H in the C register and store the result in a memory location of 8150_H.The program should halt at the end of execution.

(6 marks)

(b) With the aid of a diagram describe Ramp type analog to digital conversion.

(8 marks)

(c) A weighted resistor DAC has R_f=20KΩ and R =12.5KΩ.Calculate its output voltage when the 4-bit digital input word is (i) 1010, and (ii) 0101.
Logic 1 voltage =5V.

(6 marks)

Question 6

(a) (i) A weighted resistor type 4-bit DAC uses a voltage of 5 V and the feedback resistor is 1000Ω .If the output voltage produced by the LSB is to be 0.05 V, determine the required value for R.

(4 marks)

(ii) Draw the logic symbol ant truth table for X-NOR gate.

(4 marks)

(b) (i) An 8-bit DAC of the binary weighted type uses a lowest resistor value of 1kΩ. Calculate the values required for the other resistors. Comment on your answer.

(4 marks)

(ii) Calculate the resolution of a 12 bit ADC and find equivalent value for a 10 V input voltage range.

(5marks)

(c) Explain the operation and write the addressing method and flags involved in the following instructions

(i) LDA addr (2marks)

(ii) MOV M,R (2marks)

(iii) STA addr (2marks)

(iv) MVI M, 04. (2marks)

--THE END—