INTI International College Penang

FINAL
ALTERNATIVE ASSESSMENT

(COVER PAGE)

Session	:	**April 2021**
Programme	:	Diploma in Electrical & Electronic Engineering (DEEI)
Course	:	**EEE2112: Introduction to Power Electronics & Drives**
Date of Examination	:	27 July 2021 (Tuesday)
Time	:	2.00pm – 5.00pm Reading Time : Nil
Duration	:	3 Hours

Special Instructions :

This paper consists of **FOUR (4)** questions. Answer **ALL FOUR (4)** questions. All questions carry equal marks. The marks allocated to each sub-question are shown in square brackets at the right-hand margin. Present your answers neatly and clearly. The assessor reserves the rights to ignore your answers if they are ambiguous.

Material permitted : Non-Programmable Scientific Calculator

Materials provided : Nil

Examiner(s) : **Chan Tse Wei**

Chief Moderator : Richard Lai TF

*This paper consists of **9** printed pages, including the cover page*

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE2112: INTRODUCTION TO POWER ELECTRONICS AND DRIVES
FINAL ALTERNATIVE ASSESSMENT: APRIL 2021 SESSION

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Question 1

a. Explain two advantages of power MOSFETs that are not found in the power BJTs. [5]

b. Table-Q1(b) tabulates the difference between a single phase half-wave controlled rectifier and a single phase half-wave uncontrolled rectifier

Copy Table-Q1(b) into your answer script. Complete the table by filling up the blank cells. Assume that each rectifier has a pure resistive load and the power switching devices are ideal. [5]

Table-Q1(b)

	Single Phase Half-wave Uncontrolled Rectifier	Single Phase Half-wave Controlled Rectifier
Power switching devices used:		
Additional circuit needed:		
Power efficiency:		

c. Figure-Q1(c)(i) shows a AC-DC converter circuit and Figure-Q1(c)(ii) shows the simulated timing diagrams of the converter's input voltage V_{in} and load current I_{load}. The power switching device in the converter is assumed ideal.

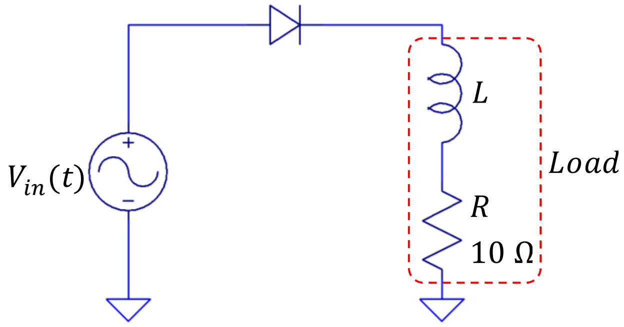

Figure-Q1(c)(i)

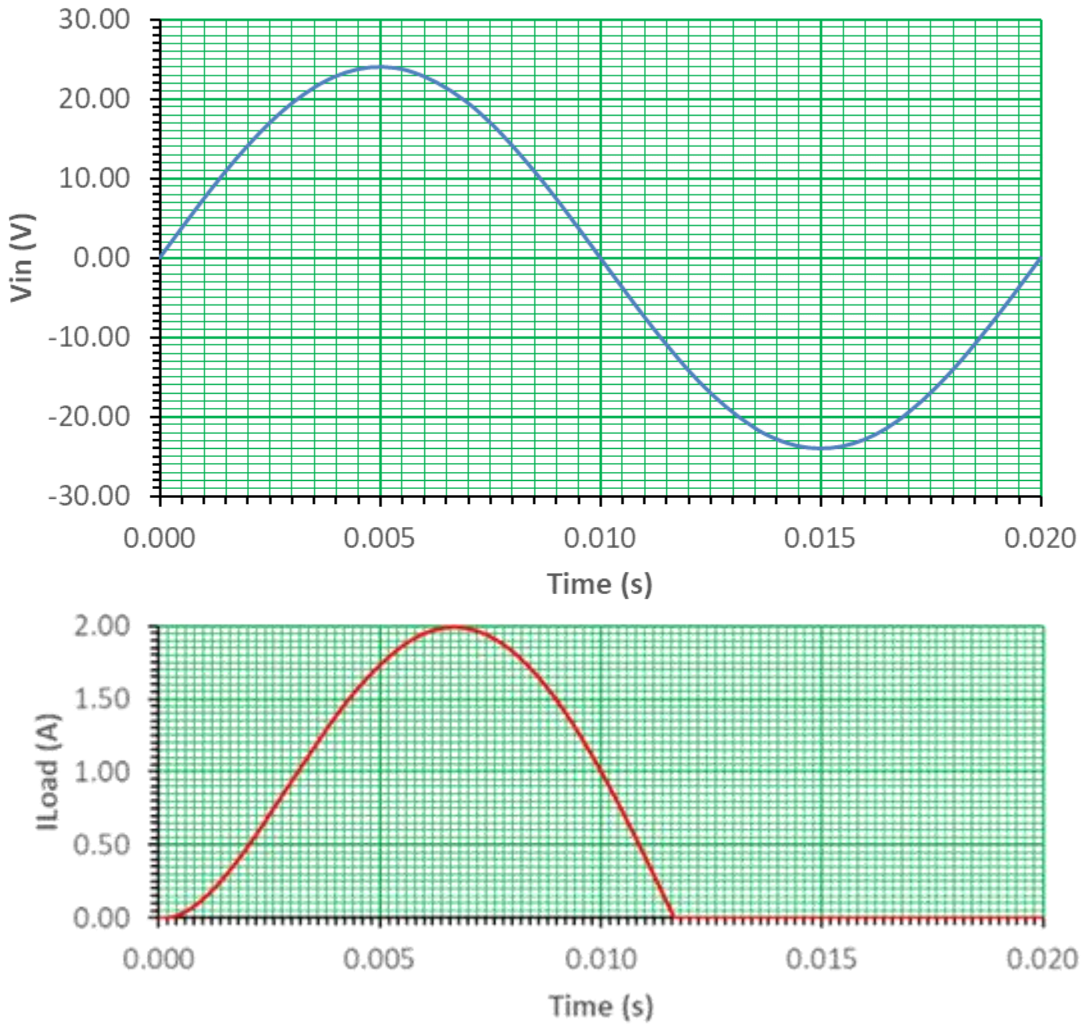

Figure-Q1(c)(ii)

i. Calculate the voltage drop across inductor L when the load current I_{load} reaches its peak value. [3]

ii. Within one complete cycle of V_{in}, determine the duration when inductor L is returning energy back to the converter. [3]

iii. Calculate the voltage drop across inductor L the moment when I_{load} reduces to 1 A from its peak value. [5]

iv. Sketch the synchronized timing diagram of the voltage drop across the load clearly. [4]

Question 2

a. Table-Q2(a) shows the specifications of an IGBT. By referring to Table-Q2(a), State and explain the type of power losses (conduction, leakage and switching losses) to be considered in this IGBT. Numerical calculations are not required. [5]

Table-Q2(a)

Parameter	Symbol	Test Conditions	Typ. Value	Unit
Collector-Emitter saturation voltage	$V_{CE(sat)}$	$V_{GE} = 15$ V, $I_C = 50$ A	1.5	V
Gate-Emitter threshold voltage	$V_{GE(th)}$	$V_{GE} = V_{CE}$, $I_C = 350$ µA	5.5	V
Collect-Emitter cutoff current	I_{CES}	$V_{GE} = 0$ V, $V_{CE} = 600$ V	0	A
Rise time	t_r	$V_{CC} = 400$ V, $I_C = 50$ A	43	ns
Fall time	t_f	$V_{CC} = 400$ V, $I_C = 50$ A	105	ns

b. Figure-Q2(b) shows a block diagram of a buck chopper circuit. Clearly explain the need for a pulse width modulated (PWM) signal generator in the circuit. [5]

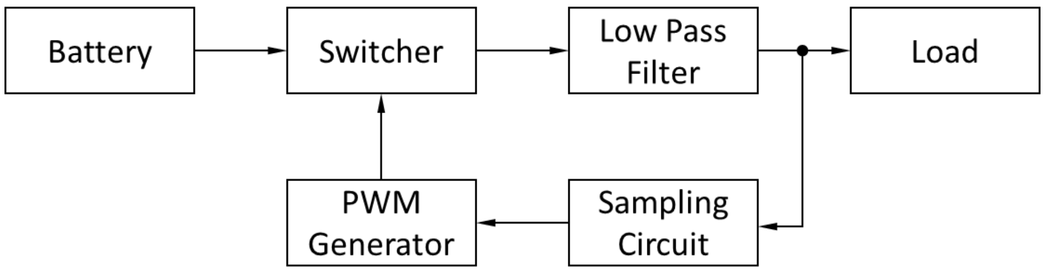

Figure-Q2(b)

c. Figure-Q2(c) shows a basic DC-DC converter. $V_{control}$ is that voltage source that drives the voltage-controlled switch S. It produces a driving pulse of 50 kHz at a duty cycle of 0.24.

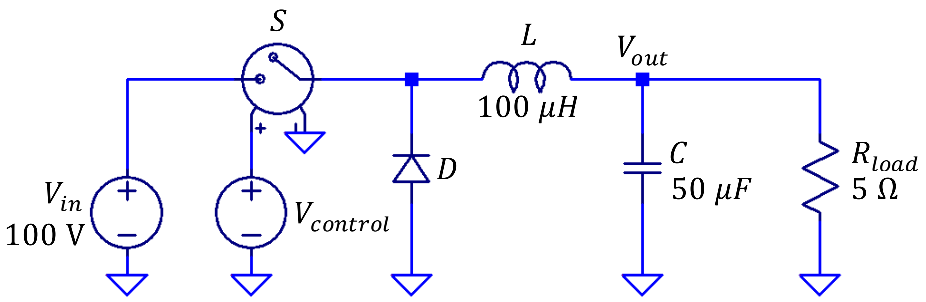

Figure-Q2(c)

Assume that the converter is operating in its steady-state condition and all components are ideal.

i. Calculate the lowest power rating for R_{load}. [4]

ii. Clearly sketch the timing diagram of the current flowing through inductor L for one complete switching cycle. [4]

iii. Calculate the current flowing through diode D in RMS value for one complete switching cycle. [7]

Question 3

a. With the aid of a diagram, explain the reason for an SCR to remain in current blocking state even though it is being forward-biased. [5]

b. Figure-Q3(b) shows a power converter circuit and its corresponding output voltage timing diagram.

i. Identify the type of power converter shown in the figure. [2]

ii. Explain the need to apply the input voltage V_{in} to the gate drive controller. [3]

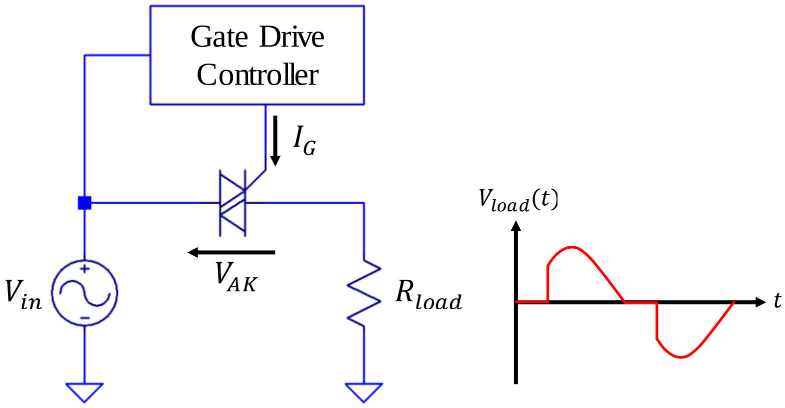

Figure-Q3(b)

c. Figure-Q3(c) shows the synchronized timing diagrams of the input voltage V_{in} and the gate current I_G of the power converter circuit shown in Figure-Q3(b).

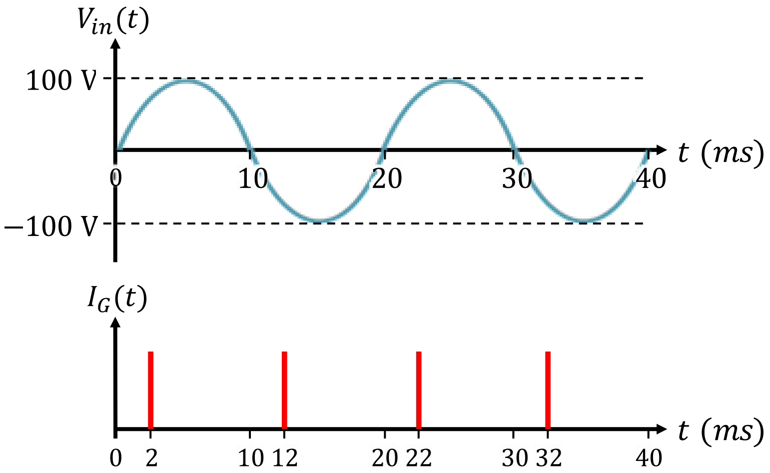

Figure-Q3(c)

For one complete cycle of V_{in}, calculate

i. the RMS voltage of V_{load}. [5]

ii. the RMS voltage of V_{AK}. Assume that the TRIAC is ideal. [4]

iii. the percentage change in the trigger moment if the RMS voltage of V_{load} is reduced by 40% from the value obtained in part (c)(i). [6]

Question 4

a. Figure-Q4(a) shows a linearized reverse recovery characteristics of a diode. Calculate the diode's recovery charge, Q_{rr}. [5]

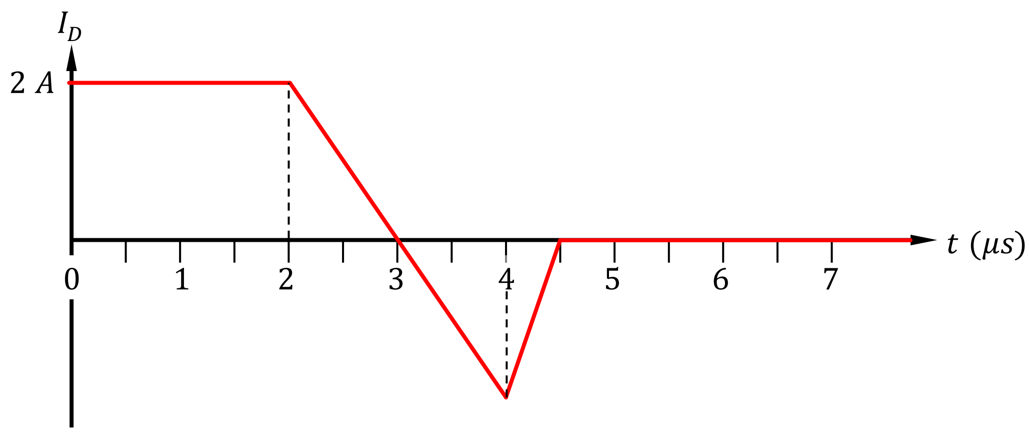

Figure-Q4(a)

b. Figure-Q4(b)(i) shows a conceptual full-bridge square-wave inverter. At the circuit's steady-state operating condition, $i_{load}(t)$ is periodic and symmetric about 0 A. S_1 to S_4 are lossless power switching devices.

The inverter operates such that, S_1 and S_4 turn on for $0 \le t \le 0.5T$ while S_2 and S_3 turns on for $0.5T \le t \le T$, where T is the period of operation for one cycle which does not cause load current saturation.

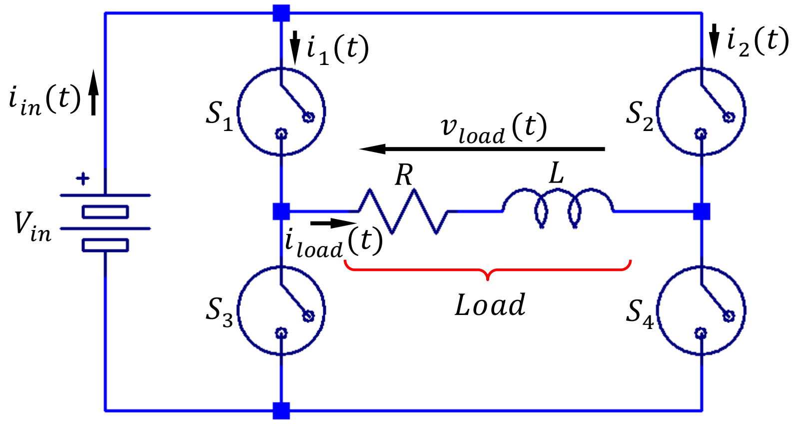

Figure-Q4(b)(i)

By copying Figure-Q4(b)(ii) into your answer script, sketch the timing diagram for all the given electrical quantities. [5]

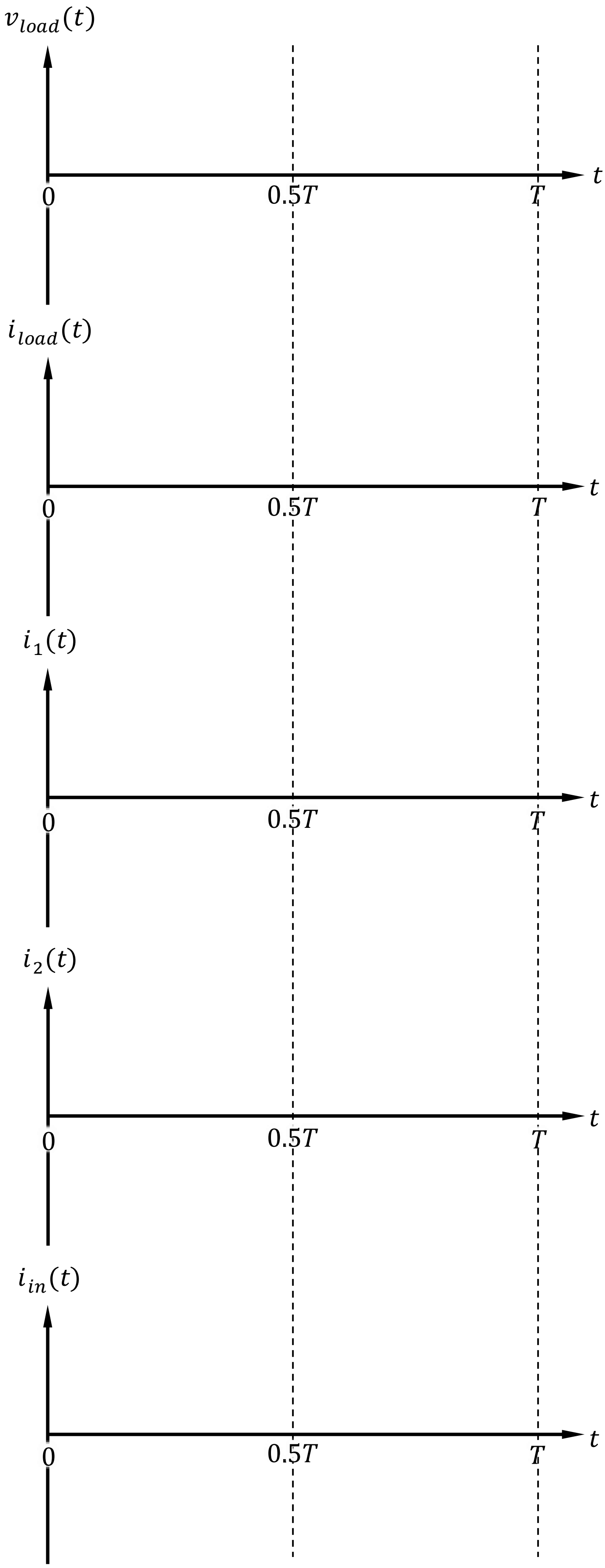
$v_{load}(t)$
t
0
$0.5T$
T
$i_{load}(t)$
t
0
$0.5T$
T
$i_1(t)$
t
0
$0.5T$
T
$i_2(t)$
t
0
$0.5T$
T
$i_{in}(t)$
t
0
$0.5T$
T

Figure-Q(b)(ii)

c. By referring to the answers provided for Figure-Q4(b)(ii),

i. show that the load current i_{load} has a peak-to-peak value given by,

$$i_{load(pp)} = \frac{2V_{in}}{R}\left(\frac{1 - e^{-\frac{0.5T}{\tau}}}{1 + e^{-\frac{0.5T}{\tau}}}\right)$$

where τ = time constant of the load. [6]

ii. calculate the load power if the inverter has the following specifications:

$V_{in} = 50$ V

$L = 20$ mH

$R = 100\ \Omega$

$T = 500\ \mu$s [9]

~THE END~