INTI International College Penang

FINAL
ALTERNATIVE ASSESSMENT

(COVER PAGE)

Session	:	**April 2021**
Programme	:	Diploma in Electrical & Electronic Engineering (DEEI)
Course	:	**EEE2101: Introduction to Digital Electronics**
Date of Examination	:	28 July 2021 (Wednesday)
Time	:	2.00pm – 5.00pm Reading Time : Nil
Duration	:	3 Hours

Special Instructions :

This paper consists of **FOUR (4)** questions. Answer **ALL** questions. All questions carry equal marks.

Material permitted :
Non-Programmable Scientific Calculator

Materials provided :
Nil

Examiner(s)	:	**Steven Khoo Boo Tap**
Chief Moderator	:	Chan Tse Wei

*This paper consists of **10** printed pages, including the cover page*

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE2101: INTRODUCTION TO DIGITAL ELECTRONICS
FINAL ALTERNATIVE ASSESSMENT: APRIL 2021 SESSION

Instructions: This paper consists of **FOUR (4)** questions. Answer **ALL** questions. All questions carry equal marks.

Question 1

(a) Present the following Boolean expressions according to the stated simplest form, using the specified method:

(i) $F_1(W,X,Y,Z) = \sum m(0,5,10,15) + d(2,7,8,13)$
Simplest Form: Any type of gate implementation deemed appropriate.
Method: Karnaugh Map and/or Boolean Algebra.

(4 marks)

(ii) $F_2(R,S,T,U) = \prod M(1,2,4,7,8,11,13,14) \cdot \prod d(3,6,9,12)$
Simplest Form: Any type of gate implementation deemed appropriate.
Method: Karnaugh Map and/or Boolean Algebra.

(4 marks)

(iii) $F_3(K,L,M,N) = \sum m(0,1,2,4,6,8,10,11,12,14) + d(3,9)$
Simplest Form: Any type of gate implementation deemed appropriate.
Method: Karnaugh Map and/or Boolean Algebra.

(4 marks)

(b) (i) Produce the simplest Boolean expression for F in Figure 1(b) and present the minimum expression using Boolean simplification method only.

(6 marks)

(ii) Suggest only one type of gate to represent the simplified expression and state the IC part number for the implementation.

(2 marks)

Show all workings clearly.

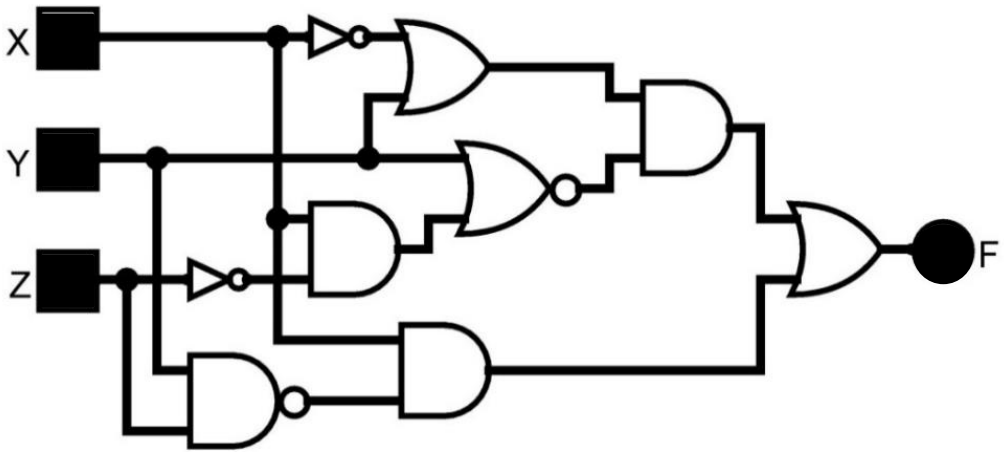

Figure 1(b)

(c) Solve the numbering system transformation of [163.0703125_{10} – 9.208_{16}] to its hexadecimal equivalent with 3 hexadecimal points accuracy. Show all workings clearly. (5 marks)

Question 2

(a) A D flip-flop is connected as shown in Figure 2a(i).

(i) Present the D flip-flop input expression in Figure 2(a)(i). (1.5 marks)

(ii) Sketch the output, Q with the given inputs, A and B waveforms as shown in Figure 2a(ii). The output Q is initially HIGH. Assume that there is no propagation delay issue and the flip-flop has been enabled. Copy Figure 2a(ii) into your answer sheet. (3.5 marks)

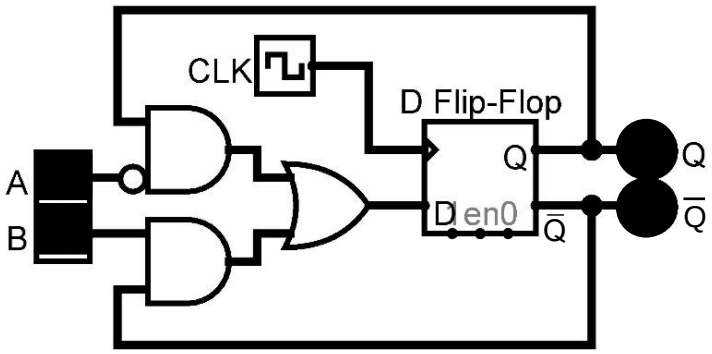

Figure 2(a)(i)

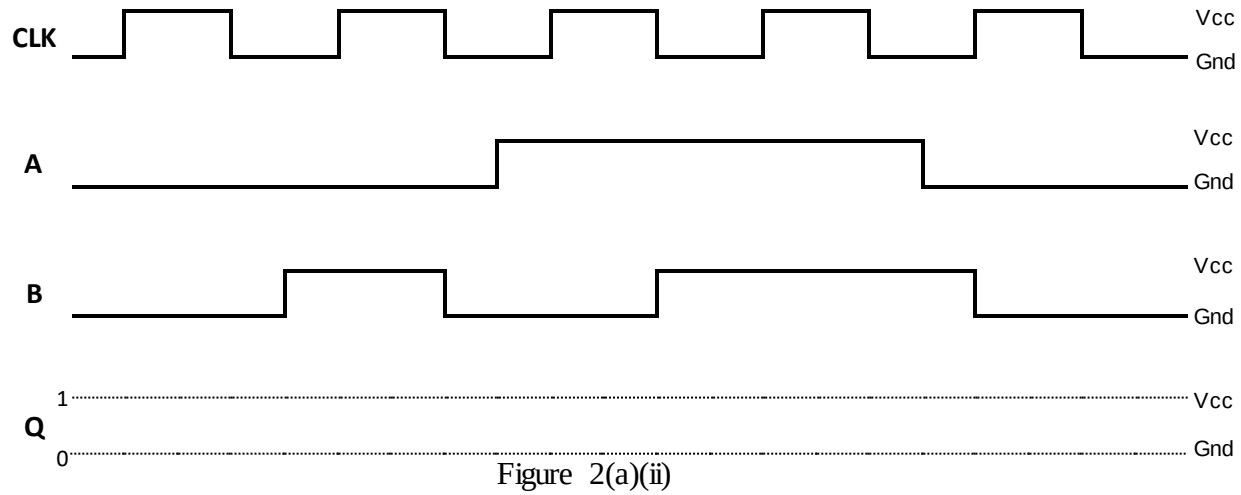

Figure 2(a)(ii)

(b) A NOR SR latch is driven by a 2-bit binary counter with outputs designated B_1B_0 (B_1 is the MSB) through a combinational logic circuit. Output B_1 is ANDed with $(B1 \oplus B0)$ and drives the R input of the SR latch. B_0 is also ANDed with $(B1 \oplus B0)$ and drives the S input.

(i) Draw the logic circuit showing the signals, B_1 & B_0 and output, Q of the SR latch. (2.5 marks)

(ii) Construct a table to record the output, Q of the SR latch as the counter steps through its 4 states beginning with $B_1B_0 = 00$. Assume the output is initially RESET. (2.5 marks)

(c) Figure 2(c) shows a 4-bit synchronous counter, which is designed to perform a specific counting sequence.

Flip-flop FF3 is MSB and flip-flop FF0 is LSB. Flip-flop J_3K_3 has output Q_3, flip-flop J_2K_2 has output Q_2, flip-flop J_1K_1 has output Q_1 and flip-flop J_0K_0 has output Q_0. Assume all flip-flops are initially in 0000 (State 0) for $Q_3Q_2Q_1Q_0$ outputs.

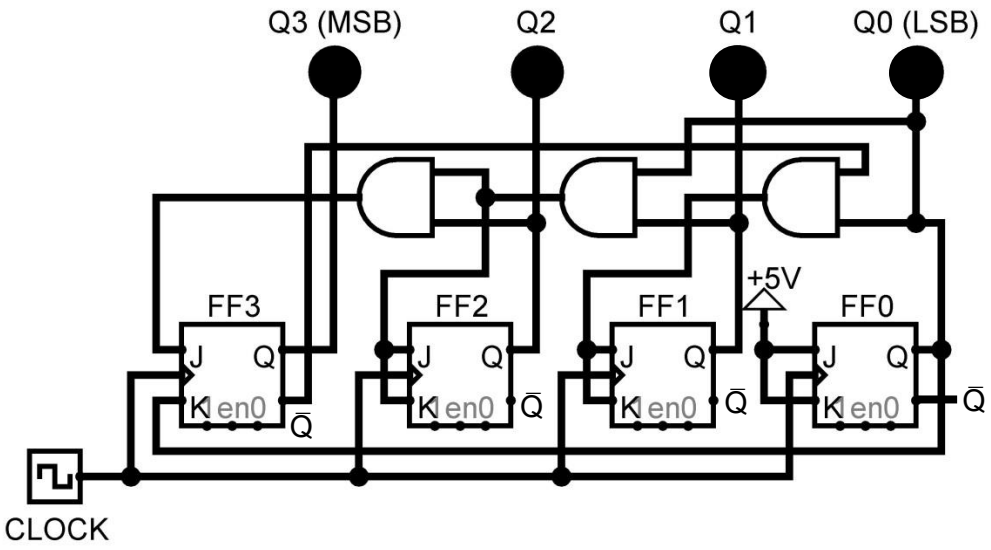

Figure 2(c)

Show all workings clearly according to the procedures listed in part (c)(i), (c)(ii), (c)(iii) and (c)(iv).

(i) Provide the excitation expressions for each of the flip-flops in Figure 2(c).

(4 marks)

(ii) Produce the Karnaugh maps according to the excitation expressions obtained in part (c)(i).

(4 marks)

(iii) Build the transition table/next state table from the Karnaugh maps obtained in part (c)(ii).

(5 marks)

(iv) Sketch the state diagram and comment on the states obtained.

(2 marks)

Question 3

(a) Solve the numbering system transformation of $[156.32_8 \times 10.625_{10}]$ to its binary equivalent with 8 binary points accuracy. Show all workings clearly.

(5 marks)

(b) Table 3(b) shows a portion of a quadruple 2-input XOR gates (DM7486) datasheet. Compute the following parameters from this datasheet, show all workings clearly:

(i) Power dissipation, $P_{D(max)}$ on a DM7486 IC when the output condition is as shown in Figure 3(b). Assume that the V_{CC} used is maximum.

(4 marks)

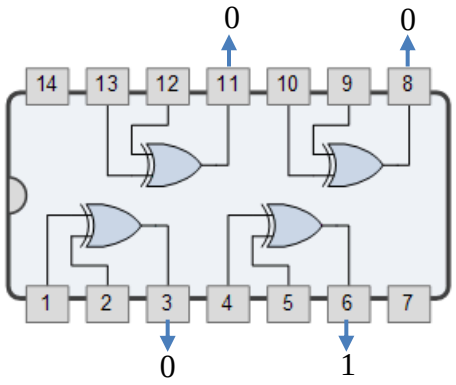

Figure 3(b)

(ii) Fan-out, the number of gates from the same IC family that can be safely driven by an output under worst-case consideration.

(3 marks)

(iii) Noise Margin voltages, V_{NL} and V_{NH}.

(3 marks)

Table 3(b)

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			–0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.2	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			40	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max (Note 4)		6.1	10	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max (Note 5)		9	15	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CCH} is measured with all outputs OPEN, one input at each gate at 4.5V, and the other inputs grounded.

Note 5: I_{CCL} is measured with all outputs OPEN and all inputs grounded.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	Conditions	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Other Input Low		18		23	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			17		21	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Other Input High		10		15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			12		15	ns

(c) The logic circuit in Figure 3(c) has three inputs (A, B, C) and two outputs (Y, Z).

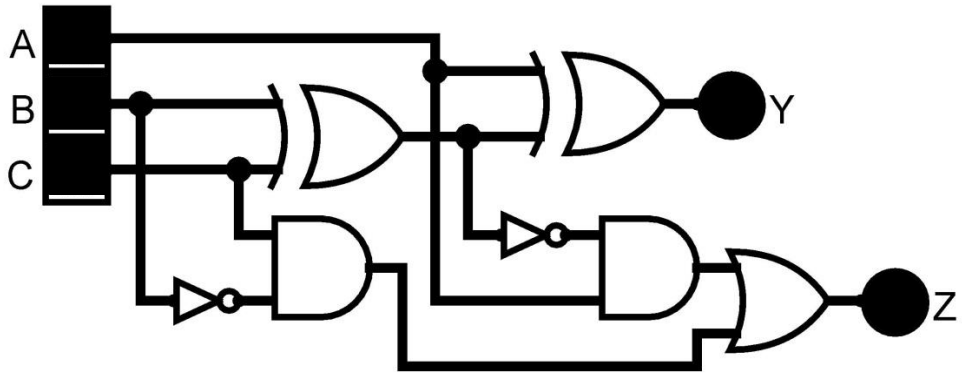

Figure 3(c)

Table 3c(i) shows a portion of a quadruple 2-input AND gates datasheet.
Table 3c(ii) shows a portion of a quadruple 2-input OR gates datasheet.
Table 3c(iii) shows a portion of a quadruple 2-input XOR gates datasheet.
Table 3c(iv) shows a portion of a hextuple NOT gates datasheet.

Table 3c(i)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	C_L = 15 pF R_L = 400Ω		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			19	ns

Table 3c(ii)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	11	4	15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	11	4	15	ns

Table 3c(iii)

Symbol	Parameter	Conditions	CL = 15 pF, RL = 400Ω		Units
			Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Other input LOW		23	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			17	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Other input HIGH		30	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			22	ns

Table 3c(iv)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	10	4	15	ns

(i) Using the datasheets given, determine the maximum propagation delay time by considering all possible paths of Figure 3(c). Show all workings clearly.

(8 marks)

(ii) Determine the maximum operating frequency that can be applied to Figure 3(c) without affecting its functionality. Show all workings clearly.

(2 marks)

Question 4

(a) Compute the 2's complement number of -216.8125_{10} in signed binary numbering system. Assuming the binary system is a 10-bit system with 8 binary points. Show all workings clearly.

(5 marks)

(b) Figure 4(b) shows a computer controlling the speed of a motor. The 0 to 2mA analog current from the DAC is amplified to produce motor speeds from 0 to 1000 revolutions per minute (rpm).

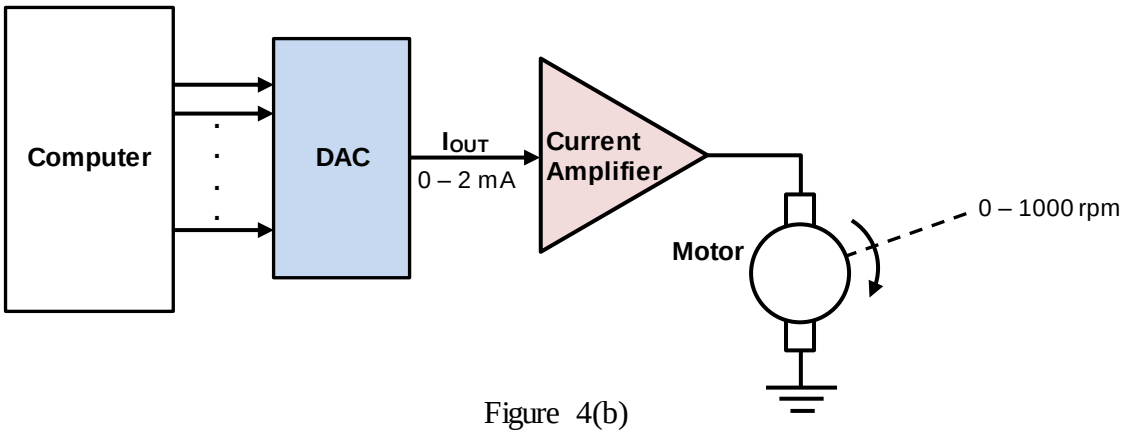

Figure 4(b)

(i) Compute the number of bits should be used if the computer is able to produce a motor speed that is within 4 rpm of the desired speed.

(5 marks)

(ii) Using the number of bits obtained in part (b)(i), compute the nearest motor speed (in rpm) achievable if 360 rpm is required.

(5 marks)

(c) Analog to Digital Converter (ADC) is an important element in signal processing for digital conversion of sensor signal. In a process to digitize a vibrating signal, an accelerometer (acceleration transducer) with the characteristics shown in Table 4(c) is used.

Table 4(c)

Sensitivity	(±5.0%) 25 mV/g
Measurement Range	±75 g peak
Frequency Range	(±5%) 10 to 15000 Hz
Sensing Element	Quartz
Weight	99 gram

Acceleration is quantified in terms of standard gravity (g). Assume the formula given is $resolution = \frac{Vrange}{2^n - 1}$.

Apply an appropriate ADC for this sensor application by computing the:

(i) Number of bits.

(7 marks)

(ii) Resolution.

(3 marks)

~THE END~