INTI
International College Penang

FINAL
Examination Paper

(COVER PAGE)

Session	:	**January 2018**
Programme	:	Diploma in Electrical and Electronic Engineering (DEEI)
Course	:	**EEE 2101: Introduction to Digital Electronics**
Date of Examination	:	8 March 2018 (Thursday)
Time	:	11:00am – 1:00pm Reading Time : Nil
Duration	:	2 Hours
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL

Materials permitted :

Non-Programmable Scientific Calculator

Materials provided :

Worksheet 4(a) & Worksheet 4(b)

Examiner(s) : **Mr. Steven Khoo Boo Tap**

Moderator : Mr. Kevin Tan Geok Su

This paper consists of 12 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE2101: INTRODUCTION TO DIGITAL ELECTRONICS
FINAL EXAMINATION: JANUARY 2018 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

A combinational logic circuit is required, which accepts BCD inputs 0000 to 1001 and displays the number '0123456789', respectively, as shown below in Figure 1(a). The BCD inputs are labelled as RSTU, R is the MSB and U is the LSB. Figure 1(b) shows a Common-Cathode 14 segment display. Assume all unused inputs as don't care.

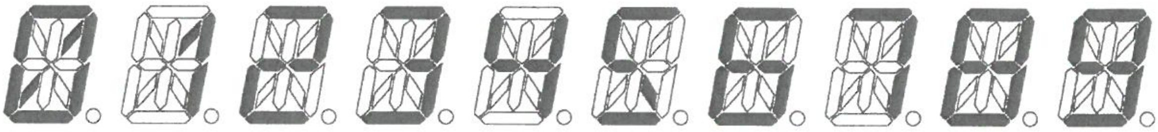

Figure 1(a)

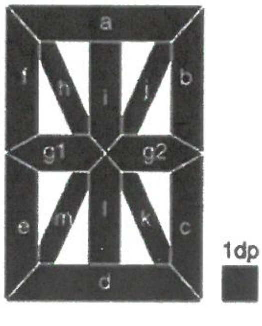

Figure 1(b)

(a) Build the truth table for the inputs to segments a through m of the 14 segment.

(4 marks)

(b) Determine the simplest SOP form of the logic expression for segments f, g1 and g2 using Karnaugh map and/or Boolean algebra.

(12 marks)

(c) Construct a logic circuit for segment f, g1 and g2 using only 2-input NAND gates with minimum gates consideration. State the number of 7400 ICs used. Show all working clearly.

(9 marks)

Question 2

(a) Table 2(a) and Table 2(b) show a portion of a dual positive edge-triggered JK flip-flops (DM7476) and a triple 3-input AND gate datasheet respectively. Figure 2(a) show the logic circuit diagram of an asynchronous counter which uses positive edge-triggered JK flip-flops with labelling of $Q_AQ_BQ_CQ_D$ where Q_D is MSB and Q_A is LSB. Assume the environment is at $T_A = 25°C$ with $V_{CC} = 5V$.

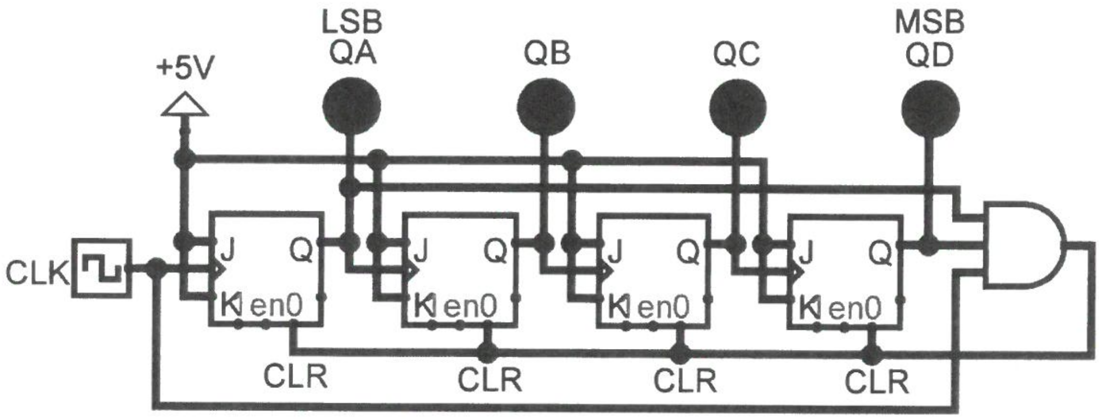

Figure 2(a)

Switching Characteristics
at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15pF$ Min	Max	Units
f_{MAX}	Maximum Clock Frequency		15		MHz
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Preset to $\overline{Q}$		40	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Preset to Q		25	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Q		40	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clear to $\overline{Q}$		25	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Q or $\overline{Q}$		40	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Q or $\overline{Q}$		25	ns

Table 2(a) JK flip-flop

Symbol	From (Input)	To (Output)	Test Conditions	Min	Typ	Max	Units
t_{PLH}	A, B or C	Y	C_L = 15 pF, $R_L = 2k\Omega$		8	27	ns
t_{PHL}					10	19	ns

Table 2(b) AND gate

(i) Analyse its operation to determine whether the logic circuit of Figure 2(a) is working as a counter or not. If not working, justify and suggest a suitable modification for the logic circuit to function as a counter.

(3 marks)

(ii) Find the total propagation delay from the given datasheets in Table 2(a) and Table 2(b).

(4 marks)

(iii) Find the maximum frequency at which the counter can be operated stably.

(2 marks)

(iv) Determine the output timing diagram of Figure 2(a) with proper labelling and state the exact function of this counter.

(4 marks)

(b) Determine the following number system transformation. Show all workings clearly.

(i) $[2018.2018_{16} - 1005.1005_{16}]$ to decimal equivalent with 5 decimal points accuracy.

(4 marks)

(ii) $[12017.01_{8} \times 15_{10}]$ to hexadecimal equivalent with 2 hexadecimal points accuracy.

(4 marks)

(iii) $[163.0703125_{10} - 12.018_{16}]$ to binary equivalent with 9 binary points accuracy.

(4 marks)

Question 3

(a) Table 3(a) shows a portion of quadruple 2-input NAND gates (SN74ALS00A) datasheet. Find the following parameters from this datasheet, show all working clearly:

(i) Fan-out, a gate can safely drive.

(3 marks)

(ii) Average Power dissipation, $P_{D\,(avg)}$ for one gate on a 74ALS00 IC.

(4 marks)

(iii) Propagation delay, t_{PD}.

(2 marks)

recommended operating conditions

		SN54ALS00A MIN	SN54ALS00A NOM	SN54ALS00A MAX	SN74ALS00A MIN	SN74ALS00A NOM	SN74ALS00A MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8‡			0.8	V
				0.7§				
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

‡ Applies over temperature range −55°C to 70°C
§ Applies over temperature range 70°C to 125°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS00A MIN	SN54ALS00A TYP†	SN54ALS00A MAX	SN74ALS00A MIN	SN74ALS00A TYP†	SN74ALS00A MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−20		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0		0.5	0.85		0.5	0.85	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.5	3		1.5	3	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§ SN54ALS00A MIN	SN54ALS00A MAX	SN74ALS00A MIN	SN74ALS00A MAX	UNIT
t_{PLH}	A or B	Y	3	15	3	11	ns
t_{PHL}			2	9	2	8	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

Table 3(a)

(b) Figure 3(b) shows the pin diagram and logic symbol of 74LS283 4-bit adder with (pin numbers in parentheses). Illustrate how two 74LS283 adders can be connected to form an 8-bit parallel adder. Determine output bits for the following 8-bit input numbers: $A_8A_7A_6A_5A_4A_3A_2A_1 = 10111001$ and $B_8B_7B_6B_5B_4B_3B_2B_1 = 1001110$. Show the adders with proper interconnections. Indicate the Low-order adder and High-order adder in details.

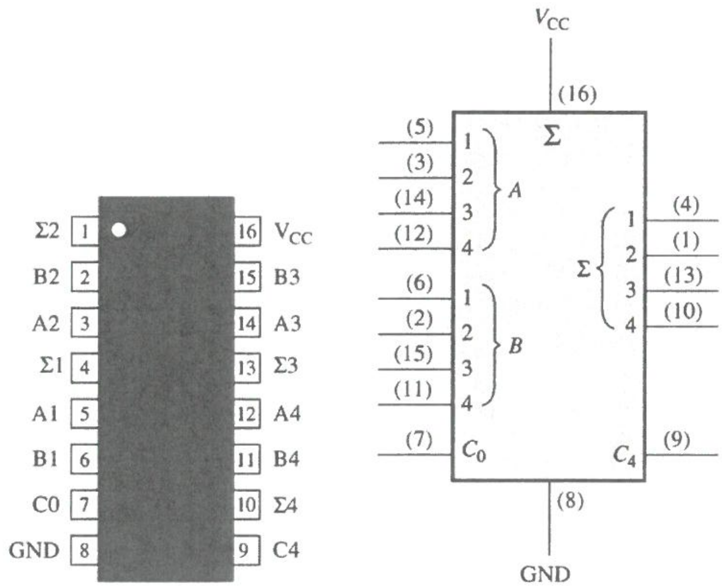

Figure 3(b)

(8 marks)

(c) Figure 3(c) shows the logic symbol of 74HC154 4-bit (1-of-16) decoder with (pin numbers in parentheses). A certain application requires that a 5-bit number be decoded. Use 74HC154 decoders to implement the logic. The binary number is represented by the format $A_4A_3A_2A_1A_0$. Provide details explanation of the fifth bit, A_4 implementation.

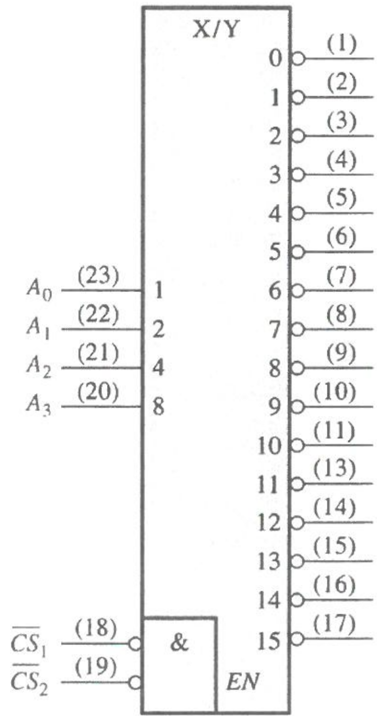

Figure 3(c)

(8 marks)

Question 4

(a) A T flip-flop is connected as shown below in Figure 4(a)(i). Sketch the output, Q with the given input, Y waveform as shown below in Figure 4(a)(ii). The Q is initially at HIGH. Assume that there is no propagation delay issue and the flip-flop has been enabled.

Note: Use **Worksheet 4(a)** to answer this question, detach Worksheet 4(a) and tie with the answer booklet.

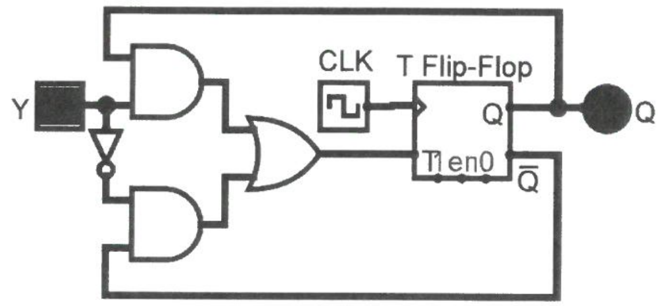

Figure 4(a)(i)

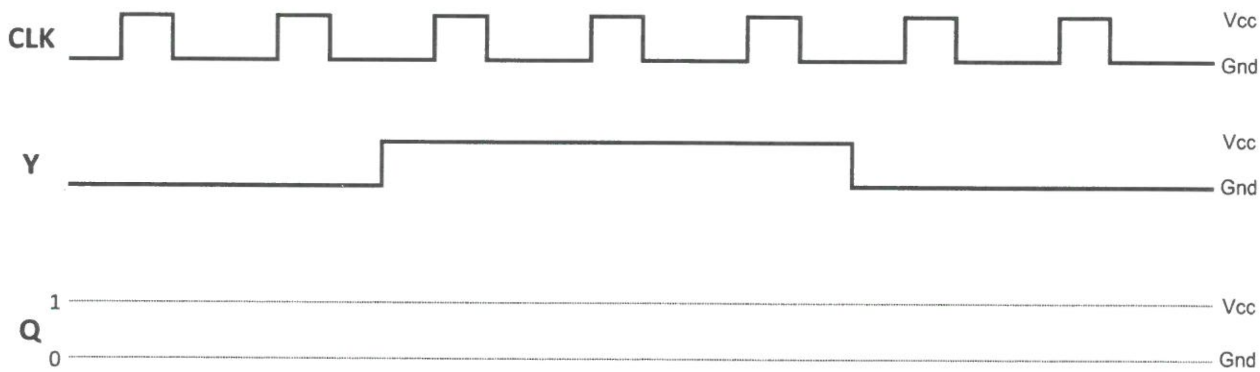

Figure 4(a)(ii)

(5 marks)

(b) A D flip-flop is connected as shown below in Figure 4(b)(i). Sketch the output, Q with the given inputs, A and B waveforms as shown in Figure 4(b)(ii). The Q is initially at LOW. Assume that there is no propagation delay issue and the flip-flop has been enabled.

Note: Use **Worksheet 4(b)** to answer this question, detach Worksheet 4(b) and tie with the answer booklet.

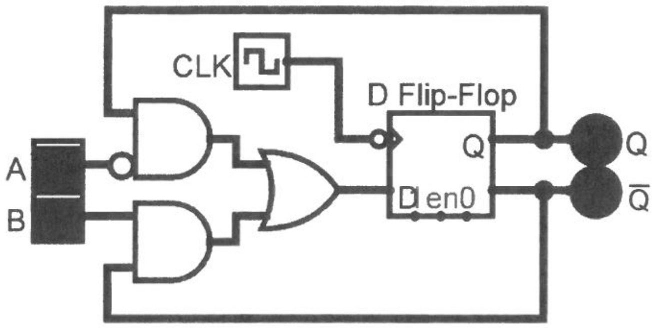

Figure 4(b)(i)

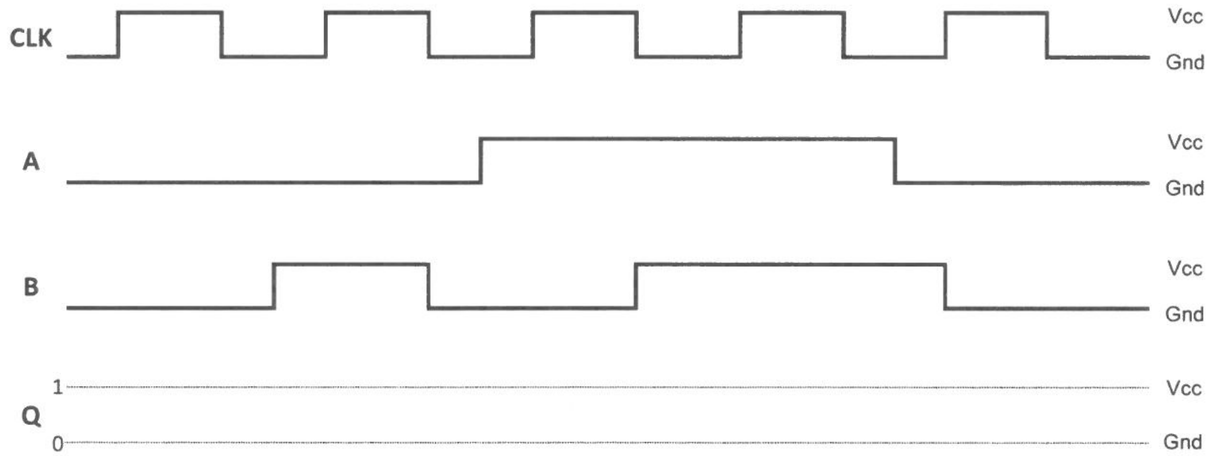

Figure 4(b)(ii)

(5 marks)

(c) The four inputs (W, X, Y, Z) to a communication network system block diagram represent an 8421 code as shown in Figure 4(c). The output (F) is 1 if the decimal number represented by the inputs is exactly divisible by 2. Assume that only valid 8421 codes occur as inputs, other inputs will be treated as 0 for the output. Show all workings clearly.

Figure 4(c)

(i) Give the complete truth-table of the network system.
(3 marks)

(ii) Use Karnaugh map to obtain the simplest expression for the network system.
(3 marks)

(iii) Sketch the logic circuit for the network system using only NAND gates with minimum gates and IC consideration. Assume that the complements of the variables are available.
(3 marks)

(iv) Build the expression obtained in Question 4(c)(ii) using an 8-to-1 MUX with Z as the select line.
(3 marks)

(v) If the company had decided to use only NOR gates for the network design, determine the complete simplest circuit for the network with minimum gates consideration. Assume that the complements of the variables are available.
(3 marks)

Question 5

(a) Table 5(a) shows the current ratings of TTL series logic gates. A 74AS08 AND gate output is driving **4** Standard TTL gate inputs, **2** Advanced Low-Power Schottky gate inputs and **14** Low-Power Schottky gate inputs. Determine if there is a loading problem.
(4 marks)

TTL Series	Output Drive		Input Loading	
	I_{OH}	I_{OL}	I_{IH}	I_{IL}
74	400μA	16mA	40μA	1.6mA
74S	1.0mA	20mA	50μA	2.0mA
74LS	400μA	8mA	20μA	400μA
74AS	2.0mA	20mA	200μA	2.0mA
74ALS	400μA	8mA	20μA	100μA
74F	1.0mA	20mA	20μA	600μA

Table 5(a)

The 74AS08 AND gate output needs to be used to drive some 74F inputs in addition to the load inputs. Determine how many additional 74F inputs could the output drive without being overloaded?

(3 marks)

(b) Illustrate the function using an appropriate multiplexer (MUX) with other logic gates, taking into consideration of minimum gates count as well.

(i) $F_1(R,S,T,U) = \sum(3,4,6,7,8,10,12,14)$ with RT as the select lines.

(4 marks)

(ii) $F_2(W,X,Y,Z) = \sum(0,2,5,6,10,11,12,15)$ with X as the select line.

(4 marks)

(c) Construct a 2-bit up/down counter using positive edge-triggered D flip-flop for MSB and JK flip-flop for LSB. Input Z will be used as the up/down control. The counter will count from 0 ⇨ 1 ⇨ 2 ⇨ 3 ⇨ 0 for count up when input, Z = 0 and 3 ⇨ 2 ⇨ 1 ⇨ 0 ⇨ 3 for counting down when input, Z = 1 as shown below in Figure 5(c). Label the output as Q_1Q_0 where Q_1 for MSB and Q_0 for LSB. Show all working steps clearly.

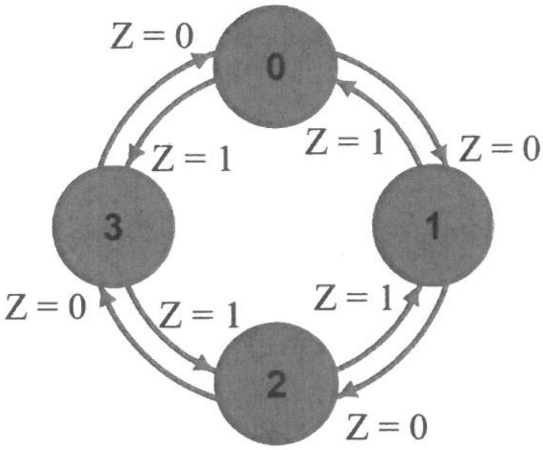

Figure 5(c)

(i) Write all excitation tables used.

(2 marks)

(ii) Prepare the transition table/ next state table.

(3 marks)

(iii) Simplify using Karnaugh map and/or Boolean algebra.

(3 marks)

(iv) Sketch the complete logic circuit diagram with proper label.

(2 marks)

Question 6

(a) For the pulse shown in Figure 6(a) below, find the Rise time, Fall time, Pulse time and Amplitude from the graph as accurate as possible.

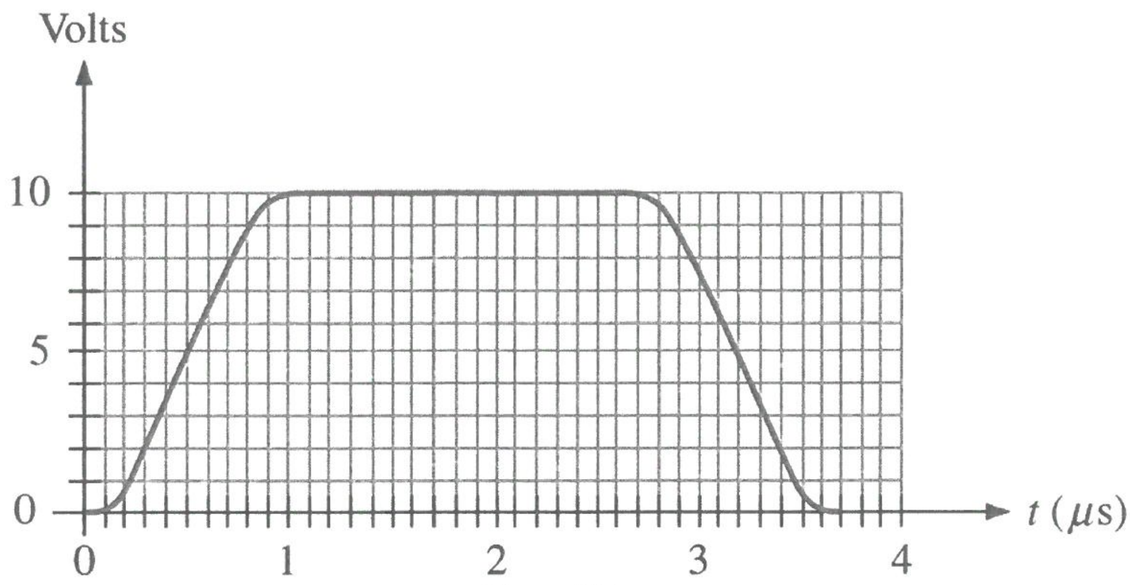

Figure 6(a)

(6 marks)

(b) A 14-bit DAC produces an output current in proportion to its digital input. For a digital input of 0010100000, an output current of 75mA is produced.

(i) Find the output current be if the digital input is 001100011110.

(3 marks)

(ii) Find the maximum output current produced by this DAC.

(3 marks)

(iii) Find the digital input if a 1805mA output current is required.

(3 marks)

(c) A binary-weighted-input DAC is shown in Figure 6(c). If the LSB bit resistor has a value of 480kΩ, calculate the values of the other input resistors. Also, determine the V_{out} if the DAC has a binary input of 1010 with Logic 1 (HIGH) as +6.0V and Logic 0 (LOW) as 0V. Assume that R_f equals to 10kΩ.

(6 marks)

Compare between Binary Weighted DAC versus R2R ladder DAC using a table.

(4 marks)

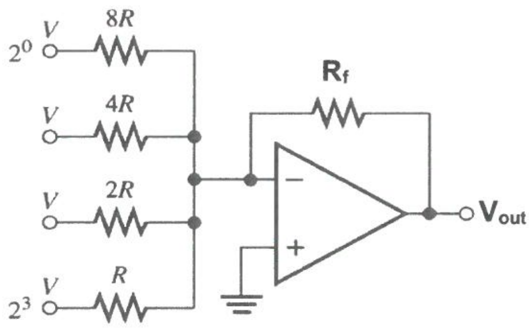

Figure 6(c)

– THE END –

EEE2101(F)/Jan18/Steven Khoo/16/01/18

Worksheet 4(a)

(a) A T flip-flop is connected as shown below in Figure 4(a)(i). Determine the output, Q with the given input, Y waveform as shown below in Figure 4(a)(ii). The Q is initially at HIGH. Assume that there is no propagation delay issue and the flip-flop has been enabled.

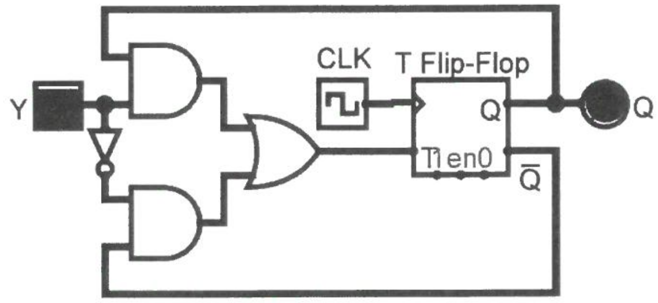

Figure 4(a)(i)

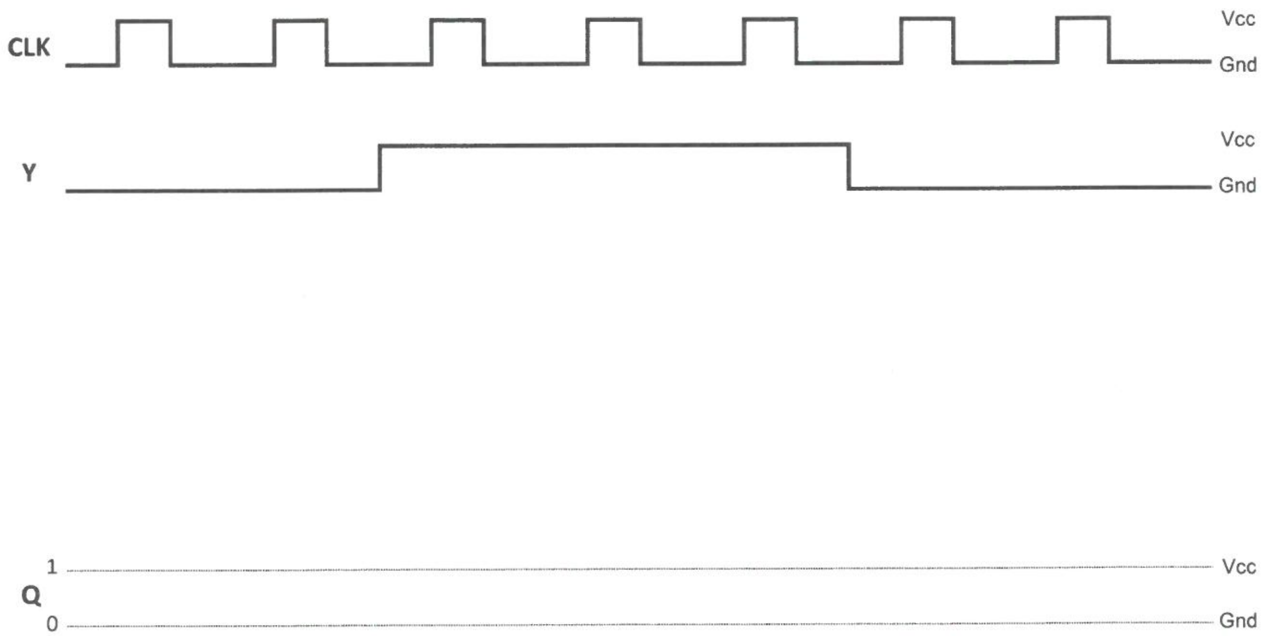

Figure 4(a)(ii)

(5 marks)

Worksheet 4(b)

(b) A D flip-flop is connected as shown below in Figure 4(b)(i). Determine the output, Q with the given inputs, A and B waveforms as shown in Figure 4(b)(ii). The Q is initially at LOW. Assume that there is no propagation delay issue and the flip-flop has been enabled.

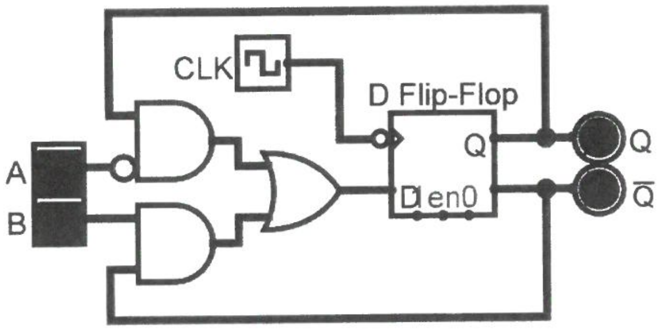

Figure 4(b)(i)

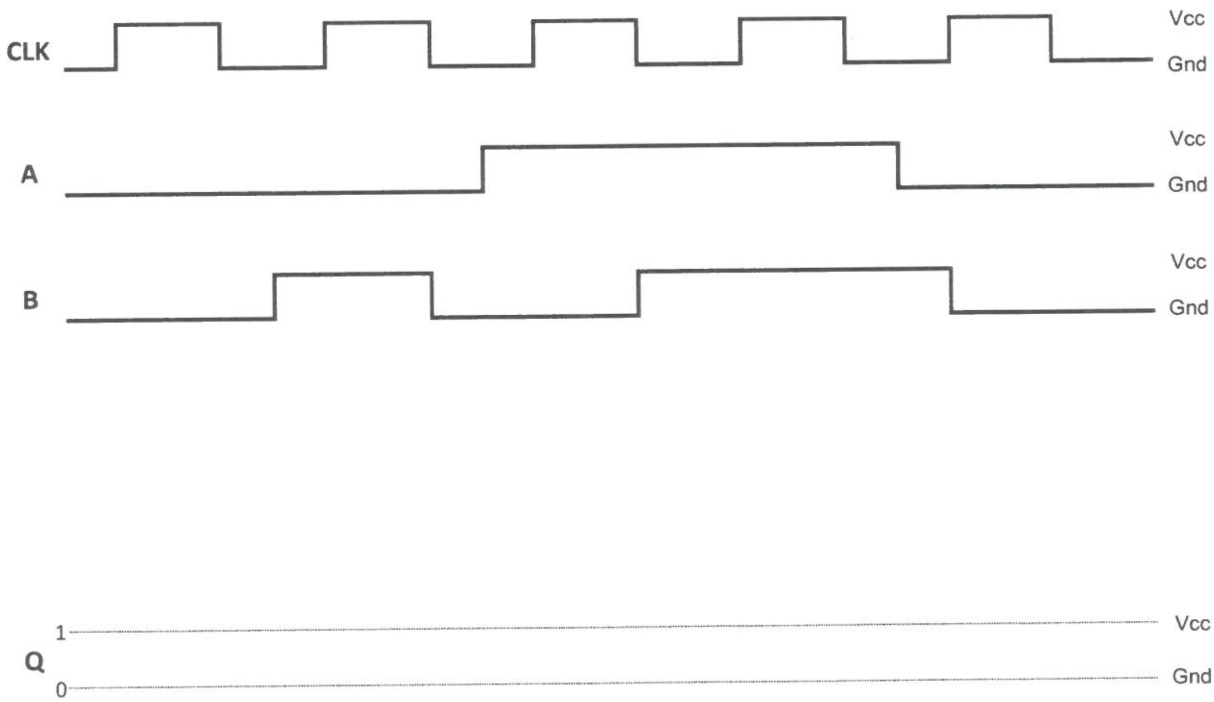

Figure 4(b)(ii)

(5 marks)