INTI International College Penang

FINAL
ALTERNATIVE ASSESSMENT

(COVER PAGE)

Session	:	**August 2020**
Programme	:	Diploma in Electrical & Electronic Engineering (DEEI)
Course	:	**EEE2101: Introduction to Digital Electronics**
Date of Examination	:	15 December 2020 (Tuesday)
Time	:	8.00am – 11.00am Reading Time : Nil
Duration	:	3 Hours

Special Instructions :

This paper consists of **FOUR (4)** questions. Answer **ALL** questions. All questions carry equal marks.

Material permitted :
Non-Programmable Scientific Calculator

Materials provided :
Nil

Examiner(s)	:	**Steven Khoo Boo Tap**
Chief Moderator	:	Chan Tse Wei

*This paper consists of **8** printed pages, including the cover page*

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE2101: INTRODUCTION TO DIGITAL ELECTRONICS
FINAL ALTERNATIVE ASSESSMENT: AUGUST 2020 SESSION

Instructions: This paper consists of **FOUR (4)** questions. Answer **ALL** questions. All questions carry equal marks.

Question 1

(a) Present the following Boolean expressions to the stated simplest form, using the specified method:

(i) $F_1(X,Y,Z) = (X+Y+Z)(X+\bar{Y}+Z)(\bar{X}+Y+Z)(\bar{X}+Y+\bar{Z})$
Simplest Form: POS.
Method: Boolean Algebra.

(3 marks)

(ii) $F_2(A,B,C,D) = \sum m(0,1,2,3,5,7,8,9) + d(10,11,12,13,14,15)$
Simplest form: minimum 2-input NOR gates implementation.
Method: Karnaugh Map.

(4 marks)

(iii) $F_3(R,S,T,U) = \prod M(1,5,7,11,12,14) \cdot \prod d(3,9)$
Simplest form: Any type of gate implementation deemed appropriate.
Method: Karnaugh Map.

(5 marks)

(b) Produce the simplest Boolean expressions for Y in Figure 1(b) and show how it can be implemented using only ONE Integrated Circuit (IC). State the part number of that IC for the simplified design. Show all workings clearly.

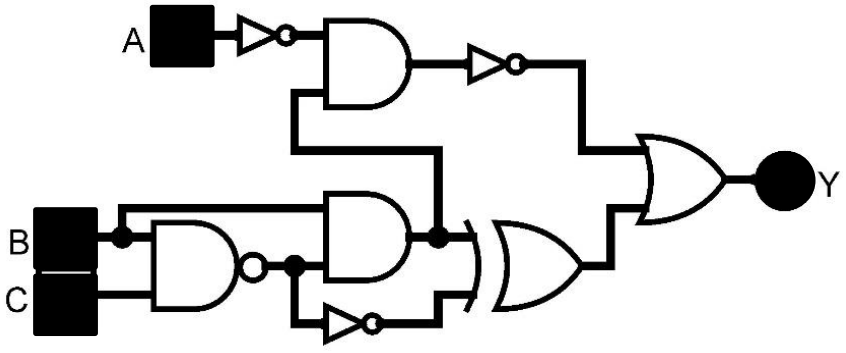

Figure 1(b)

(8 marks)

(c) Solve the numbering system transformation of [161.0703125_{10} – 1001.001000001_2] to hexadecimal equivalent with 3 hexadecimal points accuracy. Show all workings clearly.

(5 marks)

Question 2

(a) Figure 2(a) shows the logic circuit diagram of an asynchronous counter, which uses positive edge-triggered T flip-flops with labelling of $Q_AQ_BQ_C$ where Q_C is MSB and Q_A is LSB.

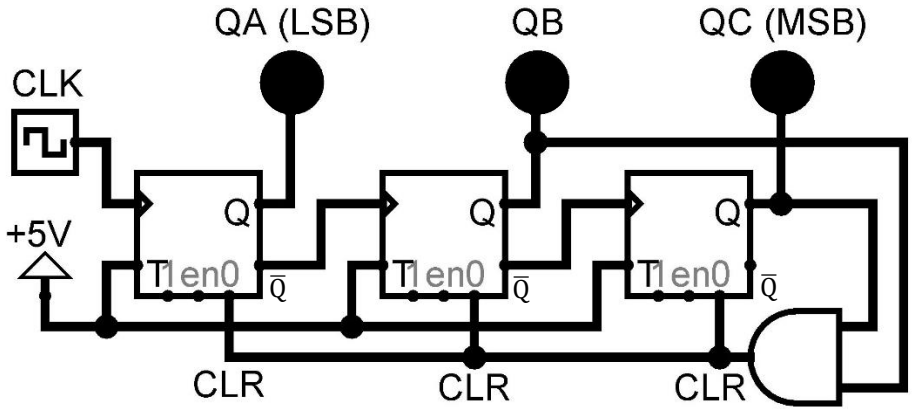

Figure 2(a)

(i) Verify if the counter operation of Figure 2(a) is working as an up counter or down counter. Also, state the modulus and function of this counter.

(5 marks)

(ii) Show the timing diagrams of counter's outputs, Q_A, Q_B and Q_C, with proper labelling.

(5 marks)

(b) Produce a synchronous 3-bit up/down counter using positive edge-triggered D flip-flop for MSB, JK flip-flop for second bit and SR flip-flop for LSB. Assume D_A is the MSB input, J_B & K_B are the next flip-flop inputs and S_C & R_C are the LSB inputs. Assume all unused states as don't care if applicable.

Input Y will be used as the up/down control. The counter will count from 0 ⇨ 2 ⇨ 4 ⇨ 3 ⇨ 7 ⇨ 1 ⇨ 6 ⇨ 5 ⇨ 0 when input, Y = 0 and 0 ⇨ 5 ⇨ 6 ⇨ 1 ⇨ 7 ⇨ 3 ⇨ 4 ⇨ 2 ⇨ 0 when input, Y = 1 as shown below in Figure 2(b). Flip-flop D_A has output Q_A, flip-flop J_BK_B has output Q_B and flip-flop S_CR_C has output Q_C.

Show all workings according to the procedures listed in part (b)(i), (b)(ii) and (b)(iii). Use the flip-flop excitation tables provided in Table 2(b).

Table 2(b)

Outputs		Inputs	
Q_n	Q_{n+1}	S	R
0	0	0	×
0	1	1	0
1	0	0	1
1	1	×	0

Outputs		Inputs	
Q_n	Q_{n+1}	J	K
0	0	0	×
0	1	1	×
1	0	×	1
1	1	×	0

Outputs		Input
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Outputs		Input
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Q_n: Present State
Q_{n+1}: Next State

(i) Prepare the transition table/next state table for the up/down counter.

(4 marks)

(ii) Produce the simplest Boolean expressions for D_A, J_B, K_B, S_C and R_C inputs using Karnaugh map and/or Boolean algebra.

(5 marks)

(iii) Construct the logic circuit diagram for the simplified Boolean expressions obtained in part (b)(ii) using D, JK, SR flip-flops and other logic gates with proper labelling.

(6 marks)

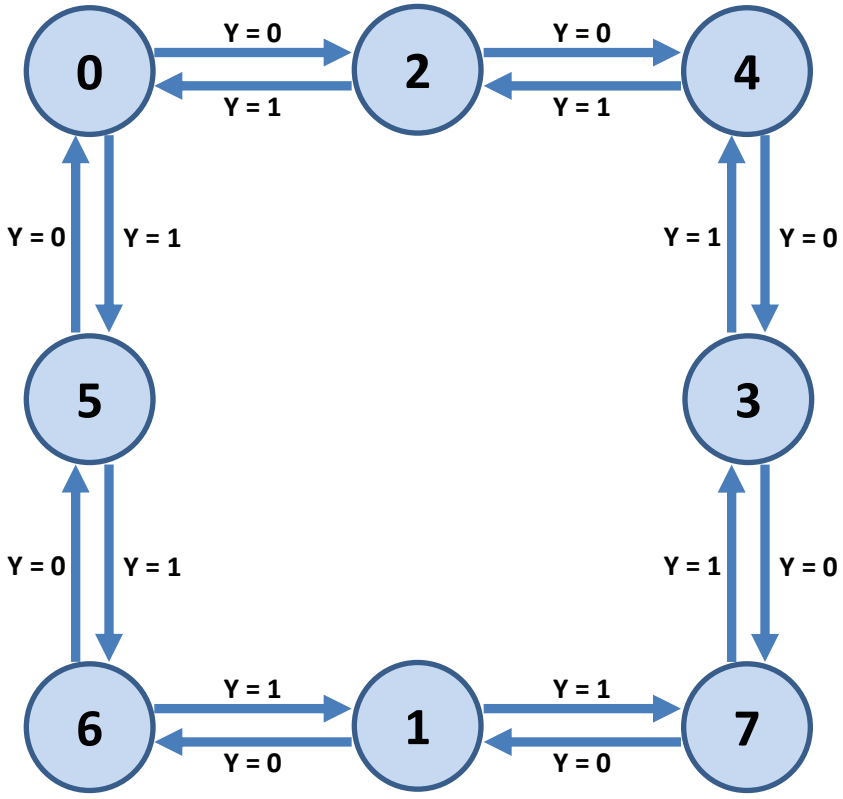

Figure 2(b)

Question 3

(a) Solve the numbering system transformation of [$156.32_8 \times A.A_{16}$] to binary equivalent with 8 binary points accuracy. Show all workings clearly.

(5 marks)

(b) Table 3(b) shows a portion of quadruple 2-input OR gates (DM74LS32) datasheet. Compute the following parameters from this datasheet, show all workings clearly:

(i) Power dissipation, $P_{D(max)}$ on a DM74LS32 IC when the output condition is as shown in Figure 3(b). Assume that the V_{CC} used is 5.25V.

(6 marks)

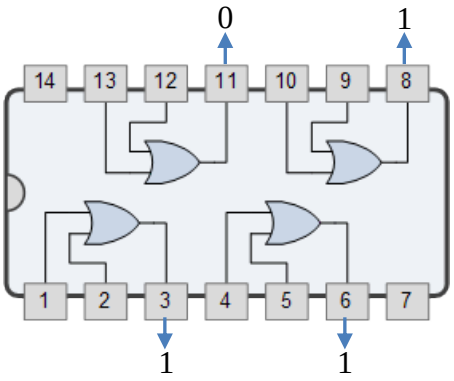

Figure 3(b)

(ii) Fan-out, a gate can safely drive.

(3 marks)

(iii) Noise Margin voltages, V_{NL} and V_{NH}.

(3 marks)

Table 3(b)

Recommended Operating Conditions

Symbol	Parameter	DM54LS32			DM74LS32			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			6	12	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			18	33	mA

(c) Table 3(c) shows the current ratings of TTL series logic gates. A 74S04 NOT gate output is driving a few other TTL inputs as shown in Figure 3(c).

(i) Discover through calculation whether there is a loading problem.

(5 marks)

Table 3(c)

TTL Series	Output Drive		Input Loading	
	I_{OH}	I_{OL}	I_{IH}	I_{IL}
74	400µA	16mA	40µA	1.6mA
74S	1.0mA	20mA	50µA	2.0mA
74LS	400µA	8mA	20µA	400µA
74AS	2.0mA	20mA	200µA	2.0mA
74ALS	400µA	8mA	20µA	100µA
74F	1.0mA	20mA	20µA	600µA

(ii) The 74S04 NOT gate output needs to drive some 74AS inputs in addition to the loads shown in Figure 3(c). Compute the additional number of 74AS inputs that can be driven by the output of the 74S04 NOT gate.

(3 marks)

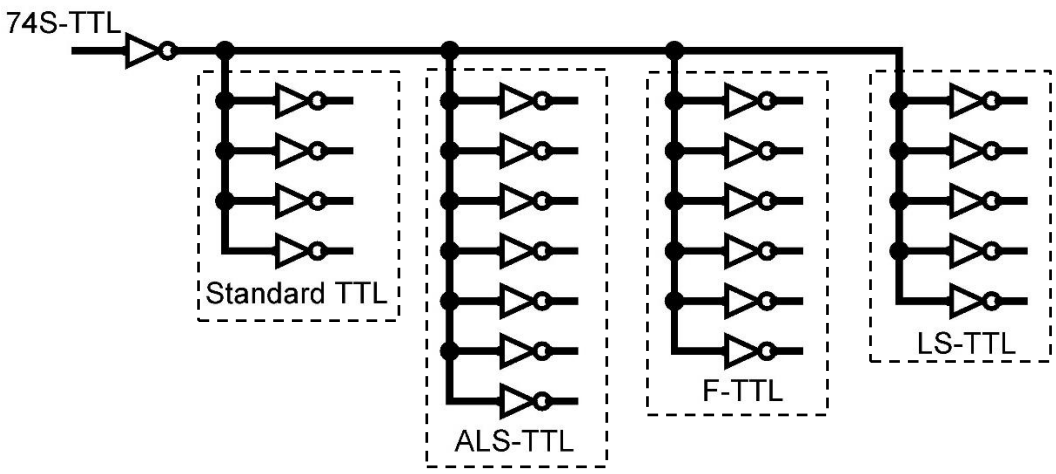

Figure 3(c)

Question 4

(a) Compute the 2's complement number of -46.03125_{10} in signed binary numbering system. Assuming the binary system is 8-bit system with 8 binary points. Show all workings clearly.

(5 marks)

(b) Figure 4(b) shows a computer controlling the speed of a motor. The 0 to 2mA analog current from the DAC is amplified to produce motor speeds from 0 to 1000 rpm (revolutions per minute).

(i) Compute the number of bits should be used if the computer is able to produce a motor speed that is within 2 rpm of the desired speed.

(5 marks)

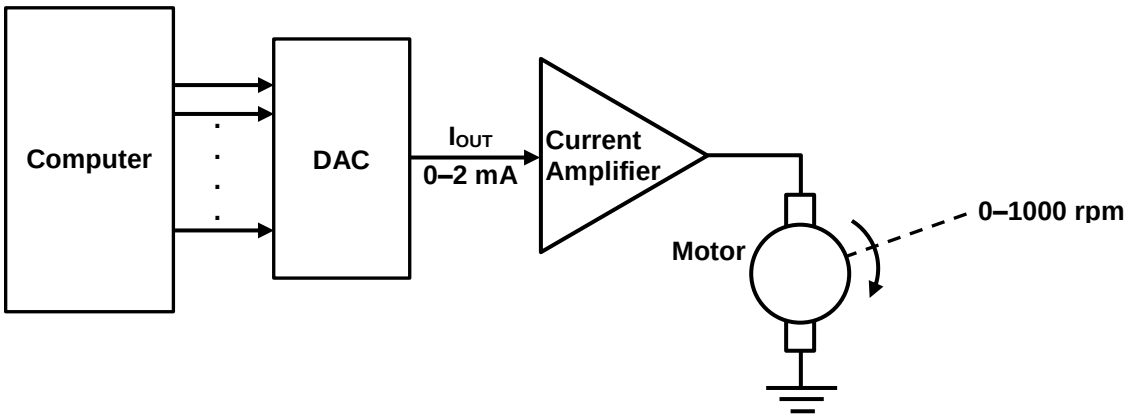

Figure 4(b)

(ii) Using the number of bits obtained in part (b)(i), compute the nearest motor speed (in rpm) achievable if 256 rpm is required.

(5 marks)

(c) Analog to Digital Converter (ADC) is an important element in signal processing for digital conversion of sensor signal. In the case of digitizing a vibration signal measured by an accelerometer with the following characteristics (PCB-301A10):

Sensitivity	(±2.0%) 100 mV/g
Measurement Range	±100 g peak
Frequency Range	(±5%) 0.5 to 10000 Hz
Sensing Element	Quartz
Weight	176 gm

Assume the formula given is $resolution = \frac{Vrange}{2^n - 1}$. Apply an appropriate ADC for this sensor application by computing the number of bits and the resolution.

(10 marks)

~THE END~