INTI International College Penang

FINAL
ALTERNATIVE ASSESSMENT

(COVER PAGE)

Session	:	**August 2020**
Programme	:	Diploma in Electrical & Electronic Engineering (DEEI)
Course	:	**EEE1106: Analogue Electronics**
Date of Examination	:	14 December 2020 (Monday)
Time	:	2.00pm – 5.00pm Reading Time : Nil
Duration	:	3 Hours

Special Instructions :

This paper consists of **FOUR (4)** questions. Answer **ALL FOUR (4)** questions. All questions carry equal marks.

Material permitted :
Non-Programmable Scientific Calculator

Materials provided :
Nil

Examiner(s)	:	**Dr. Su Hsiao Wei**
Chief Moderator	:	Chai Yoon Yik

*This paper consists of **9** printed pages, including the cover page*

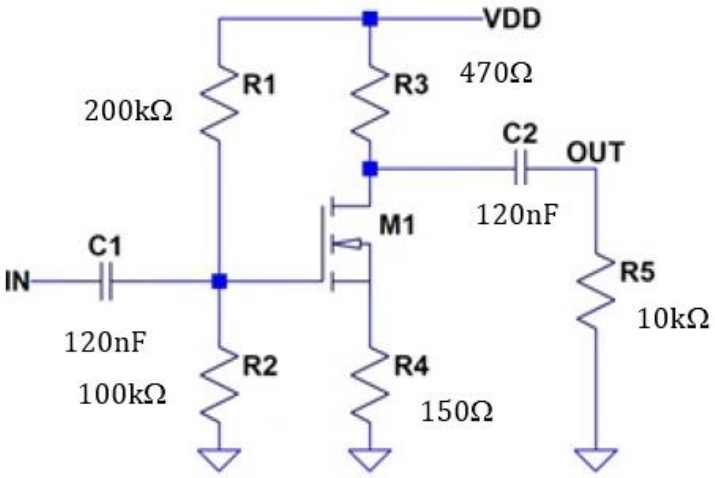
INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE1106: ANALOGUE ELECTRONICS
FINAL ALTERNATIVE ASSESSMENT: AUGUST 2020 SESSION

Instructions: This paper consists of **FOUR (4)** questions. Answer **ALL FOUR (4)** questions. All questions carry equal marks.

Question 1

(a) Figure 1(a) shows a single stage FET amplifier and its voltage gain frequency response.



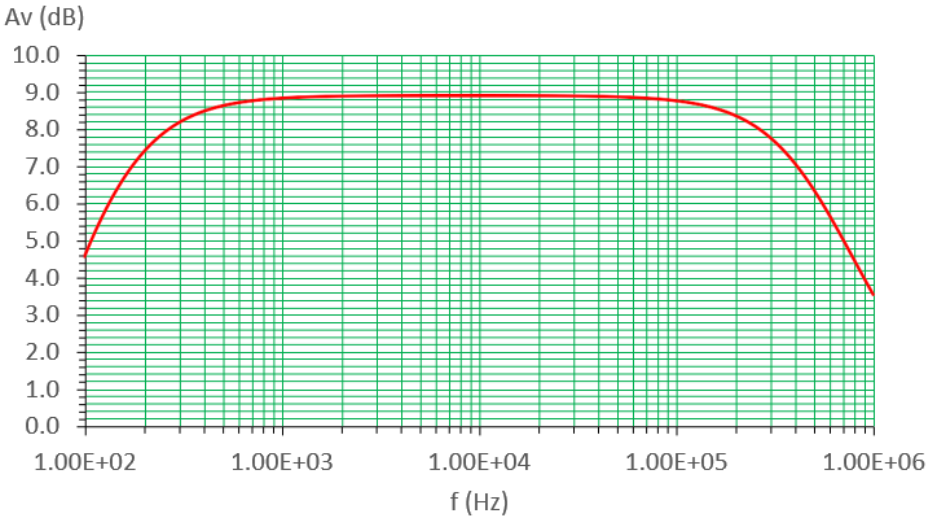


Figure 1(a)

(i) Identify which circuit components contribute to the gain reduction at the low frequency band. Explain electrically how these components cause the gain reduction.

(2 marks)

(ii) Identify and explain the components that contribute to the gain reduction at the high frequency band. Explain a way to increase the amplifier upper cutoff frequency.

(3 marks)

(iii) Find the upper and lower cutoff frequencies from the amplifier voltage gain frequency response. Then estimate the bandwidth of the amplifier. Explain a way to reduce the amplifier lower cutoff frequency, state any assumption made.

(4 marks)

(b) Figure 1(b) shows a single-stage E-MOSFET amplifier suitable for low-voltage low-power applications. The E-MOSFET has the following parameter values:
$I_{DQ} = 200\mu A @ V_{GSQ} = 1.5V$

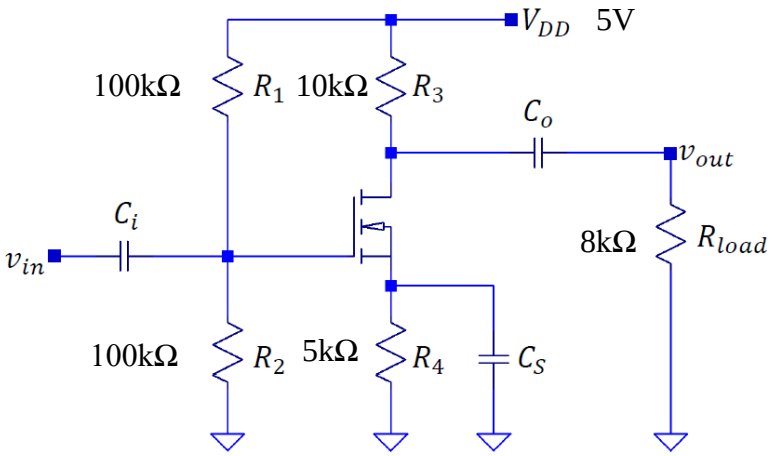


Figure 1(b)

(i) Explain the important of DC biasing for this amplifier.

(2 marks)

(ii) Explain the influence on the DC biasing of the amplifier if capacitors C_i and C_o are shorted.

(2 marks)

(iii) Calculate the quiescent voltages $V_{GQ}, V_{DQ}, V_{SQ}, and\ V_{DSQ}$.

(4 marks)

(iv) If the maximum allowed power consumption at the $R_1 - R_2$ branch is $50\mu W$, calculate the minimum value for $(R_1 + R_2)$.

(2 marks)

(c) Figure 1(c) shows the AC equivalent circuit model of an FET voltage amplifier.

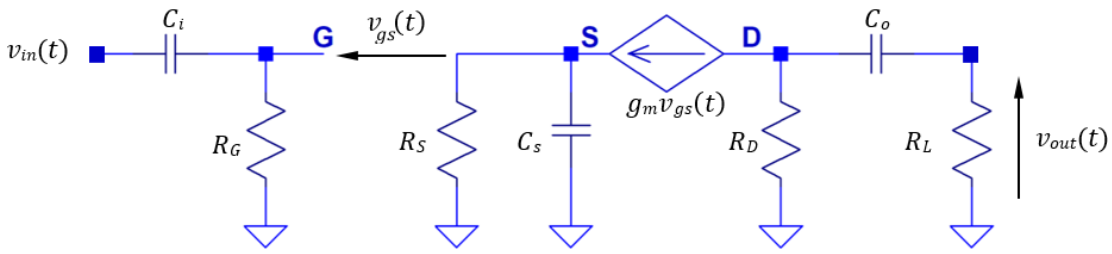


Figure 1(c)

(i) Modify the AC equivalent circuit model to evaluate the cutoff frequency contributed by capacitor C_o.

(2 marks)

(ii) Utilizing the AC equivalent circuit model obtained in part 1(c)(i), show that the voltage transfer function of $V_{OUT}(s)/V_{IN}(s)$ can be expressed in the form of,

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{a_0 s}{s + \omega_o}$$

and state a_0 and ω_o in terms of the relevant passive components and transistor parameter, g_m. Obtain the cutoff frequency of the amplifier which is contributed by capacitor C_o.

(4 marks)

Question 2

(a)

(i) Draw the schematic diagrams of both non-inverting and inverting amplifiers each utilizing a single op-amp, operating in dual supply mode.

(2 marks)

(ii) Using circuit analysis principle, derive the voltage transfer function expression of the amplifiers given in part 2(a)(i). State the assumption(s) in your analysis.

(3 marks)

(iii) Sketch input V_{in} and output V_{out} waveforms as a function time for each of the amplifier in part 2(a)(i) with the closed-loop voltage gain of 2 and $V_{in} = \sin(2\pi(1000)t)$. Label your sketch clearly.

(3 marks)

(iv) Explain a way to implement an amplifier circuit using only inverting amplifier(s), such that the overall input and output signals are in-phase.

(2 marks)

(b) Figure 2(b) shows a non-inverting amplifier implemented using an op-amp with the following specifications:

$Vs(max)$ = ±9 V
$slew\ rate$ = 8 V/μs
$|V_{out(sat)}| = |Vsupply| - 0.5$ V
If v_{in} = 2sin(200000πt), do the following.

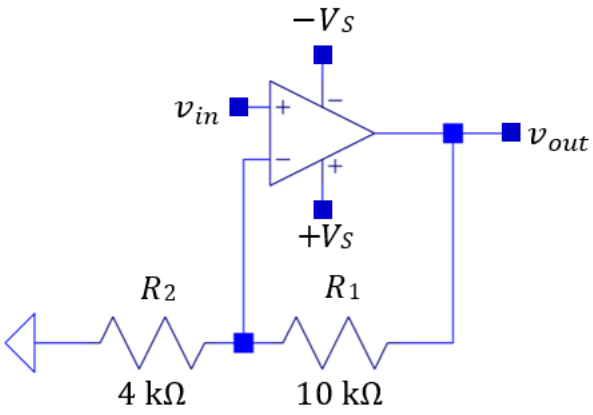


Figure 2(b)

(i) Calculate the maximum output voltage V_{out} of the amplifier. Justify the suitability of the op-amp implementation from the saturation voltage point of view.

(3 marks)

(ii) Calculate the maximum rate of change of the amplifier output. Justify the suitability of the op-amp implementation from the slew-rate point of view.

(4 marks)

(c) Figure 2(c) shows a Schmitt triggered comparator with reference voltage circuitry. Analyse the entire circuit, calculate relevant voltage levels and sketch the voltage transfer curve of the comparator circuit and clearly show the saturated output voltage levels, the upper and lower threshold points of the circuit. Assume that the op-amps used in the circuit have rail-to-rail output. Show all your workings clearly.

(8 marks)

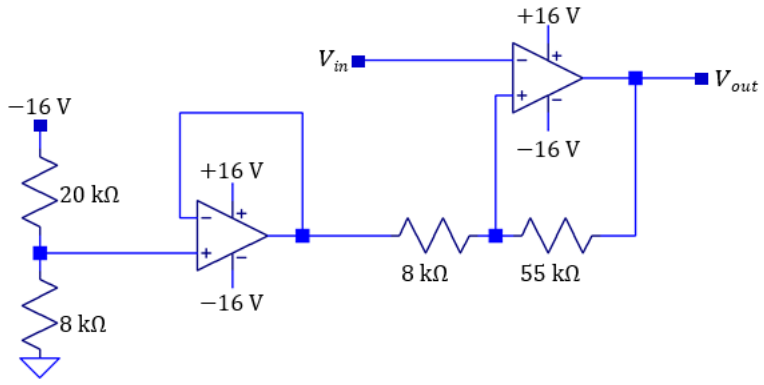


Figure 2(c)

Question 3

(a) Clearly state in a table form, two pros and two cons between passive filters and active filters in general.

(4 marks)

(b) The voltage transfer function of a filter circuit is given as,

$$T(s) = \frac{a_0 s}{s^2 + b_1 s + b_0}$$

(i) Identify the type and order of the filter.

(1 mark)

(ii) Identify the cut-off frequency of the filter.

(1 mark)

(iii) Explain in general with the aid of a diagram and frequency spectrums how to conceptually implement a band-pass filter from a high-pass filter and a low-pass filter.

(3 marks)

(iv) Based on the concept in part (iii) and using only a single non-inverting op-amp, draw an overall schematic diagram of an active filter that has the similar voltage transfer function and derive the voltage transfer function. Determine the values of a_0, b_0, and b_1 in terms of the circuit components by comparing the filter transfer function against a standard transfer function.

(9 marks)

(c) A filter is realized by cascading two same stages and the overall transfer function is expressed as

$$T(s) = \left(\frac{2s}{2s + 40}\right)\left(\frac{2s}{2s + 40}\right)$$

(i) Identify the type and order of the filter.

(3 marks)

(ii) Calculate the cutoff frequency in rad/s.

(2 marks)

(iii) Identify the filter type (passive or active). Justify your answer.

(2 marks)

Question 4

(a) In general, explain the followings pertaining to an oscillator circuit.

(i) Operation.

(2 marks)

(ii) Output design requirements.

(2 marks)

(b) Figure 4(b) shows a design example of a relaxation oscillator assembled from a 555 timer IC.

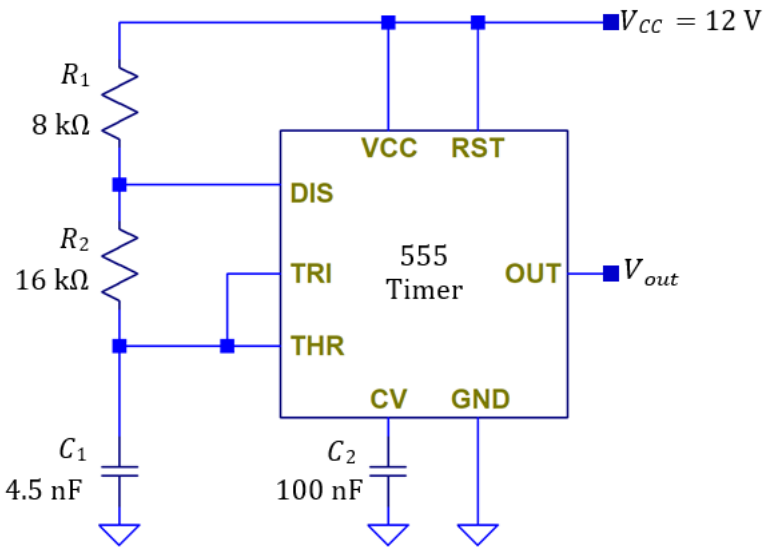


Figure 4(b)

(i) Calculate the oscillation frequency of the output signal V_{out}.

(3 marks)

(ii) Calculate the duty cycle of the output signal in %.

(3 marks)

(iii) Suggest and explain the method to allow this oscillator to produce an output signal with duty cycle less than 50%. Based on the suggested method, calculate the duty cycle of the output signal in %.

(4 marks)

(iv) State the limitation of the method suggested in part (b)(iii).

(2 marks)

(c) Figure 4(c) shows an analogue oscillator circuit.

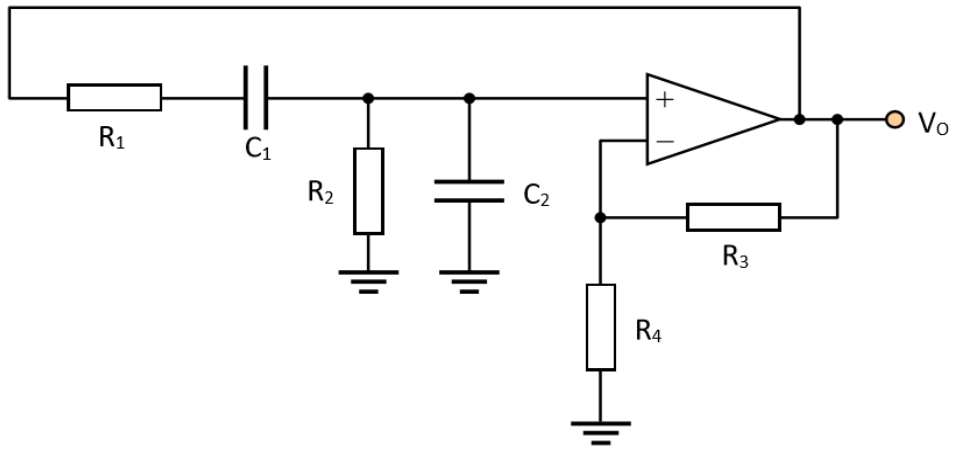


Figure 4(c)

(i) State the name of this oscillator circuit.

(1 mark)

(ii) State the expression of the resonant frequency of the circuit.

(2 marks)

(iii) If $R_1 = R_2 = 8$ kΩ and $C_1 = C_2 = 1$ nF, calculate the output frequency.

(2 marks)

(iv) State the relationship between R_3 and R_4 for the circuit to sustain oscillation and explain the reason for such relationship.

(4 marks)

~THE END~