INTI International College Penang

FINAL
ALTERNATIVE ASSESSMENT

(COVER PAGE)

Session	:	**August 2020**
Programme	:	Diploma in Electrical & Electronic Engineering (DEEI)
Course	:	**EEE1105: Circuit Theory & Electronic Devices**
Date of Examination	:	14 December 2020 (Monday)
Time	:	8.00am – 11.00am Reading Time : Nil
Duration	:	3 Hours

Special Instructions :

This paper consists of **FOUR (4)** questions. Answer all the questions. All questions carry equal marks.

Answer script Blackboard submission requirement:

- Submit your softcopy answer script ONE time only to Blackboard.
- Write on top of each page of the answer script student Inti ID or name, subject code and page number. *Example: P20209539 / EEE1105 / Page 2 of 5.*
- Arrange your answer in proper order, scan the answer scripts and submit it to Blackboard within the given examination allocated time. Late submission is NOT allowed.
- Use a proper scanner or CamScanner on your mobile for scanning. Combine all pages in ONE PDF file for submission to Blackboard. Filename: **EEE1105 Final Exam (Name).PDF**
- Make sure pages of answer script are scanned with the good contrast and readable quality.
- Marking will be based on the scanned document as final.

Material permitted :
Non-Programmable Scientific Calculator

Materials provided :
Nil

Examiner(s)	:	**Chai Yoon Yik**
Chief Moderator	:	Steven Khoo Boo Tap

*This paper consists of **6** printed pages, including the cover page*

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE1105: CIRCUIT THEORY & ELECTRONIC DEVICES
FINAL ALTERNATIVE ASSESSMENT: AUGUST 2020 SESSION

Instructions: This paper consists of **FOUR (4)** questions. Answer all the questions. All questions carry equal marks.

Question 1 [25]

(a) A multiple sources network is shown in Figure Q1(a). Using nodal analysis, calculate the current passing through each resistor. [10]

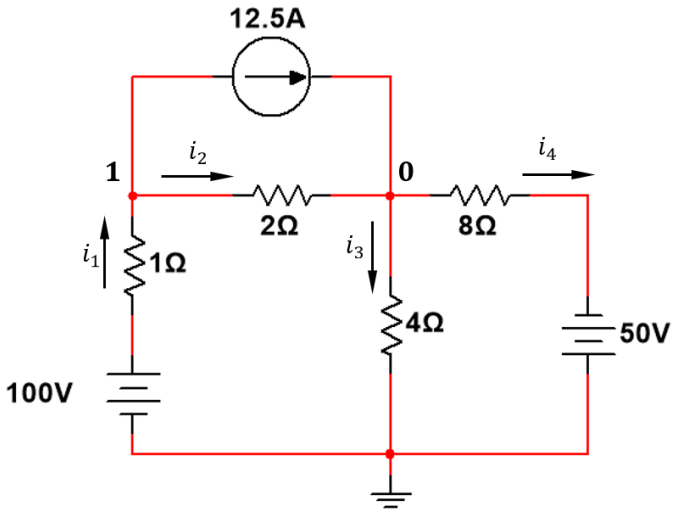


Figure Q1(a)

(b) In the circuit of Figure Q1(b), using mesh analysis, calculate i_1 , i_2 , and i_3. [9]

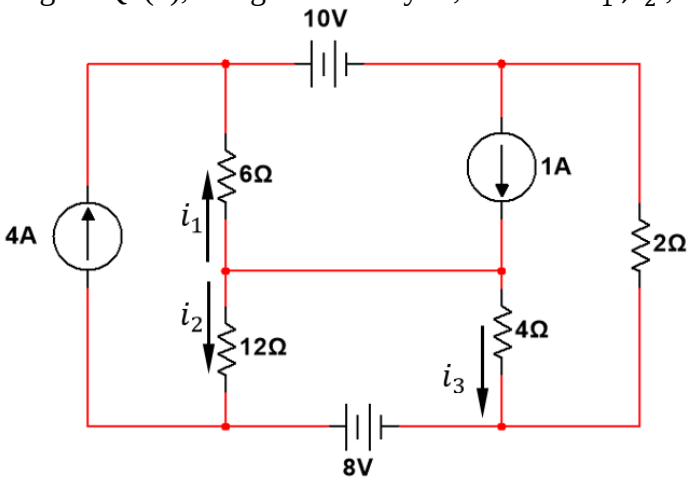


Figure Q1(b)

(c) Find the Norton equivalent (I_N, R_N) with respect to terminals a-b in the circuit as shown in Figure Q1(c). [6]

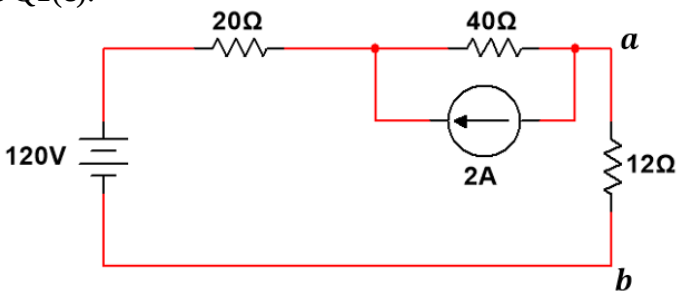


Figure Q1(c)

Question 2 [25]

(a) Figure Q2(a) shows an electrical circuit connection with sinusoidal voltage source of 50Hz.

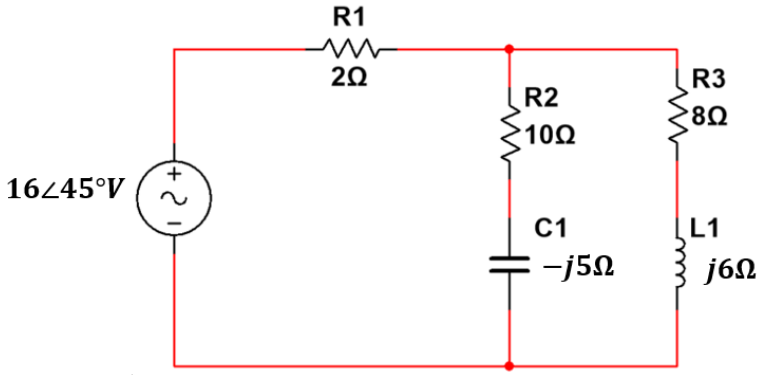


Figure Q2 (a)

Calculate:

(i) The complex power and the power factor of the circuit. [4]

(ii) The average power delivered by the source. [2]

(iii) The reactive power of the circuit. [2]

(iv) The apparent power of the circuit. [2]

(b) Suggest how to increase the power factor of the circuit to unity without affecting the total average power delivered by the source? Your solution must have relevant calculation and justification. [6]

(c) Consider the phase shifting circuit in Figure Q2(c). Let the $v_i = 120\angle 0°V$ operating at 60Hz.

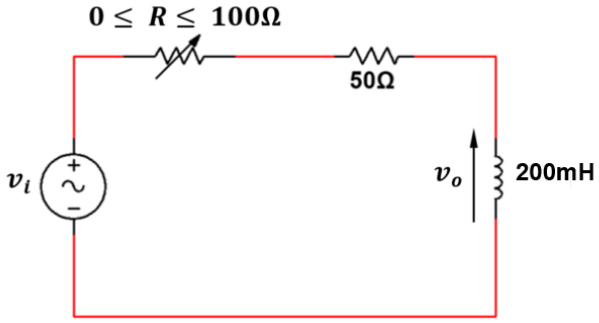


Figure Q2(c)

Calculate:

(i) The v_o when R is maximum. [3]

(ii) The v_o when R is minimum. [2]

(iii) The R that will produce a current with phase shift of 45°. [4]

Question 3 [25]

(a) Figure Q3(a) shows an electronic flash lamp which has a charging current-limiting resistor of $6k\Omega$ and a 2mF electrolytic capacitor. Assume the capacitor is charged to 240 V and the lamp resistance is 12Ω, calculate:

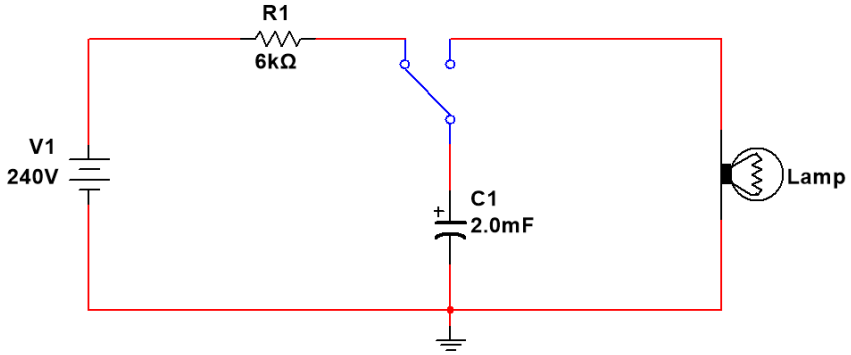


Figure Q3(a)

(i) The peak charging current. [2]

(ii) The time required for the capacitor to be fully charged. [2]

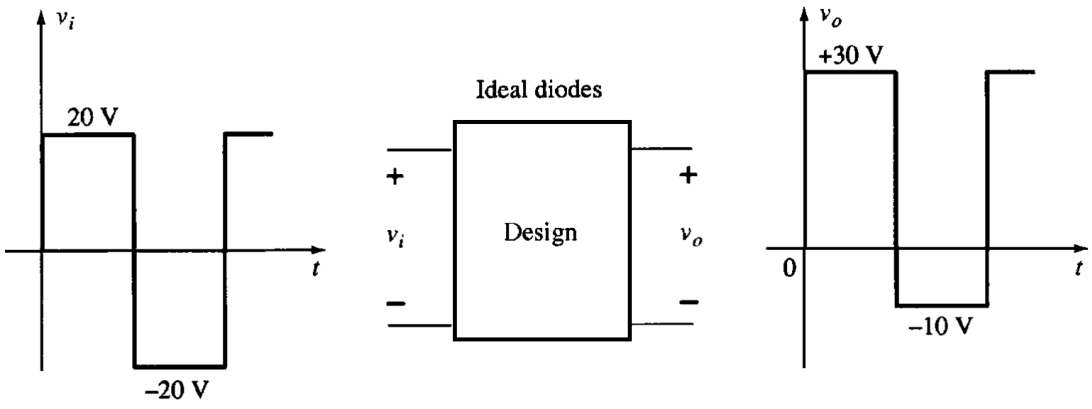
(iii) The peak discharging current. [2]

(iv) The total energy stored in the capacitor. [2]

(v) The average power dissipated by the lamp. [2]

(b) Explain why there is a 0.7V developed across a forward-bias silicon pn junction. [5]

(c) Design a diode circuit to perform the function indicated in Figure Q3(c). Assume an ideal diode. Explain the circuit operation.



[10]

Figure Q3(c)

Question 4 [25]

(a) A bipolar junction transistor is connected in emitter-bias configuration as shown in the Figure Q4(a). If the Q-point is defined at $I_{C_Q} = 4mA$ and V_{CE_Q}=10V, calculate:

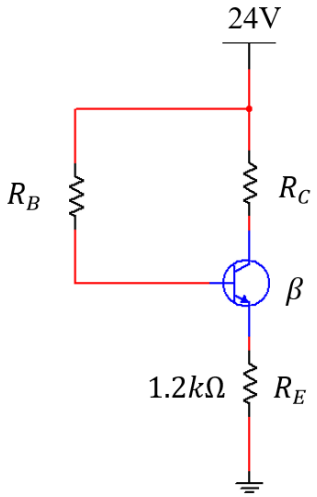


Figure Q4(a)

(i) R_C [4]

(ii) β at Q-point. [2]

(iii) R_B [2]

(iv) V_E [2]

(v) *transistor power dissipation* [2]

(b) Sketch the channel condition in an n-channel enhancement-type MOSFET structure for each of the following conditions:

- $V_{GS} = 0$
- $V_{GS} > 0$ and $V_{DS} = 0$
- $V_{GS} > 0$ and $V_{DS} > 0$

[3]

(c) Figure Q4(c) shows an n-depletion mode MOSFET circuit.

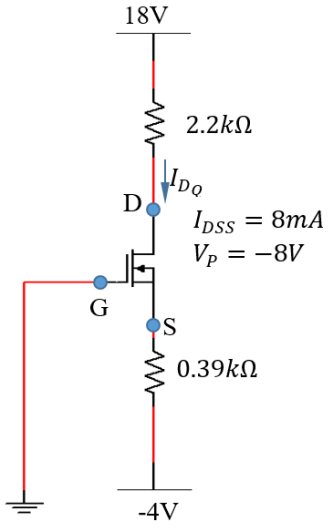


Figure Q4(c)

(i) Draw the transfer characteristics and bias line of the circuit. [4]

(ii) Determine the V_{GS_Q} and the I_{D_Q} from (i). [2]

(iii) Calculate the V_{DS_Q} and the V_S. [3]

(iv) Which region of the drain characteristic the MOSFET operates in? [1]

~THE END~