INTI
International College Penang

FINAL
Examination Paper

(COVER PAGE)

Session	:	**August 2019**
Programme	:	Diploma in Electrical and Electronic Engineering (DEEI)
Course	:	**EEE 2101: Introduction to Digital Electronics**
Date of Examination	:	9 December 2019 (Monday)
Time	:	2:00pm – 4:00pm Reading Time : Nil
Duration	:	2 Hours
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL

Materials permitted :

Non-Programmable Scientific Calculator

Materials provided :

Nil

Examiner(s) : **Mr. Steven Khoo Boo Tap**

Moderator : Dr. Ooi Beng Lee

*This paper consists of **12** printed pages, including the cover page.*

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE2101: INTRODUCTION TO DIGITAL ELECTRONICS
FINAL EXAMINATION: AUG2019 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

A combinational logic circuit is required, which accepts BCD inputs 0000 to 1001 and displays the alphanumeric '01234AbCdE', respectively, as shown below in Figure 1(a). The BCD inputs are labelled as KLMN, K is the MSB and N is the LSB. Figure 1(b) shows a Common-Anode 7 segment display. Assume all unused inputs as don't care. Show all working clearly.

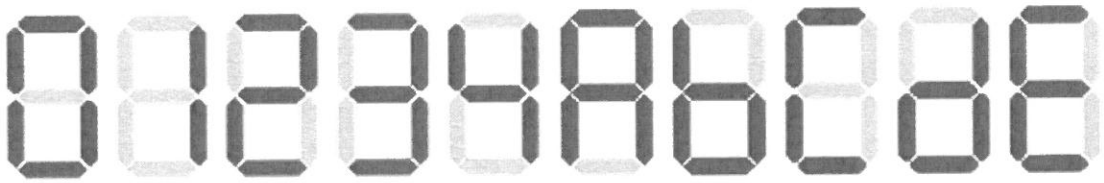

Figure 1(a)

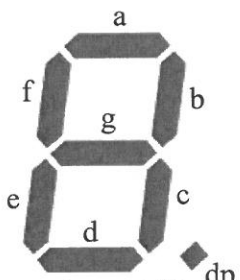

Figure 1(b)

(a) Give the complete truth table for the inputs to segments a through g of the 7 segment including the unused inputs.

(6 marks)

(b) Find the simplest form of the logic expression for segments a, e and f using Karnaugh map and/or Boolean algebra.

(9 marks)

(c) Design a (ONE) logic circuit for segment a, e and f using only 3-input NAND gates with minimum gates consideration. State the number of 7410 ICs used.

(10 marks)

Question 2

(a) Table 2(a) shows a portion of a dual negative edge-triggered D flip-flops (DM7474) datasheet. Figure 2(a) shows the logic circuit diagram of an asynchronous counter, which uses negative edge-triggered D flip-flops with labelling of $Q_AQ_BQ_CQ_D$ where Q_D is MSB and Q_A is LSB. Assume the environment is at $T_A = 25°C$ with voltage supply, $V_{CC} = 5V$.

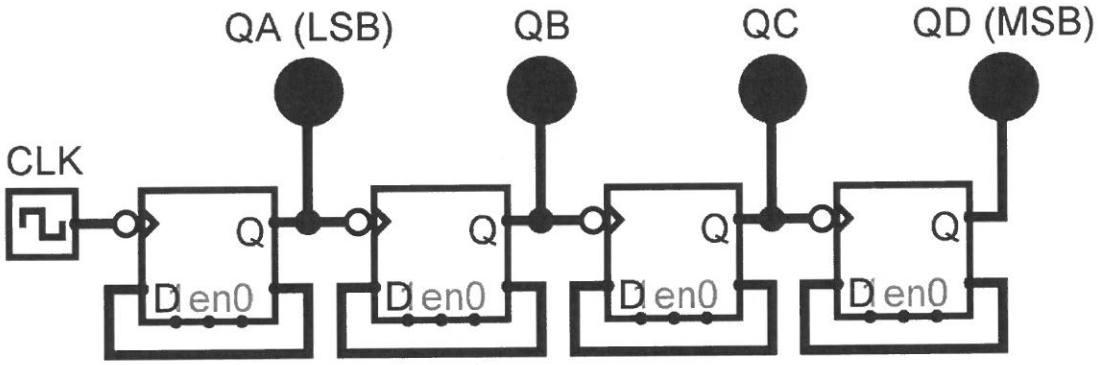

Figure 2(a)

Switching Characteristics at V_{CC} = 5V and T_A = 25°C					
Symbol	**Parameter**	**From (Input) To (Output)**	**R_L = 400Ω, C_L = 15pF**		**Units**
			Min	**Max**	
f_{MAX}	Maximum Clock Frequency		15		MHz
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Q		40	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clear to $\bar{Q}$		25	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Q or $\bar{Q}$		40	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Q or $\bar{Q}$		25	ns

Table 2(a) D flip-flop

(i) Analyse its operation to determine whether the logic circuit of Figure 2(a) is working as an up counter or down counter. Also, state the modulus and function of this counter.

(4 marks)

(ii) Determine the total propagation delay from the given datasheets in Table 2(a).

(3 marks)

(iii) Find the maximum frequency at which the counter can be operated stably.

(2 marks)

(iv) Determine the output timing diagram of Figure 2(a) with proper labelling for this counter.

(4 marks)

(b) Find the following number system transformation. Show all workings clearly.

(i) $[401.41_8 - 10001001.01_2]$ to decimal equivalent with 6 decimal points accuracy.

(4 marks)

(ii) $[36.8125_{10} \times 1011.11_2]$ to octal equivalent with 2 octal points accuracy.

(4 marks)

(iii) $[12.48_{16} - 12.5_8]$ to BCD equivalent with full BCD points accuracy.

(4 marks)

Question 3

(a) Table 3(a) shows a portion of quadruple 2-input OR gates (DM54LS32) datasheet. Find the following parameters from this datasheet, show all working clearly:

(i) Fan-out, a gate can safely drive. Assume that the gate is driving the same family type of logic gate, DM54LS32 inputs.

(3 marks)

(ii) Average Power dissipation, $P_{D\,(avg)}$ for one gate on a DM54LS32 IC.

(3 marks)

(iii) Noise Margin voltages, V_{NL} and V_{NH}.

(3 marks)

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V	DM54LS and 54LS	−55°C to +125°C
Input Voltage	7V	DM74LS	0°C to +70°C
Operating Free Air Temperature Range		Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS32			DM74LS32			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			3.1	6.2	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			4.9	9.8	mA

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	11	4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	11	4	15	ns

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Table 3(a)

(b) Find the Boolean expression of F in Figure 3(b) and present the expression to the minimum using Boolean simplification only. Use only ONE IC (Integrated Circuit) of your choice to represent the simplified expression. Show working clearly.

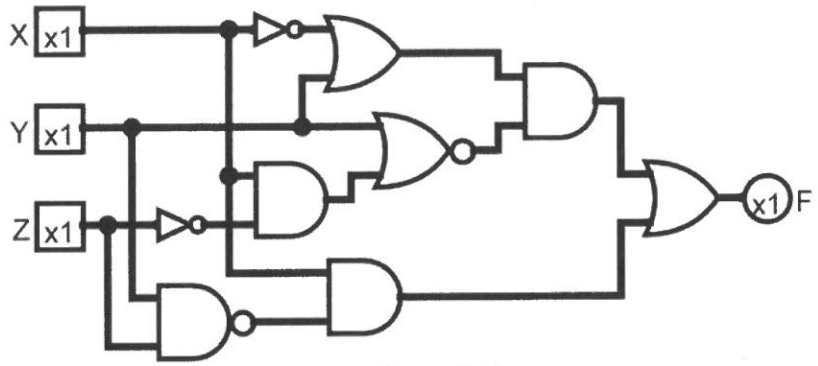

Figure 3(b)

(8 marks)

(c) Figure 3(c) shows the pin diagram and logic symbol of 74LS283 4-bit adder with (pin numbers in parentheses). Explain and show how two 74LS283 adders can be connected to form an 8-bit parallel adder. Include the calculation of the 8-bit parallel adder for the following 8-bit input numbers:
$A_8A_7A_6A_5A_4A_3A_2A_1 = 10111001$ and $B_8B_7B_6B_5B_4B_3B_2B_1 = 10011110$.

Show the adders with proper interconnections labelling. Indicate the Low-order adder and High-order adder in details. Label the sum output as $\Sigma_8\Sigma_7\Sigma_6\Sigma_5\Sigma_4\Sigma_3\Sigma_2\Sigma_1$ and the carry output as Σ_9.

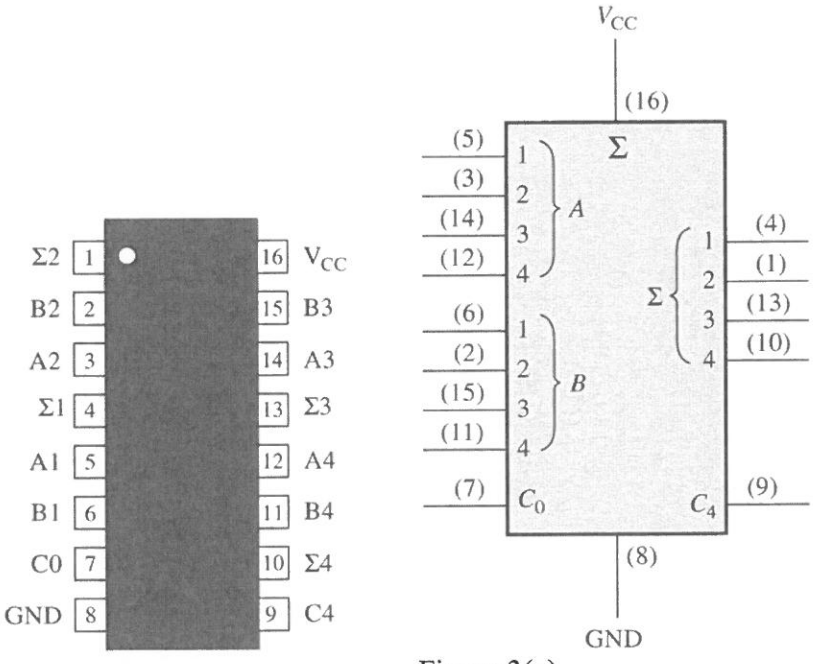

Figure 3(c)

(8 marks)

Question 4

(a) For the given truth tables in Table 4a(i) and excitation tables in Table 4a(ii),

(i) design a D flip-flop function using JK flip-flop. The design can be added with additional gates in order to fulfil the conversion. Show all working clearly for JK-to-D converter.

(5 marks)

(ii) design a T flip-flop function using SR flip-flop. The design can be added with additional gates in order to fulfil the conversion. Show all working clearly for T-to-SR converter.

(5 marks)

Table 4a(i) Flip-flop Truth Tables

Inputs		Outputs	
S	R	Q_n	Q_{n+1}
0	0	No Change	
0	1	Reset	
1	0	Set	
1	1	Invalid	

Inputs		Outputs	
J	K	Q_n	Q_{n+1}
0	0	No Change	
0	1	Reset	
1	0	Set	
1	1	Toggle	

Input	Outputs	
D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Input	Outputs	
T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Q_n: Present State
Q_{n+1}: Next State

Table 4a(ii) Flip-flop Excitation Tables

Outputs		Inputs	
Q_n	Q_{n+1}	S	R
0	0	0	×
0	1	1	0
1	0	0	1
1	1	×	0

Outputs		Inputs	
Q_n	Q_{n+1}	J	K
0	0	0	×
0	1	1	×
1	0	×	1
1	1	×	0

Outputs		Input
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Outputs		Input
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Q_n: Present State
Q_{n+1}: Next State

(b) In computer system, it is often necessary to choose data from exactly one of a number of sources. The circuit has an output (F) that is exactly the same as one of two data inputs (X, Y) based on the value of a control input (S). If $S = 0$, then output $F = X$. If $S = 1$, then output $F = Y$. Assume S is the MSB and Y is the LSB. Show all workings clearly.

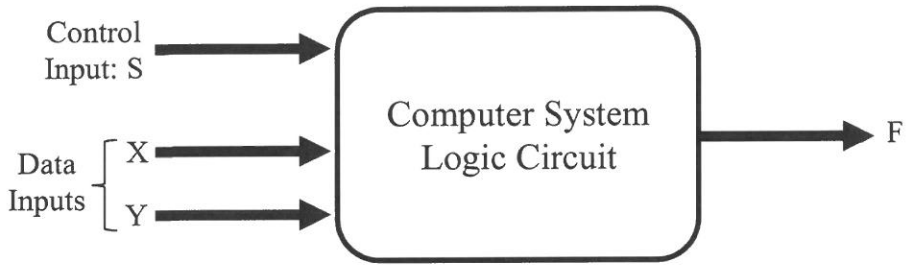

Figure 4(b)

(i) Give the complete truth table of the computer system.

(3 marks)

(ii) Give the simplest expression for the computer system using Karnaugh Map.

(3 marks)

(iii) Design the logic circuit for the computer system using only ONE IC (Integrated Circuit) of your choice to represent the simplified expression.

(3 marks)

(iv) Design the logic circuit for the computer system using a 2-to-1 Multiplexer with X as the select line and logic gates (if required).

(3 marks)

(v) Build the expression obtained in Question 4(b)(ii) using only 3-to-8 Decoder and logic gates (if required).

(3 marks)

Question 5

(a) Table 5(a) shows the current ratings of TTL series logic gates. A 74S08 AND gate output is driving a few other TTL outputs as shown in Figure 5(a). Determine if there is a loading problem.

(4 marks)

TTL Series	Output Drive		Input Loading	
	I_{OH}	I_{OL}	I_{IH}	I_{IL}
74	400μA	16mA	40μA	1.6mA
74S	1.0mA	20mA	50μA	2.0mA
74LS	400μA	8mA	20μA	400μA
74AS	2.0mA	20mA	200μA	2.0mA
74ALS	400μA	8mA	20μA	100μA
74F	1.0mA	20mA	20μA	600μA

Table 5(a)

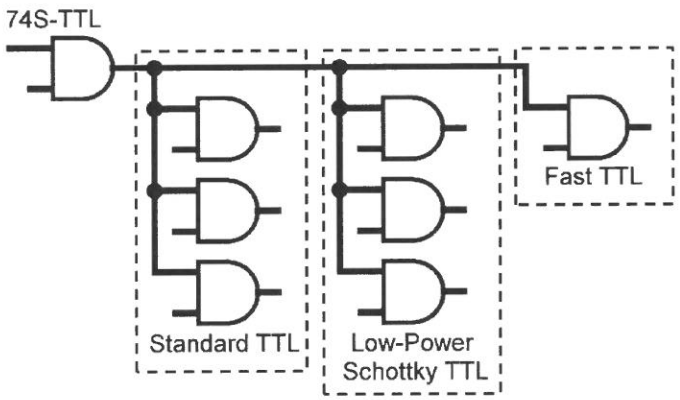

Figure 5(a)

The 74S08 AND gate output needs to be used to drive some 74S inputs in addition to the load inputs. Determine how many additional 74S inputs could the output drive without being overloaded?

(3 marks)

(b) Express the following Boolean expression using Karnaugh Map and Boolean expression to the most simplified form:

(i) $F_1(R,S,T,U) = \prod M(0,1,2,4,5,6,11,13) \cdot \prod D(8,9,10)$ to the simplest POS form.

(4 marks)

(ii) $F_2(W,X,Y,Z) = \sum m(2,7,8,13) + d(1,4,11,14)$ to the simplest form.

(4 marks)

(c) Design a synchronous 3-bit up/down counter using positive edge-triggered T flip-flop for MSB, SR flip-flop for second bit and JK flip-flop for LSB. Assume T_2 is the MSB input, S_1 & R_1 are the next flip-flop inputs and J_0 & K_0 are the LSB inputs. Assume all unused states as don't care.

Input S will be used as the up/down control. The counter will count from 0 ⇨ 1 ⇨ 2 ⇨ 4 ⇨ 6 ⇨ 7 ⇨ 0 when input, S = 1 and 7 ⇨ 6 ⇨ 4 ⇨ 2 ⇨ 1 ⇨ 0 ⇨ 7 when input, S = 0 as shown below in Figure 5(c).

Use $Q_2Q_1Q_0$ outputs labelling for T_2, S_1 & R_1 and J_0 & K_0 inputs. Provide proper labelling for the designed logic circuit. Show all workings clearly.

(i) Construct the transition table/next state table for the up/down counter.

(5 marks)

(ii) Design the simplified Boolean expressions for T_2, S_1, R_1, J_0 and K_0 inputs using Karnaugh map and Boolean algebra to the simplest form.

(5 marks)

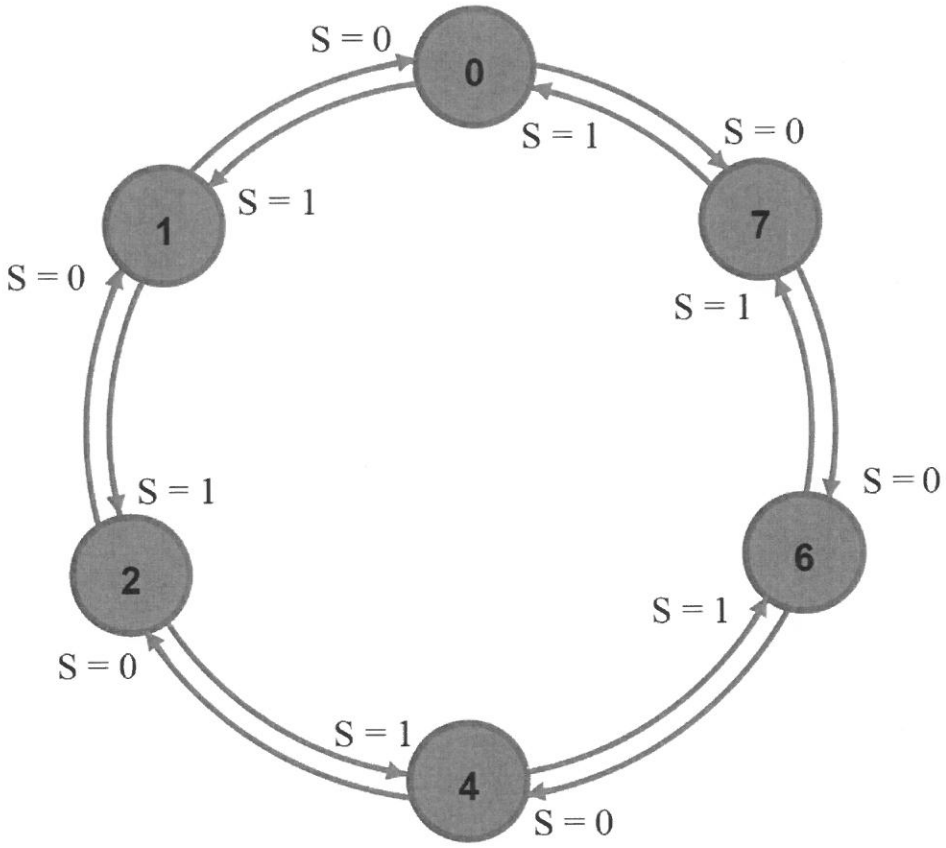

Figure 5(c)

Question 6

(a) For the pulse shown in Figure 6(a) below, determine the Rise time, Fall time, Pulse time and Amplitude from the graph as accurate as possible.

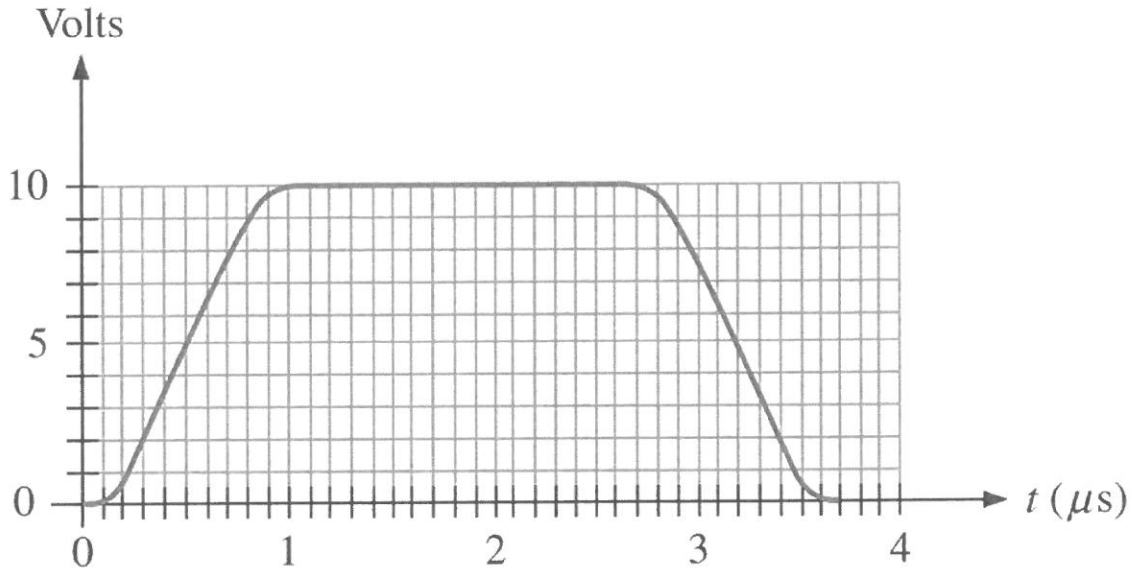

Figure 6(a)

(4 marks)

(b) Figure 6(b) shows a computer controlling the speed of a motor. The 0 to 2mA analog current from the DAC is amplified to produce motor speeds from 0 to 1000 rpm (revolutions per minute). Assuming a 12-bit DAC with perfect accuracy, explain how close to 250 rpm can the motor speed be adjusted for the motorized system in Figure 6(b)?

(9 marks)

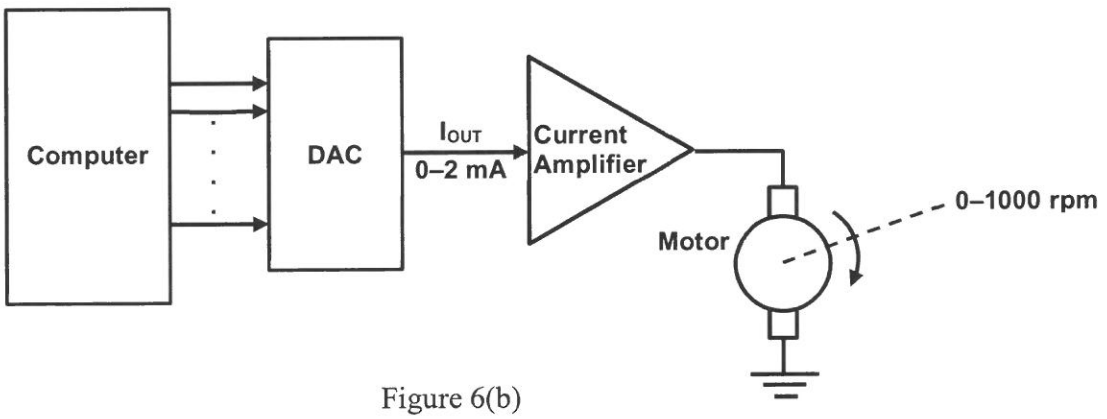

Figure 6(b)

(c) An 8-bit digital ramp ADC with a 40 mV resolution uses a clock frequency of 2.5 MHz. Assume the number of steps is using $2^n - 1$. Determine the following values:-

(i) the digital output for an analog voltage of 6.019 V.

(3 marks)

(ii) the digital output for an analog voltage of 6.040 V.

(2 marks)

(iii) the maximum and average conversion times.

(4 marks)

If the digital outputs of part (i) and part (ii) are the same, justify your answer. Otherwise, explain why they are different.

(3 marks)

– THE END –

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