



INTI International College Penang

FINAL
Examination Paper

(COVER PAGE)

Session : August 2019

Programmes : Diploma in Electrical and Electronic Engineering (DEEI)

Course : EEE1106: ANALOGUE ELECTRONICS

Date of Examination : 11 December 2019 (Wednesday)

Time : 2:00pm – 4:00pm

Duration : 2 Hours Reading Time Nil

Special Instructions :

This paper consists of SIX (6) questions. Answer any FOUR (4) questions in the answer scripts provided. All questions carry equal marks.

IMPORTANT NOTE : THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL BY THE STUDENTS.

Materials Permitted :
Non-programmable Calculator (e.g. Model fx570 Series)

Materials Provided :
Worksheet for Q2(c)

Examiner(s) : Chan Tse Wei

Moderator : Prof. Ir. Dr. Mandeep Singh

This paper consists of 13 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)

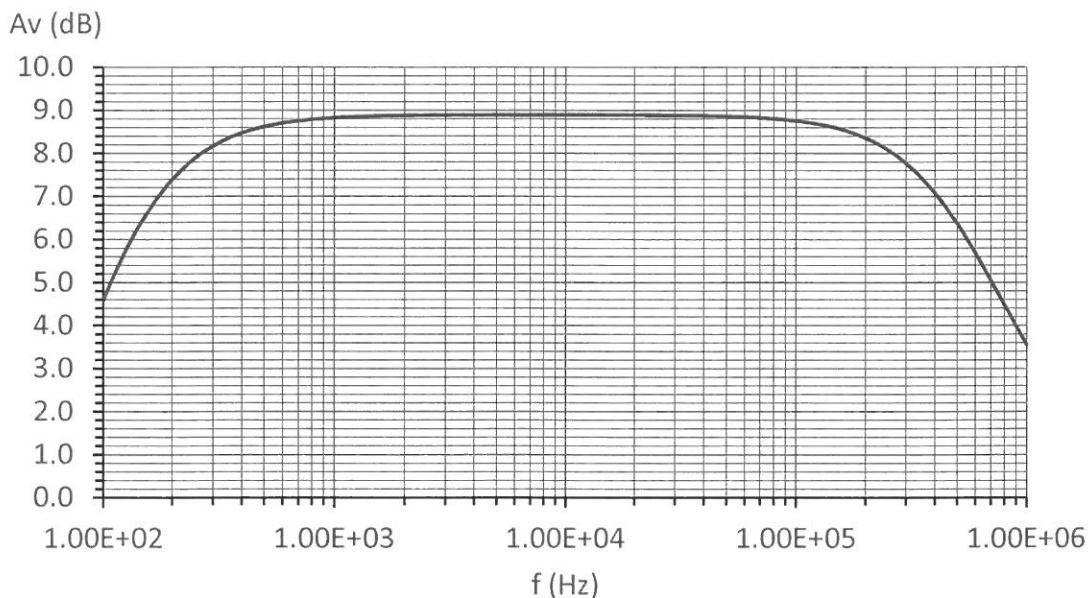
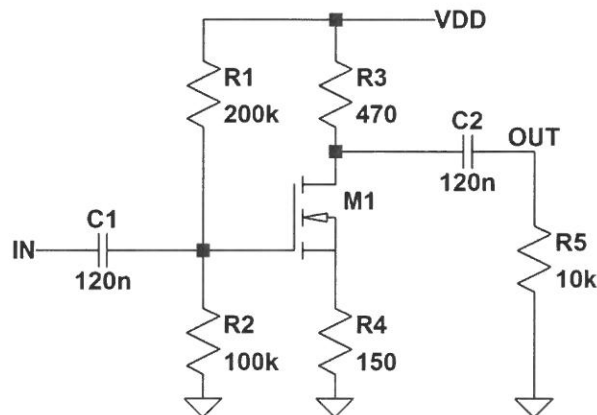
EEE1106: ANALOGUE ELECTRONICS

FINAL EXAMINATIONS: AUGUST 2019 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks. The marks allocated to each sub-question are shown in square brackets at the right-hand margin. Present your answers neatly and clearly. The assessor reserves the rights to ignore your answers if they are ambiguous.

Question 1

- a. Figure-Q1(a) shows a single stage FET amplifier and its voltage gain frequency response.

**Figure-Q1(a)**

- i. Explain the state of the circuit, in terms of the behavior of the capacitors, which exhibits maximum voltage gain (approximately 8.9 dB in this case) at the mid-band frequency spectrum.

[1]

- ii. Explain the root cause of the gain reduction at the low frequency spectrum. [2]
- iii. Explain the root cause of the gain reduction at the high frequency spectrum. [2]

b. Figure-Q1(b) shows the voltage gain frequency response of an amplifier.

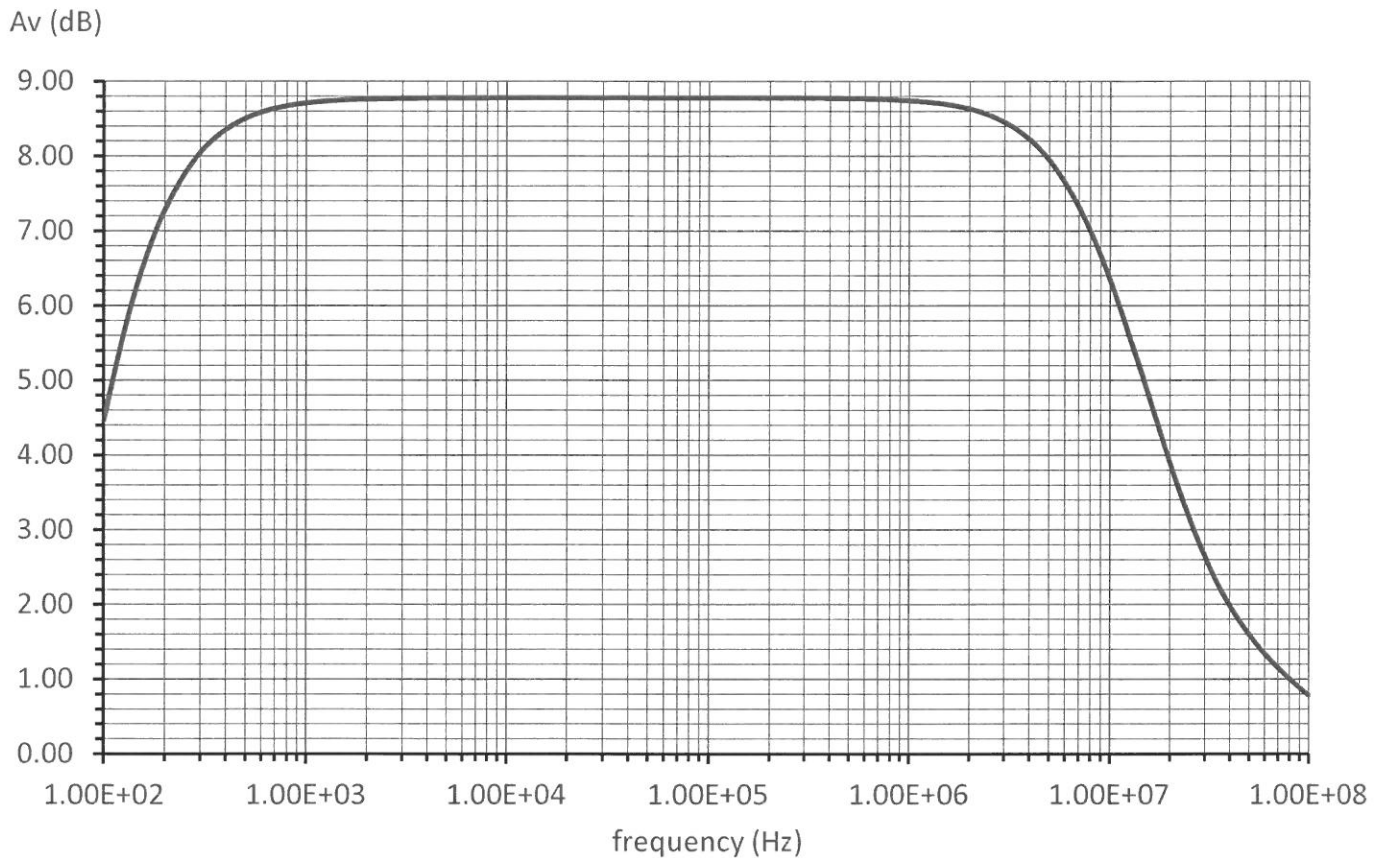


Figure-Q1(b)

- i. Calculate the maximum output voltage of the amplifier in volts if the input voltage is a sinusoidal signal having a peak value of 2.0 V at 20 kHz. [5]
- ii. Estimate the bandwidth of the amplifier. [5]

c. Figure-Q1(c) shows the AC equivalent circuit model of an FET voltage amplifier.

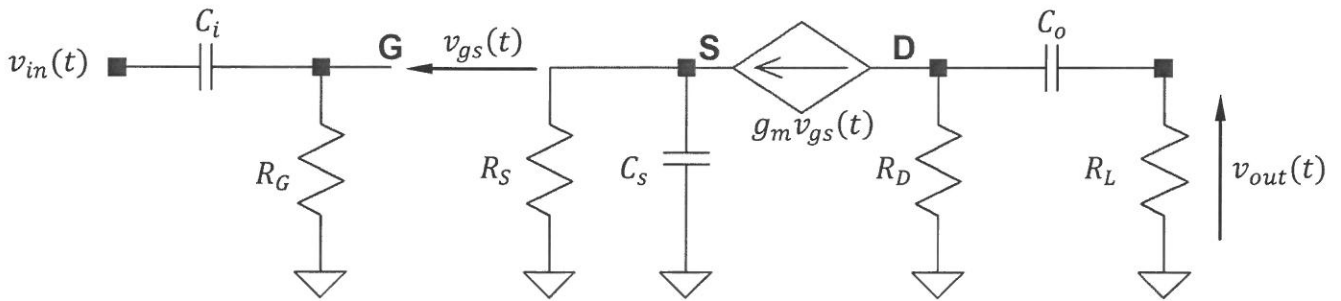


Figure-Q1(c)

- i. Draw an AC equivalent circuit model for the amplifier to evaluate the cutoff frequency contributed by capacitor C_S . [3]
- ii. Utilizing the AC equivalent circuit model obtained in part (c)(i), show that the voltage transfer function of $V_S(s)/V_G(s)$ can be expressed in the form of,

$$\frac{V_S(s)}{V_G(s)} = \frac{a_0}{s + \omega_o}$$

and state a_0 and ω_o in terms of the relevant passive components and transistor parameter, g_m . [5]

- iii. Determine the cutoff frequency expression of the amplifier which is contributed by capacitor C_S . [2]

Question 2

- a. Clearly explain the difference between class-A and class-B power amplifiers in terms of their respective transistor conduction and power conversion efficiency. [5]
- b. Figure-Q2(b)(i) shows a basic class-B power amplifier circuit, and Figure-Q2(b)(ii) shows the power amplifier's input and output voltage timing diagrams.

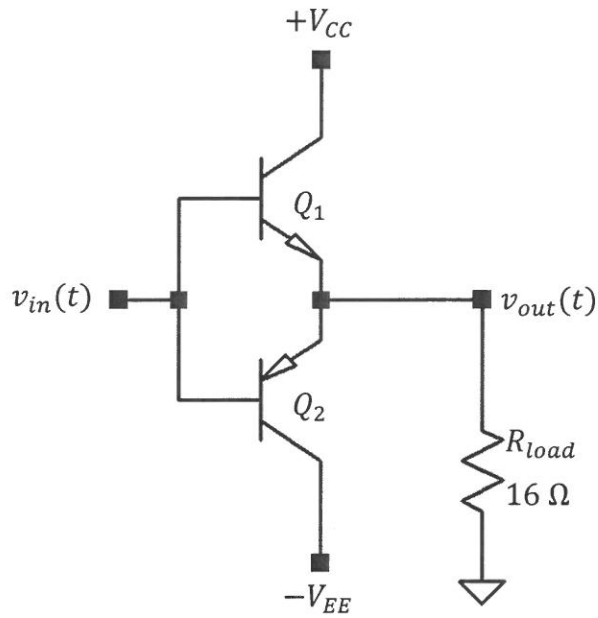


Figure-Q2(b)(i)

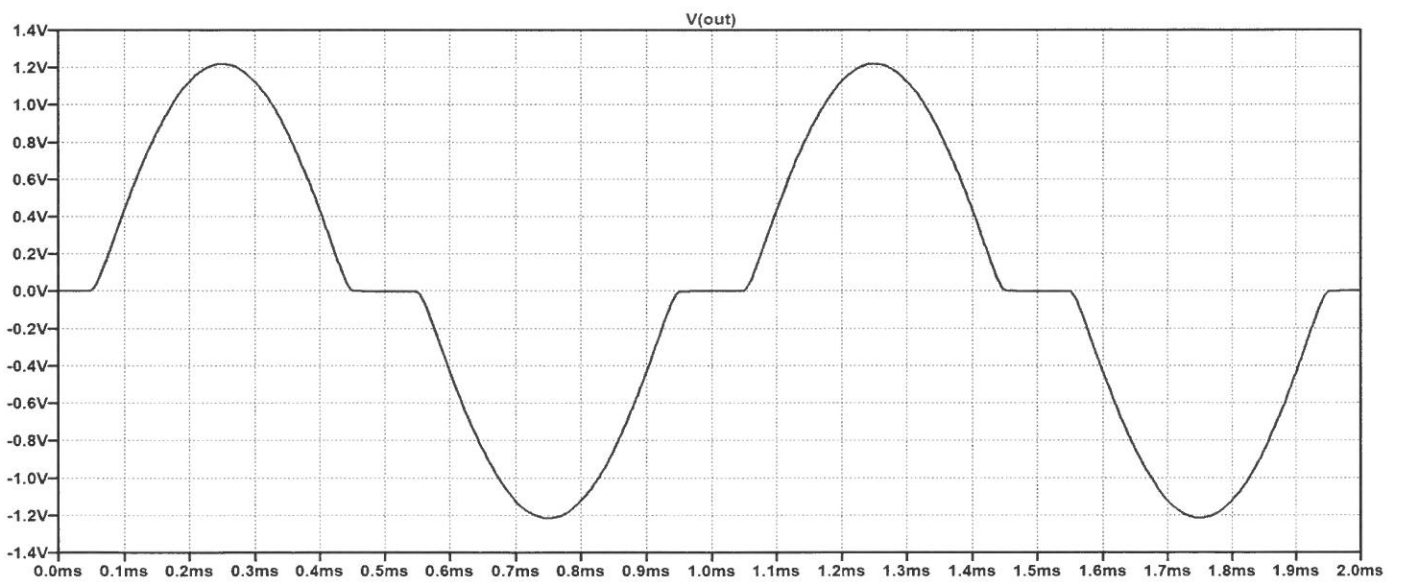
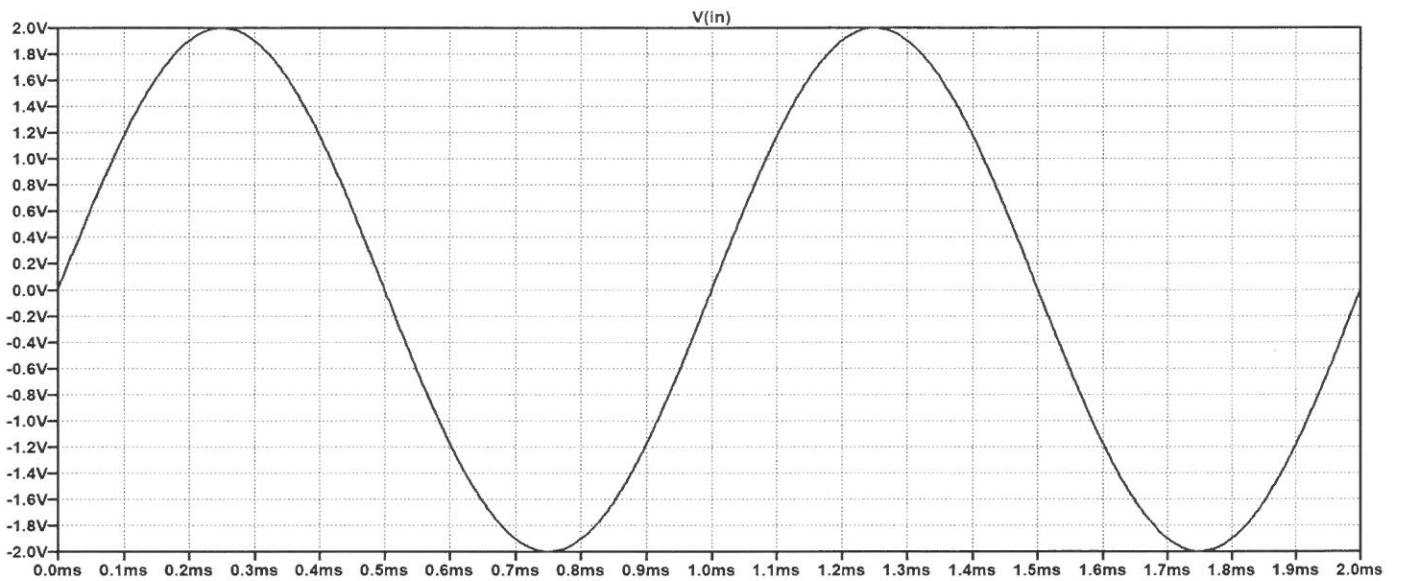


Figure-Q2(b)(ii)

- i. State the type of distortion exhibited by the power amplifier. [1]
 - ii. Based on the given timing diagrams in Figure-Q2(b)(ii), sketch the voltage transfer curve (VTC) of the power amplifier. [5]
 - iii. Determine the minimum collector current rating suitable for the two transistors used in the power amplifier. [2]
 - iv. Determine the minimum power rating suitable for the load resistor terminating the power amplifier output. [2]
- c. Figure-Q2(c) shows a power amplifier circuit that resolved the problem exists in the power amplifier shown in Figure-Q2(b)(i). Diodes D_1 and D_2 matches the characteristic of the respective BE-junction voltages (which are obtainable from part (b)).

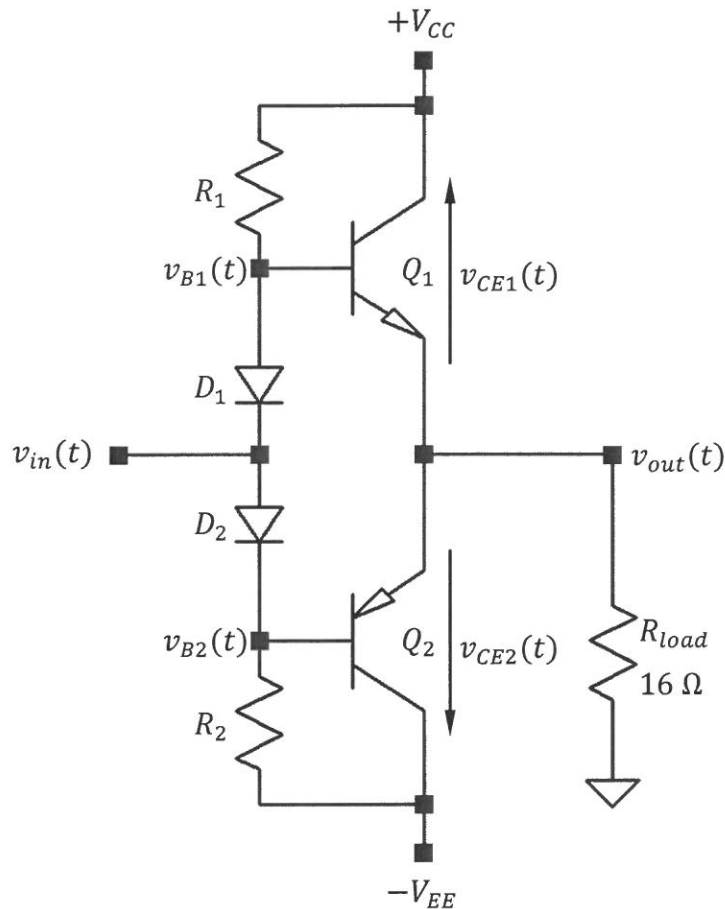


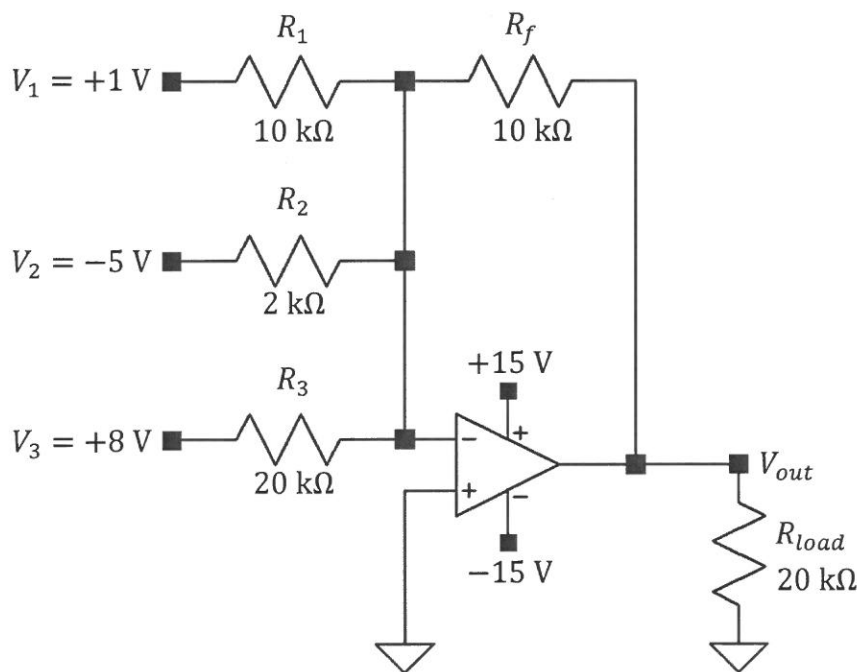
Figure-Q2(c)

The timing diagram of $v_{in}(t)$ is shown in “**WORKSHEET FOR Q2(c)**”. Complete the worksheet by sketching the respective timing diagrams of the node voltages listed in the worksheet. Each of the timing diagram carries equal marks.

[10]

Question 3

- a. i. Draw the schematic diagram of a non-inverting amplifier utilizing a single op-amp, operating in dual supply mode. [2]
- ii. State the voltage transfer function expression of the amplifier given in part (a)(i). [1]
- iii. Explain the reason for naming the circuit as "non-inverting amplifier". [2]
- b. Figure-Q3(b) shows an inverting summing amplifier. The op-amp used is assumed ideal.

**Figure-Q3(b)**

- i. Calculate the value of the output voltage V_{out} . [5]
- ii. Calculate the maximum current drawn from the op-amp. [5]
- c. Figure-Q3(c) shows an inverting Schmitt Triggered Comparator. The op-amp used is assumed ideal. The input voltage, V_{in} , is taken from a sensor output which varies between 0 V and 5 V levels. V_{ref} is a reference voltage targeted to concurrently adjust the upper and lower threshold values of the comparator.
- Identify the range of V_{ref} such that the comparator maintain a valid hysteresis characteristic. Show your analysis clearly. [10]

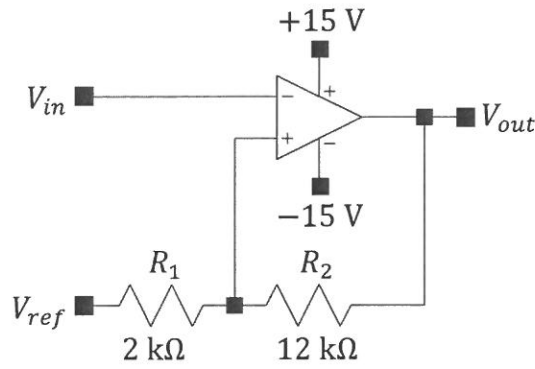


Figure-Q3(c)

Question 4

a. Clearly differentiate the frequency response between an ideal analogue filter and a practical one in general. [5]

b. The voltage transfer function of a filter circuit is given as,

$$T(s) = \frac{a_2 s^2}{s^2 + b_1 s + b_0}$$

i. Identify the type of filter that has the given transfer function. [3]

ii. Identify the maximum magnitude of the voltage transfer function at the pass band frequency range. [3]

iii. Draw the schematic diagram of a passive filter that has the similar voltage transfer function and state the value of a_2 for the passive filter drawn. [4]

c. Figure-Q4(c) shows an example of an analogue filter.

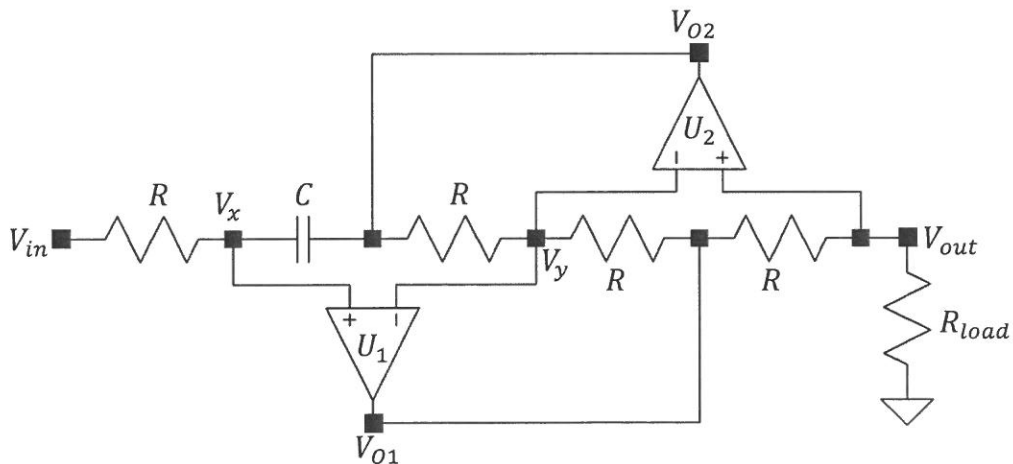


Figure-Q4(c)

- i. Assuming that op-amps U_1 and U_2 are operating linearly, determine the relationship between V_x , V_y and V_{out} . [3]
- ii. Derive the voltage transfer function expression of the filter, $V_{out}(s)/V_{in}(s)$. [5]
- iii. Determine the type of filter that is implemented by the circuit based on the voltage transfer function obtained in part (c)(ii). [2]

Question 5

- a. Explain,
 - i. the function of a harmonic oscillator. [2]
 - ii. the oscillation criteria of an RC feedback harmonic oscillator. [3]

- b. Figure-Q5(b)(i) shows the schematic diagram of a Wien Bridge oscillator. R_T is a thermistor in which its resistance reduces when its body resistance increases.

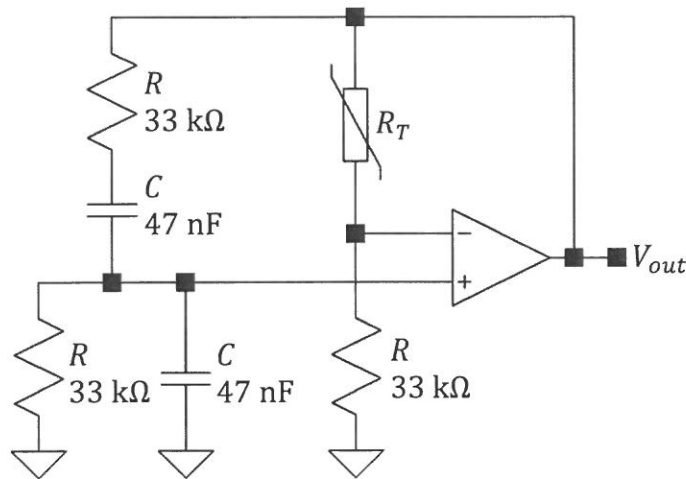


Figure-Q5(b)(i)

- i. Calculate the expected frequency of V_{out} . [3]
- ii. To initiate oscillation, R_T needs to be at least 10% higher than its resistance value that sustain output oscillation, calculate the minimum value of R_T to initiate oscillation. [3]
- iii. If the implemented thermistor, R_T has a characteristic as shown in Figure-Q5(b)(ii), estimate the expected RMS value of output voltage, V_{out} . [4]

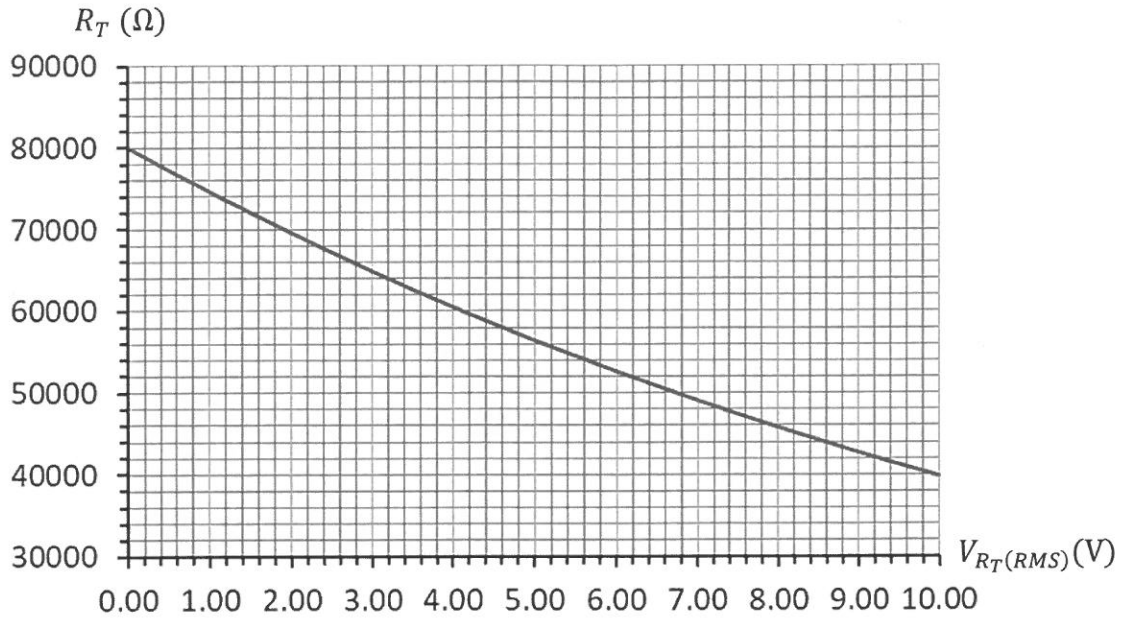


Figure-Q5(b)(ii)

- c. Figure-Q5(c) shows the schematic diagram of a Sallen-Key low pass filter modified to implement a harmonic oscillator. The modification involved grounding its input terminal and replacing one of its amplifier's feedback resistor with a thermistor identical to the one shown in part (b).

Determine the expression of R_T in terms of the passive components in the circuit to sustain output oscillation. Show all workings clearly. [10]

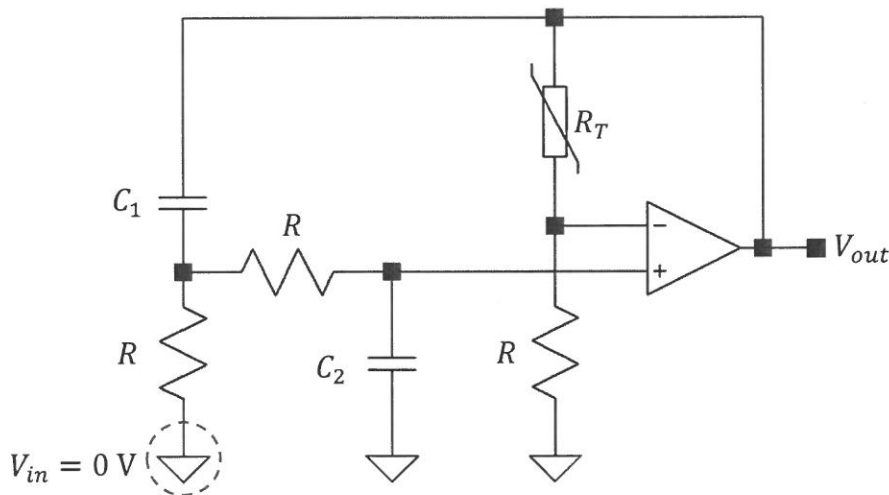


Figure-Q5(c)

Question 6

- a. An op-amp based non-inverting amplifier has a voltage gain of 20. The op-amp chosen for the amplifier has a slew rate of $13 \text{ V}/\mu\text{s}$. If an input voltage of $v_{in}(t) = \sin(5000t)$ is applied to the amplifier, determine if the amplifier's output is distorted. [5]
- b. Figure-Q6(b)(i) shows a Schmitt Trigger Comparator while Figure-Q6(b)(ii) shows its input and output voltage timing diagrams.
- i. Based on the timing diagrams in Figure-Q6(b)(ii), sketch the voltage transfer curve (VTC) of the comparator with clear labelling of relevant voltage values [4]
- ii. Calculate the resistance value for R_2 . [6]

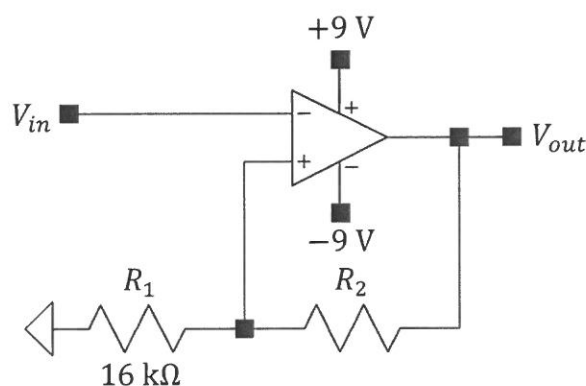


Figure-Q6(b)(i)

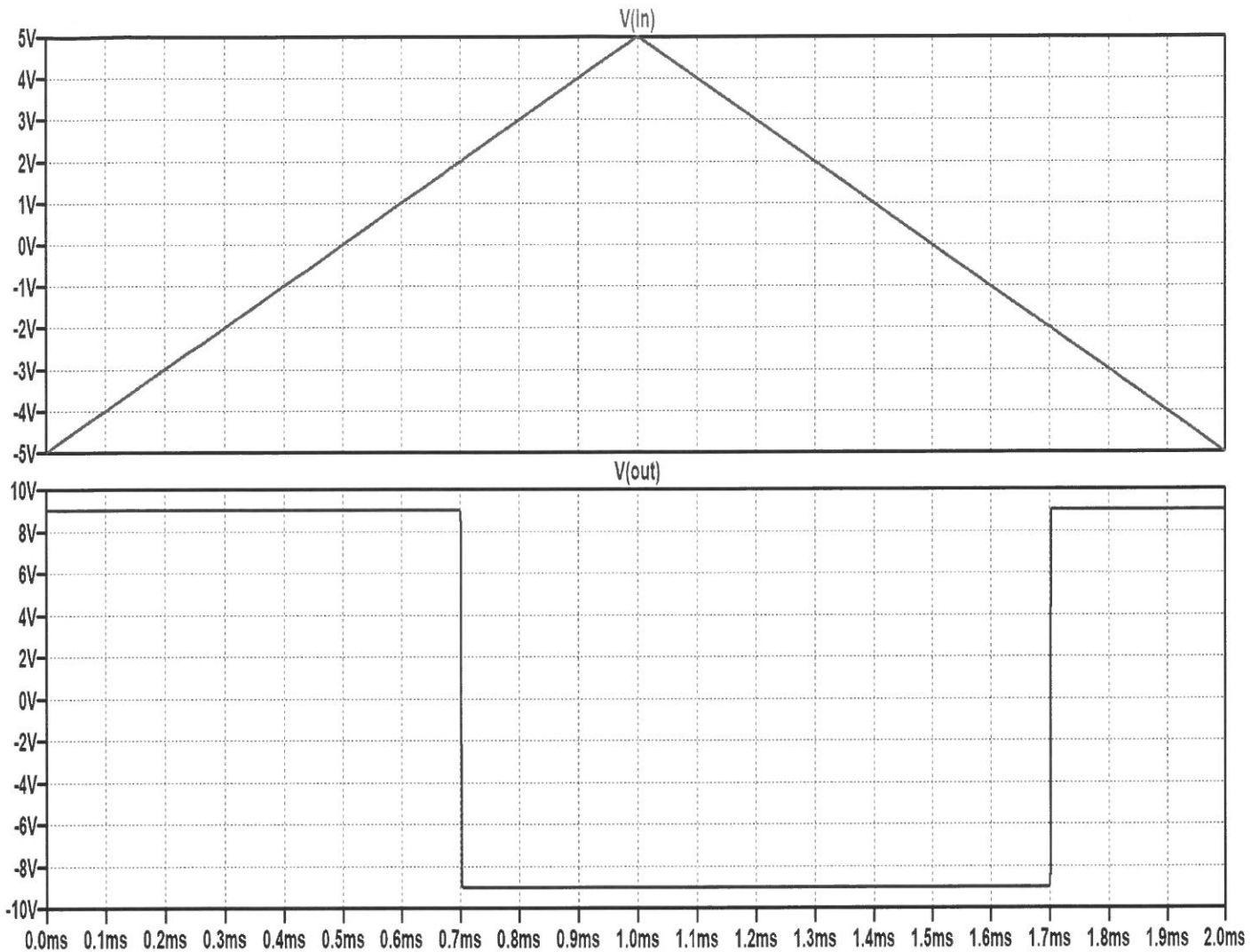


Figure-Q6(b)(ii)

- c. Figure-Q6(c) shows a common source amplifier. Capacitor C_i is the amplifier's input coupling capacitor which has sufficiently low impedance at mid-band operation. The transconductance (g_m) of transistor Q_1 is 2 mS. The load capacitance, C_{load} is sufficiently large that the parasitic capacitances of transistor Q_1 and the wiring capacitance of the circuit can be ignored.

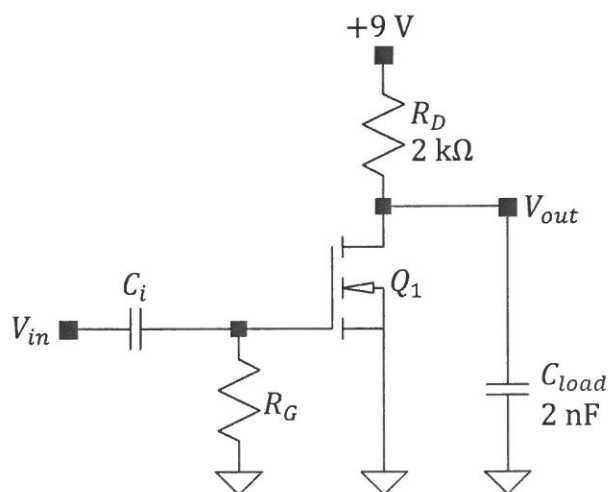


Figure-Q6(c)

- i. Sketch the AC equivalent circuit model for the amplifier at high frequency operation. [4]
- ii. Analyze the voltage gain of the amplifier at 200 kHz frequency operation, which is the high frequency spectrum operation for the amplifier. Express the voltage gain in polar form. [6]

~ The End ~

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