INTI International College Penang

FINAL
Examination Paper

(COVER PAGE)

Session	:	**August 2019**
Programme	:	Diploma in Electrical and Electronic Engineering (DEEI)
Course	:	**EEE1105: Circuit Theory and Electronic Devices**
Date of Examination	:	9 December 2019 (Monday)
Time	:	2:00pm – 4:00pm Reading Time : Nil
Duration	:	2 Hours
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL

Materials permitted :

Non-Programmable Scientific Calculator

Materials provided :

Appendix A (on page 8)

Examiner(s)	:	**Mr. Chai Yoon Yik**
Moderator	:	Prof. Ir. Dr. Mandeep Singh

*This paper consists of **9** printed pages, including the cover page.*

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE1105: CIRCUIT THEORY AND ELECTRONIC DEVICES
FINAL EXAMINATION: AUGUST 2019 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

(a) For the network shown in Figure Q1(a), calculate:

(i) The total resistance, R_T of the circuit. [3]
(ii) The I_2, I_6, I_S, and V_5. [8]
(iii) The I_S again when there is a short circuit across R1. [1]

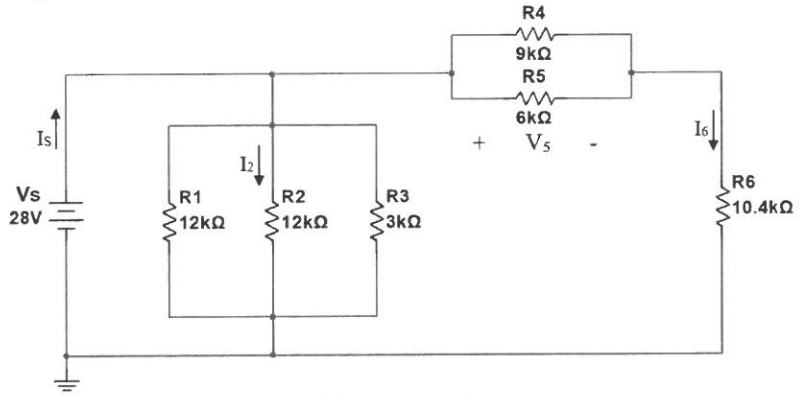


Figure Q1(a)

(b) A DC network is shown in Figure Q1(b). Calculate the value of the nodal voltage V_1, V_2 and V_3 using Nodal analysis. [9]

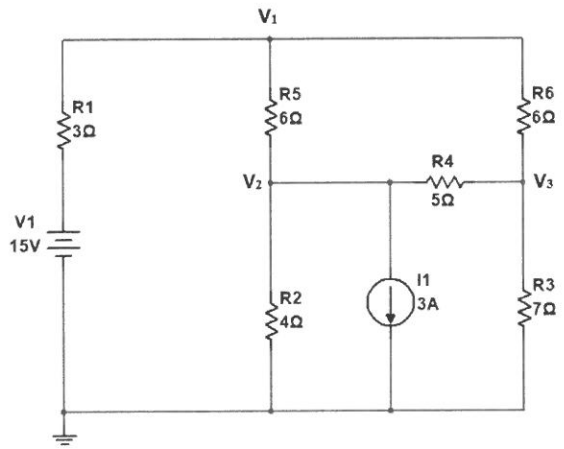


Figure Q1(b)

(c) Determine the potential difference V_1 in the Figure Q1(c). [4]

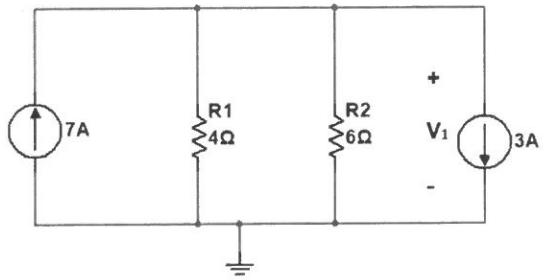


Figure Q1(c)

Question 2

(a) A 230 V, 50 Hz AC power supply is connected to an inductive load with resistance of 8Ω and inductance of 0.05 H. Determine the:

(i) Impedance of the load in polar form. [2]
(ii) Magnitude and phase angle of the load current. [2]
(iii) Apparent power and power factor. [4]
(iv) Real power supplied to the load. [2]
(v) Reactive power supplied to the load. [2]

(b) A capacitor is connected in parallel to the load in (a) to increase the power factor to unity. Determine:

(i) The required capacitance value. [4]
(ii) The change in supply current from the uncorrected to the corrected power factor system. [2]

(c) Explain the phenomenon of a series R-L-C resonant circuit using a frequency response plot. Why Q factor is very important parameter in an resonant circuit? [7]

Question 3

(a) Determine the current I flows through R1 resistor in. [6]

Figure Q3(a)

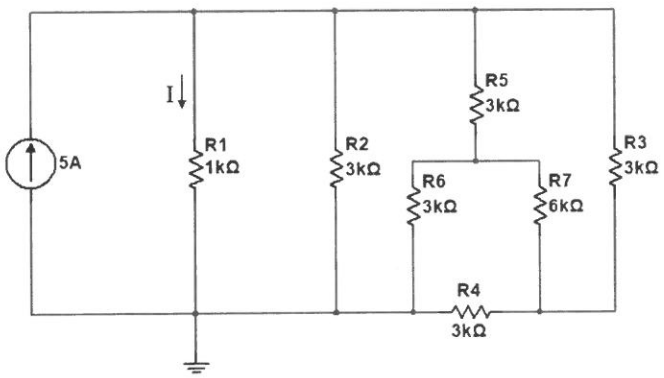


Figure Q3(a)

(b) Given a network in Figure Q3(b), using the superposition principle, find:

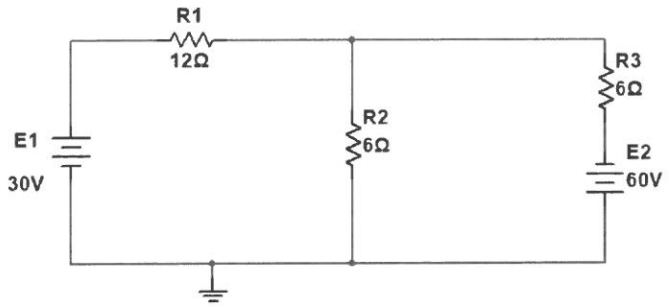


Figure Q3(b)

(i) The current through each resistor. [8]

(ii) The power dissipated in R1. [2]

(c) Determine the Thévenin equivalent circuit for the network external to the resistor RL in Figure Q3(c). [9]

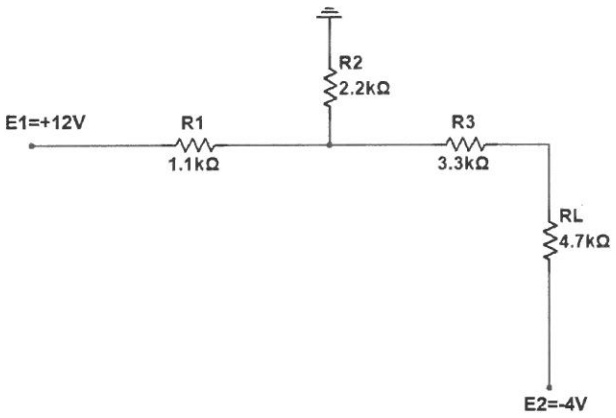


Figure Q3(c)

Question 4

(a) Briefly describe the following terms:

(i) n-type silicon [1]

(ii) p-type silicon [1]

(iii) Donor impurity [1]

(iv) Acceptor impurity [1]

(v) Majority carrier [1]

(vi) Minority carrier [1]

(b) Describe in your own words the conditions established by forward- and reverse-bias conditions in a p–n junction diode and how the resulting current is affected. [6]

(c) Draw the V_o signal for the diode circuit with V_i as shown in the Figure Q4(c). All the important details must be indicated in the drawing. Appropriate calculation illustration also required in your answer. [8]

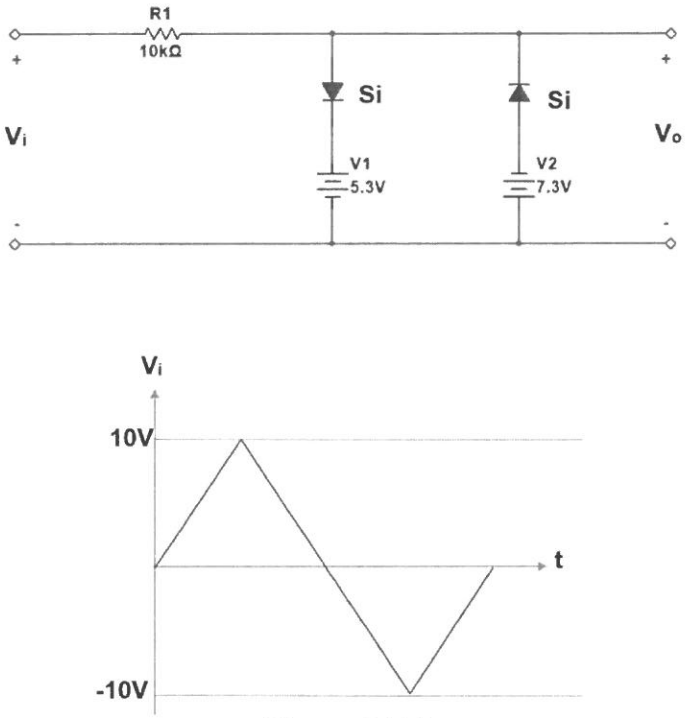
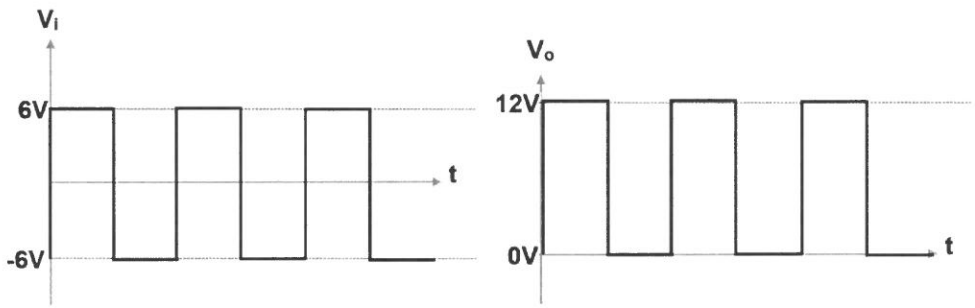


Figure Q4(c)

(d) How do you transform the V_i into V_o signal as shown in Figure Q4(d) using a diode circuit?



[5]

Figure Q4(d)

Question 5

(a) A BJT transistor 2N2222A is used in a signal amplifier circuit as shown in the Figure Q5(a).

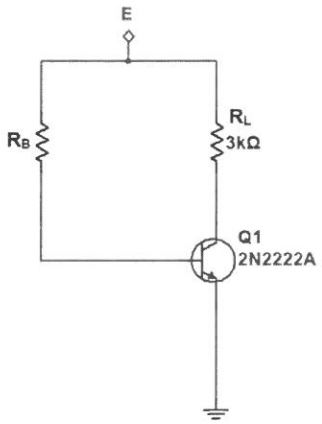


Figure Q5(a)

Using the I-V characteristics shown in the Appendix A, do the followings:

(i) Draw a load line on the characteristics determined by E = 21 V and R_L = 3 kΩ. Attach the Appendix A to your answer booklet. [2]

(ii) Choose an operating point midway between cutoff and saturation. Determine the value of R_B to establish the resulting operating point. [2]

(iii) What are the resulting values of I_{CQ} and V_{CEQ}? [1]

(iv) What is the value of β at the operating point? [1]

(v) What is the value of α defined by the operating point? [1]

(vi) What is the saturation current I_{Csat} for the design? [1]

(vii) What is the dc power dissipated by the device at the operating point? [1]

(viii) What is the power supplied by dc supply E? [1]

(ix) What is the power loss of the amplifier? [1]

(b) List the three different regions of a BJT transistor output characterisitcs. Explain an application for each region. [4]

(c) For the emitter-bias network of Figure 5(c) with the $\beta = 50$, determine:

(i) I_B and I_C [3]

(ii) V_{CE} [2]

(iii) V_C, V_E and V_B [3]

(iv) V_{BC} [2]

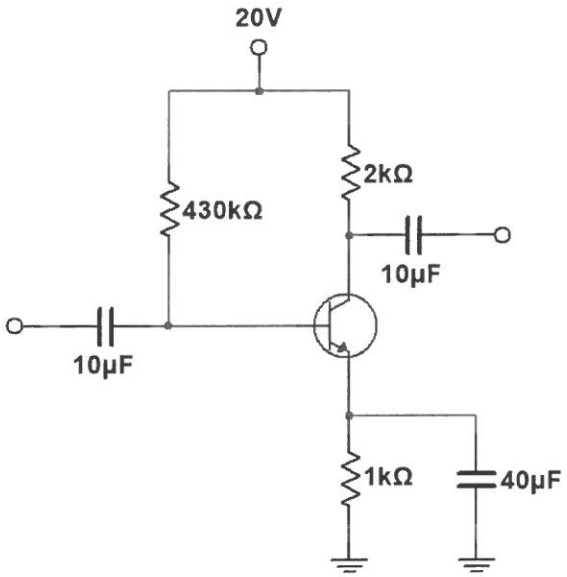


Figure Q5(c)

Question 6

(a) What are the major differences between the collector characteristics of a BJT transistor and the drain characteristics of a JFET transistor? [4]

(b) (i) Sketch the transfer characteristics directly from the drain characteristics given in Figure Q6(b). [4]

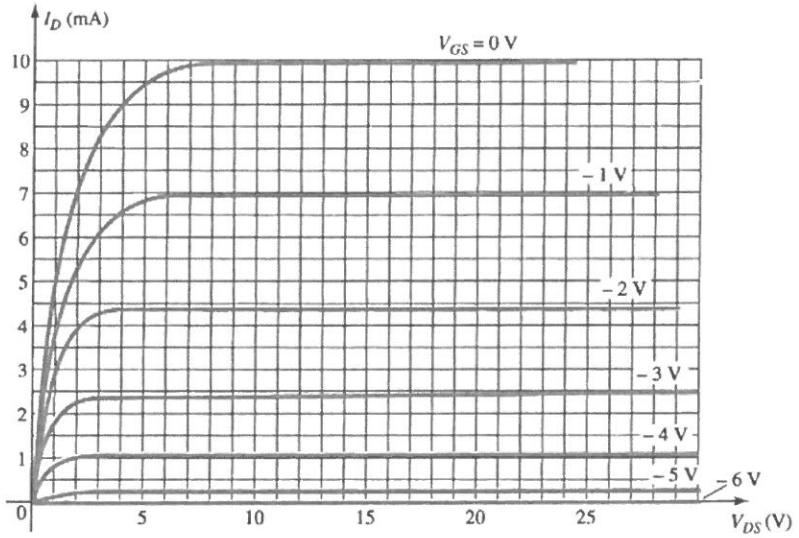


Figure Q6(b)

(ii) Using Figure Q6(b) to find the values of I_{DSS} and V_P, sketch the transfer characteristics using the Shockley's equation. [4]

(c) For the JFET network of Figure Q6(c) , when the $V_D = 9V$, determine:

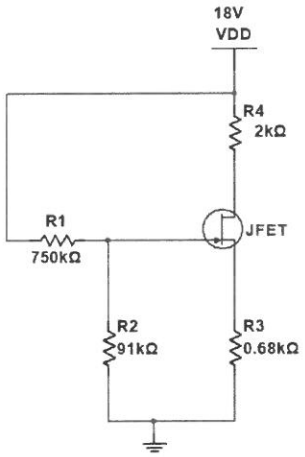


Figure Q6(c)

(i) I_D [2]

(ii) V_S and V_{DS} [3]

(iii) V_G and V_{GS} [2]

(iv) V_P [2]

(d) Sketch all the four symbols for enhancement type MOSFET. [4]

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Question: _____

Name: _____ **Student No:** _____

Appendix A

Transistor 2N2222A I_C vs V_{CE} curve