INTI
International College Penang

FINAL
Examination Paper

(COVER PAGE)

Session	:	**August 2018**
Programme	:	Diploma in Electrical and Electronic Engineering (DEEI)
Course	:	**EEE 2114: Introduction to Embedded Systems**
Date of Examination	:	12 December 2018 (Wednesday)
Time	:	11:00am – 1:00pm Reading Time : Nil
Duration	:	2 Hours
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL

Materials permitted :

Non-Programmable Scientific Calculator

Materials provided :

Appendix A, Appendix B & Appendix C

Examiner(s)	:	**Mr. Steven Khoo Boo Tap**
Moderator	:	Dr. Ooi Beng Lee

*This paper consists of **13** printed pages, including the cover page.*

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE2114: INTRODUCTION TO EMBEDDED SYSTEMS
FINAL EXAMINATION: AUGUST 2018 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

(a) Differentiate between PIC16F628A microcontroller and PIC16F877A microcontroller by completing Table 1a as shown below.

Table 1a Comparison between PIC16F628A and PIC16F877A microcontroller

Description	PIC16F628A	PIC16F877A
Ports		
Number of Analog Pins		
Total I/O Pins		
Data Memory (Bytes)		
Program Flash (Words)		
Data EEPROM (Bytes)		
ADC		
CCP		
SSP		
Internal Oscillator		

(10 marks)

(b) Given the Special Function Registers and File Registers for PIC16F877A microcontroller as follows:

Table 1(b)(i) Special Function Registers

Update Address	Symbol Name	Value
	WREG	0x32
003	STATUS	0x1F
004	FSR	0x70
006	PORTB	0X00
086	TRISB	0xFF

Table 1(b)(ii) File Registers

Address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
000	00	00	00	1F	70	00	00	--	--	--	16	77	00	--	00	00
010	10	20	00	--	--	00	55	33	60	00	00	--	--	--	--	00
020	61	12	10	56	34	18	52	AA	11	33	22	44	50	60	78	80
030	14	24	34	45	54	64	74	84	94	A4	B4	C4	D4	E4	F4	04
040	21	31	41	51	62	71	81	91	01	02	03	04	05	06	07	08
050	09	0A	0B	0C	0D	E0	0E	0F	F0	35	36	37	38	39	40	42
060	42	46	47	48	49	56	85	57	58	59	5A	5B	5C	5D	5E	5F
070	63	65	66	67	68	69	6A	6B	6C	6D	6E	6F	72	73	74	75
080	00	FF	00	1F	70	FF	00	--	--	--	16	77	70	--	08	--
090	--	--	FF	--	--	--	--	--	02	79	7A	7B	0C	00	--	6E
0A0	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	92	93
0B0	94	95	96	97	98	99	9A	9B	9C	9D	9F	9E	A0	B0	C0	D0
0C0	E0	F0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AD	AE
0D0	30	05	06	07	35	08	09	0A	0B	0C	0D	0E	0F	19	90	70

(All data of File Register are hexadecimal)

Perform the following short programs. Elaborate the result of the affected register(s) and Status (Z, DC and C) as shown in Table 1(b)(iii) using **Before** and **After** the execution of each instruction. The questions are independent of each other but the instructions are linked within the question.

Table 1(b)(iii) Before and After

Instruction	Before						After					
ANDLW 0X0F	W 32	FSR 70	70H 63	Z 1	DC 1	C 1	W	FSR	70H	Z	DC	C
COMF FSR,0												

(i)
```
ANDLW    0X0F
COMF     FSR,0
RRF      FSR,F
ADDWF    INDF,W
SWAPF    0x41,1
```

(5 marks)

(ii)
```
MOVLW    .32
RLF      FSR,W
ANDWF    INDF,F
IORWF    b'101010',1
DECF     0X42,0
```

(5 marks)

(iii)
```
MOVF     o'76',W
SUBWF    INDF,F
XORWF    FSR,1
SWAPF    0X43,F
INCF     INDF,0
```

(5 marks)

Question 2

(a) Table 2(a) assembly program will be built using MPLAB X IDE with MPASMWIN assembler. Study and analyze the Assembly Language Codes given below written using PIC16F628A microcontroller and answer the following questions.

Table 2(a) PIC16F628A Assembly Coding

Line 1	`INCLUDE <PIC16F628A.inc>`
Line 2	`__CONFIG 3F38H`
Line 3	`C EQU 0x0`
Line 4	`ORG 0`
Line 5	`movf 22H,W`
Line 6	`addwf 32,0`
Line 7	`btfss STATUS,C`
Line 8	`goto NC`
Line 9	`clf 0x41,1`
Line 10	`incf 41H,F`
Line 11	`movwf .66`
Line 12	`movf h'21',0`
Line 13	`addwf b'110001',W`
Line 14	`addwf 41h,1`
Line 15	`goto A`
Line 16	`NC movwf o'102'`
Line 17	`movf 21H,0`
Line 18	`addwf 0x31,W`
Line 19	`movwf d'101'`
Line 20	`A goto A`
Line 21	`END`

(i) Identify significant **ERROR(S)** in the instructions of Table 2(a) that will caused the assembler to output "BUILD FAILED" when build all. Explain why it is incorrect and write the correct codes according to the Assembly Language format. Indicate the Line number of the error code as well.

(3 marks)

(ii) Based on the assumption that all lines of codes are corrected, describe the function of the program and also provide a sample final result of Table 2(a) program after correction.

(4 marks)

(iii) Modify the program in Table 2(a) to less than 13 lines of coding but still perform the same outcome as the original function of the coding. Hint: The improved full program should be less than 13 lines of coding instead of 21 lines.

(8 marks)

(b) Figure 2(b) shows output connection of PIC16F877A microcontroller driving 5 LEDs in parallel configuration. Analyze if the circuit is going to work when Port D, RD1 is outputting a High or Logic 1? Referring to the Electrical Characteristics of the microcontroller as shown in Table 2(b), justify your explanation with calculation whether Figure 2(b) configuration is going to work or not. If not, then provide a solution.

(10 marks)

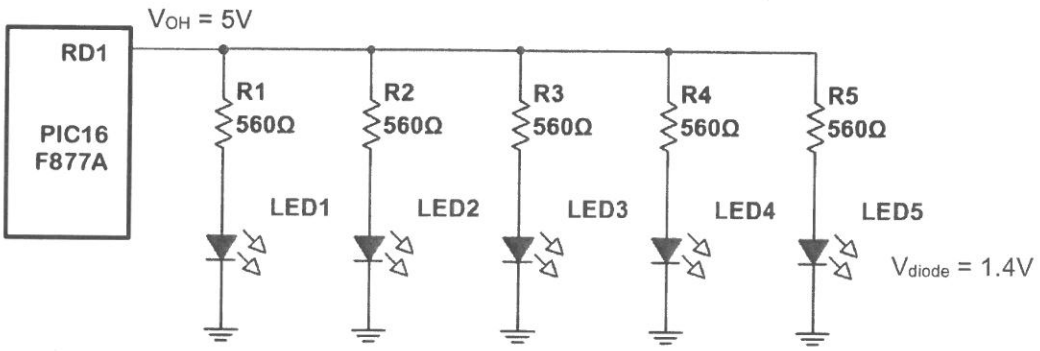


Figure 2(b)

Table 2(b) Electrical Characteristics

Absolute Maximum Ratings †

Ambient temperature under bias	-55 to +125°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to Vss (except VDD, $\overline{\text{MCLR}}$, and RA4)	-0.3V to (VDD + 0.3V)
Voltage on VDD with respect to Vss	-0.3 to +7.5V
Voltage on $\overline{\text{MCLR}}$ with respect to Vss **(Note 2)**	0 to +14V
Voltage on RA4 with respect to Vss	0 to +8.5V
Total power dissipation **(Note 1)**	1.0W
Maximum current out of Vss pin	300 mA
Maximum current into VDD pin	250 mA
Input clamp current, IIK (VI < 0 or VI > VDD)	± 20 mA
Output clamp current, IOK (VO < 0 or VO > VDD)	± 20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by PORTA, PORTB and PORTE (combined) **(Note 3)**	200 mA
Maximum current sourced by PORTA, PORTB and PORTE (combined) **(Note 3)**	200 mA
Maximum current sunk by PORTC and PORTD (combined) **(Note 3)**	200 mA
Maximum current sourced by PORTC and PORTD (combined) **(Note 3)**	200 mA

Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - Σ IOH} + Σ {(VDD - VOH) x IOH} + Σ(Vol x IOL)

2: Voltage spikes below Vss at the $\overline{\text{MCLR}}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{\text{MCLR}}$ pin rather than pulling this pin directly to Vss.

3: PORTD and PORTE are not implemented on PIC16F873A/876A devices.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Question 3

(a) Define embedded systems with the aid of diagram. Label the diagram clearly.

(5 marks)

(b) Describe the following serial communications used in PIC microcontroller with the aid of diagram. The description should include pin designations, data rate and data communication protocol.

(i) Universal Asynchronous Receiver Transmitter (UART)

(4 marks)

(ii) Universal Synchronous Asynchronous Receiver Transmitter (USART)

(4 marks)

(c) Describe and compare the serial communications used in PIC microcontroller shown in Figure 3(c).

(12 marks)

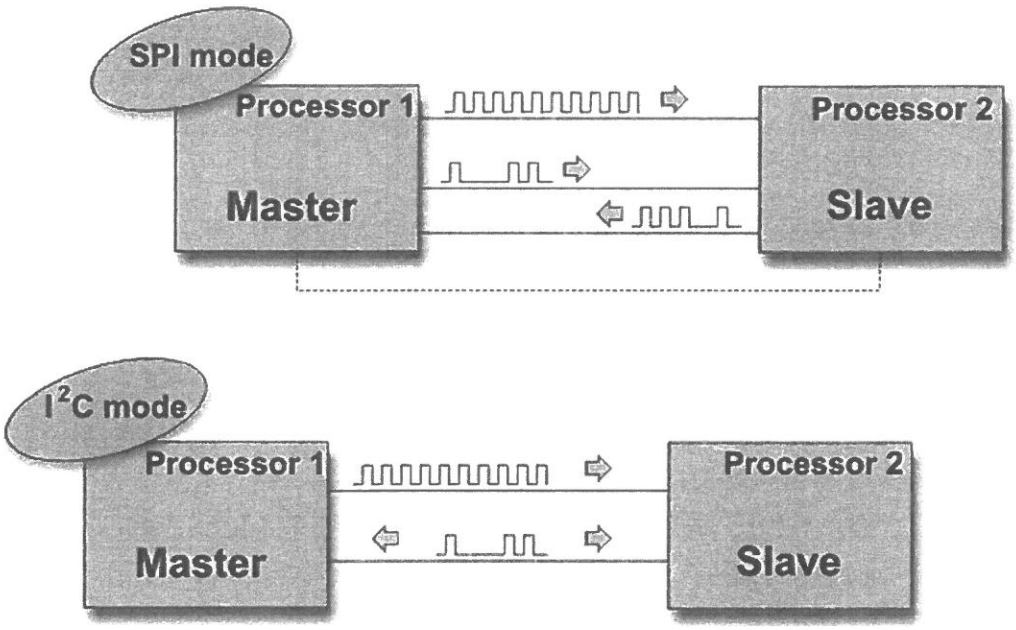


Figure 3(c)

Question 4

(a) Figure 4(a) shows the PIC to PIC communication via UART. Describe the UART communication between these 2 PIC microcontrollers. State on the typical baud rate used for this communication. Assume the communication protocol used is 8N1. The figure below shows communication between two PIC16F877A microcontrollers.

(7 marks)

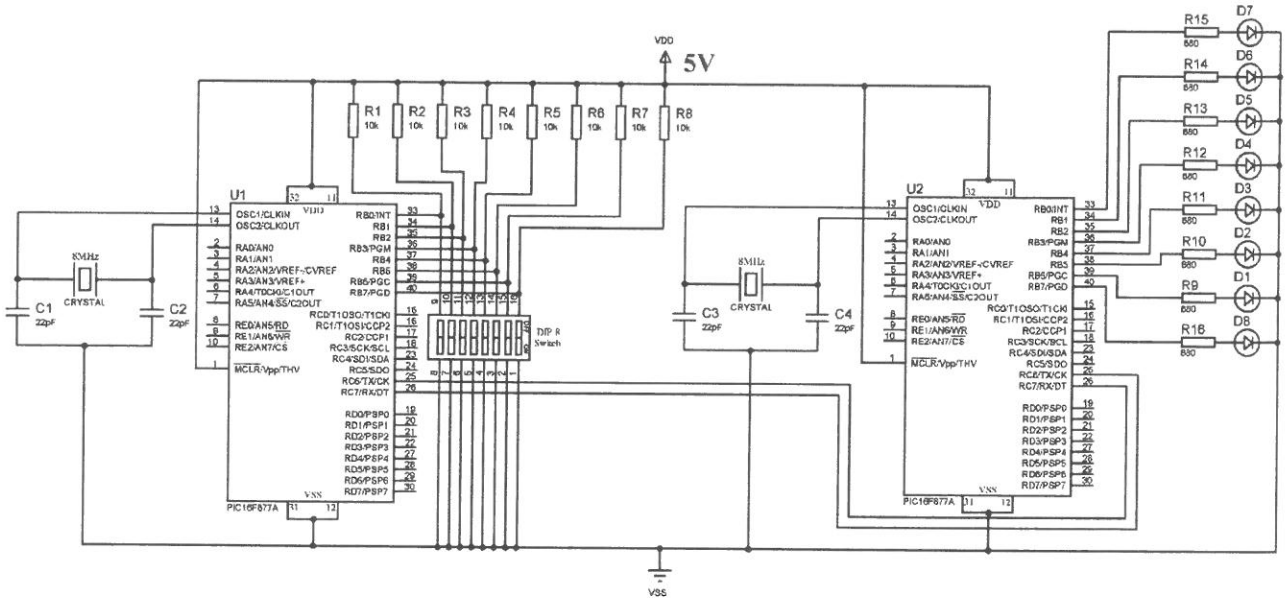


Figure 4(a)

(b) Describe the types of embedded systems for each classification:

(i) Networked embedded systems

(3 marks)

(ii) Mobile embedded systems

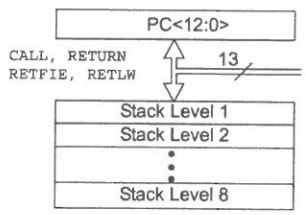
(3 marks)

(iii) Standalone embedded systems

(3 marks)

(c) With the aid of a simple diagram, describe the purpose and operation of the stack, when a PIC16F628A microcontroller executes a subroutine.

(9 marks)



TOS Stack Level	Return Address Location
	0x00 STKPTR
0	0000
1	0000
2	0000
3	0000
4	0000
5	0000
6	0000
7	0000

Figure 4(c)

Question 5

(a) Figure 5(a) below shows the Port B Functions of PIC16F877A microcontroller. Pin RB4:RB7 of PIC16F877A are normally used in keypad interfacing, explain why? Sketch the circuit diagram connection of Port B of PIC16F877A microcontroller and the 4 × 4 matrix keypad.

(8 marks)

Name	Bit#	Buffer	Function
RB0/INT	bit 0	TTL/ST(1)	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit 1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit 2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3/PGM(3)	bit 3	TTL	Input/output pin or programming pin in LVP mode. Internal software programmable weak pull-up.
RB4	bit 4	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB5	bit 5	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB6/PGC	bit 6	TTL/ST(2)	Input/output pin (with interrupt-on-change) or in-circuit debugger pin. Internal software programmable weak pull-up. Serial programming clock.
RB7/PGD	bit 7	TTL/ST(2)	Input/output pin (with interrupt-on-change) or in-circuit debugger pin. Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode or in-circuit debugger.

3: Low-Voltage ICSP Programming (LVP) is enabled by default which disables the RB3 I/O function. LVP must be disabled to enable RB3 as an I/O pin and allow maximum compatibility to the other 28-pin and 40-pin mid-range devices.

Figure 5(a)

(b) Explain THREE (3) types of memories available in the Peripheral Interface Controller (PIC) microcontroller and how each of them are being used by the programmer. Assume that the microcontroller is PIC16F877A microcontroller. The description should include the size and the range of each memory explained.

(9 marks)

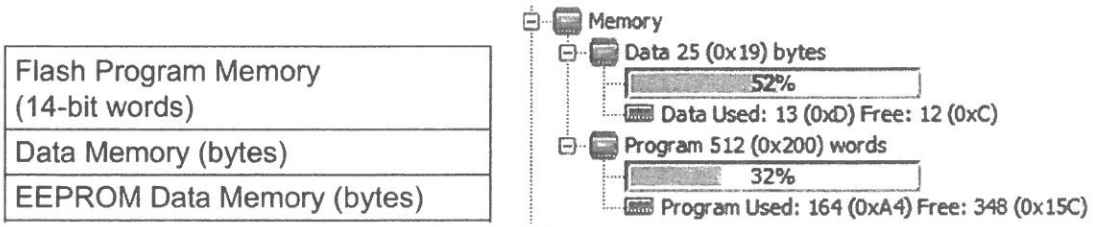


Figure 5(b)

(c) The block diagram of the PIC16F877A analogue to digital converter (ADC) is shown in Figure 5(c)(i). The ADCON0 and ADCON1 registers are shown in Figure 5(c)(ii) and Figure 5(c)(iii) respectively. In this design, an internal voltage reference is selected, input channel 3 is selected, and the ADC is switched on but not running. Assume that channel 0, channel 1, channel 2 and channel 4 are configured as analogue input only. Also, assume that the conversion clock used is Fosc/4 with left justification on the result.

(i) What is the setting of the ADCON0 register?

(2 marks)

(ii) What is the setting of the ADCON1 register?

(2 marks)

(iii) Give one advantage of using an internal voltage reference or an external voltage reference.

(4 marks)

A/D Block Diagram

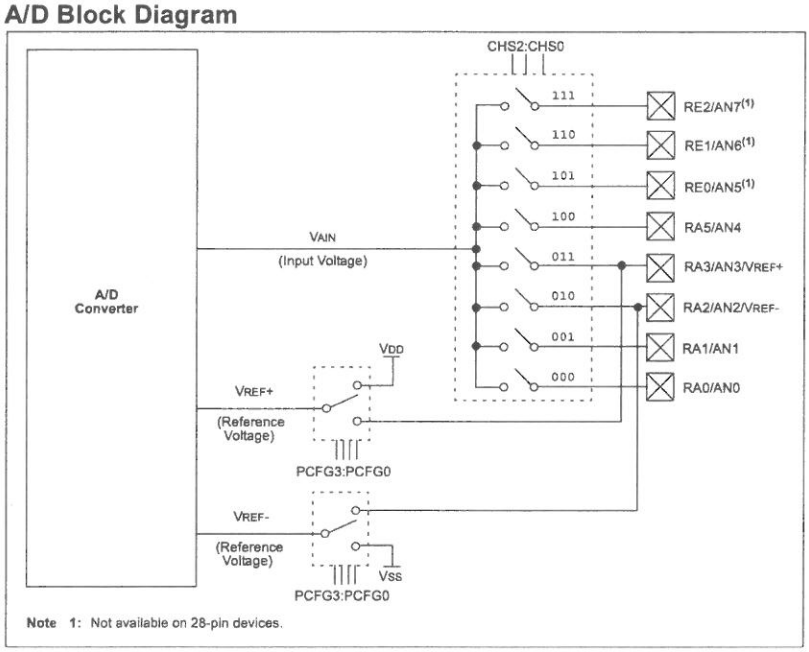


Figure 5(c)(i)

ADCON0: A/D CONTROL REGISTER 0

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	—	ADON
bit 7							bit 0

bit 7-6 **ADCS1:ADCS0:** A/D Conversion Clock Select bits (ADCON0 bits in **bold**)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	**00**	Fosc/2
0	**01**	Fosc/8
0	**10**	Fosc/32
0	**11**	FRC (clock derived from the internal A/D RC oscillator)
1	**00**	Fosc/4
1	**01**	Fosc/16
1	**10**	Fosc/64
1	**11**	FRC (clock derived from the internal A/D RC oscillator)

bit 5-3 **CHS2:CHS0:** Analog Channel Select bits

000 = Channel 0 (AN0)
001 = Channel 1 (AN1)
010 = Channel 2 (AN2)
011 = Channel 3 (AN3)
100 = Channel 4 (AN4)
101 = Channel 5 (AN5)
110 = Channel 6 (AN6)
111 = Channel 7 (AN7)

Note: The PIC16F873A/876A devices only implement A/D channels 0 through 4; the unimplemented selections are reserved. Do not select any unimplemented channels with these devices.

bit 2 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit

When ADON = 1:

1 = A/D conversion in progress (setting this bit starts the A/D conversion which is automatically cleared by hardware when the A/D conversion is complete)
0 = A/D conversion not in progress

bit 1 **Unimplemented:** Read as '0'

bit 0 **ADON:** A/D On bit

1 = A/D converter module is powered up
0 = A/D converter module is shut-off and consumes no operating current

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Figure 5(c)(ii)

ADCON1: A/D CONTROL REGISTER 1

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	ADCS2	—	—	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

bit 7 **ADFM:** A/D Result Format Select bit

1 = Right justified. Six (6) Most Significant bits of ADRESH are read as '0'.

0 = Left justified. Six (6) Least Significant bits of ADRESL are read as '0'.

bit 6 **ADCS2:** A/D Conversion Clock Select bit (ADCON1 bits in shaded area and in **bold**)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	00	Fosc/2
0	01	Fosc/8
0	10	Fosc/32
0	11	FRC (clock derived from the internal A/D RC oscillator)
1	00	Fosc/4
1	01	Fosc/16
1	10	Fosc/64
1	11	FRC (clock derived from the internal A/D RC oscillator)

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits

PCFG <3:0>	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	VREF+	VREF-	C/R
0000	A	A	A	A	A	A	A	A	VDD	VSS	8/0
0001	A	A	A	A	VREF+	A	A	A	AN3	VSS	7/1
0010	D	D	D	A	A	A	A	A	VDD	VSS	5/0
0011	D	D	D	A	VREF+	A	A	A	AN3	VSS	4/1
0100	D	D	D	D	A	D	A	A	VDD	VSS	3/0
0101	D	D	D	D	VREF+	D	A	A	AN3	VSS	2/1
011x	D	D	D	D	D	D	D	D	—	—	0/0
1000	A	A	A	A	VREF+	VREF-	A	A	AN3	AN2	6/2
1001	D	D	A	A	A	A	A	A	VDD	VSS	6/0
1010	D	D	A	A	VREF+	A	A	A	AN3	VSS	5/1
1011	D	D	A	A	VREF+	VREF-	A	A	AN3	AN2	4/2
1100	D	D	D	A	VREF+	VREF-	A	A	AN3	AN2	3/2
1101	D	D	D	D	VREF+	VREF-	A	A	AN3	AN2	2/2
1110	D	D	D	D	D	D	D	A	VDD	VSS	1/0
1111	D	D	D	D	VREF+	VREF-	D	A	AN3	AN2	1/2

A = Analog input D = Digital I/O

C/R = # of analog input channels/# of A/D voltage references

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Note: On any device Reset, the port pins that are multiplexed with analog functions (ANx) are forced to be an analog input.

Figure 5(c)(iii)

Question 6

(a) Table 6(a) shows partial Port B Functions of PIC16F628A microcontroller. Differentiate between the Schmitt Trigger (ST) input and TTL input. Assume that the microcontroller is operating at 5V voltage source.

(5 marks)

Name	Function	Input Type	Output Type	Description
RB0/INT	RB0	TTL	CMOS	Bidirectional I/O port. Can be software programmed for internal weak pull-up.
	INT	ST	–	External interrupt
RB1/RX/DT	RB1	TTL	CMOS	Bidirectional I/O port. Can be software programmed for internal weak pull-up.
	RX	ST	–	USART Receive Pin
	DT	ST	CMOS	Synchronous data I/O
RB2/TX/CK	RB2	TTL	CMOS	Bidirectional I/O port
	TX	–	CMOS	USART Transmit Pin
	CK	ST	CMOS	Synchronous Clock I/O. Can be software programmed for internal weak pull-up.

Table 6(a)

(b) Compare the operation of Figure 6(b-1) architecture with Figure 6(b-2) architecture. Name the architecture for Figure 6(b-1) and Figure 6(b-2).

(4 marks)

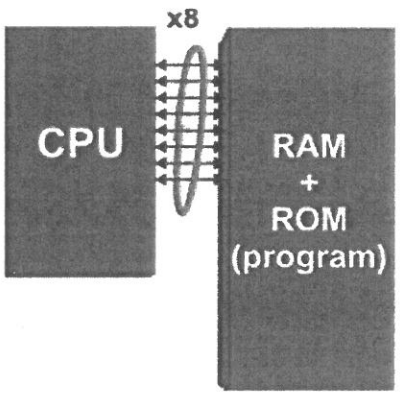


Figure 6(b-1)

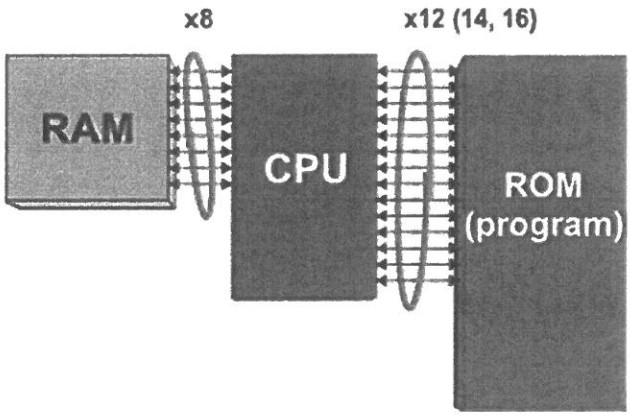


Figure 6(b-2)

(c) Name and describe the function of the following labels in Figure 6(c) as shown below.

(i) Label (A)

(3 marks)

(ii) Label (B)

(3 marks)

(iii) Label (C)

(3 marks)

(iv) Label (D)

(3 marks)

(v) Label (E)

(3 marks)

State the possible type of microcontroller for Figure 6(c) internal architecture.

(1 mark)

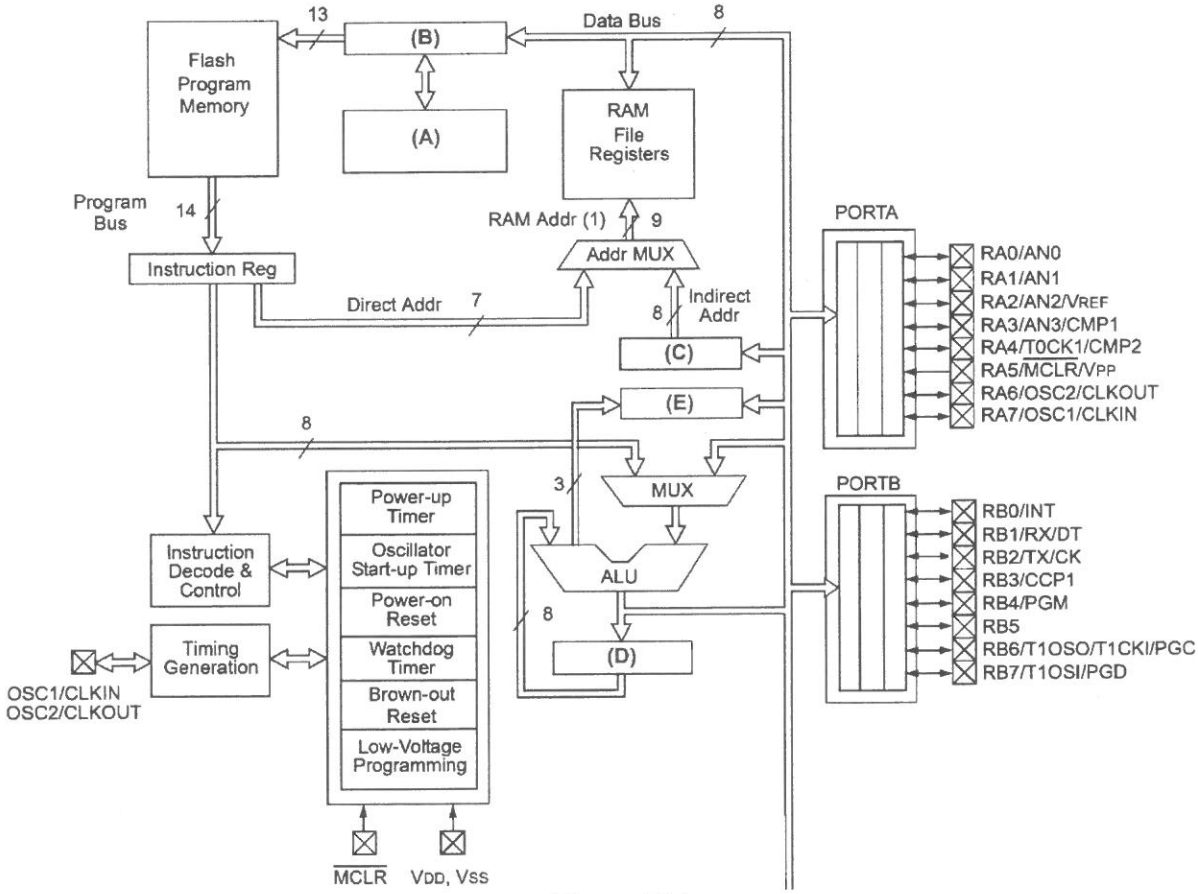


Figure 6(c)

– THE END –

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