



**INTI**  
International College Penang

**FINAL**  
Examination Paper

(COVER PAGE)

Session : August 2018

Programme : Diploma in Electrical and Electronic Engineering (DEEI)

Course : EEE 2101: Introduction to Digital Electronics

Date of Examination : 11 December 2018 (Tuesday)

Time : 11:00am – 1:00pm Reading Time : Nil

Duration : 2 Hours

Special Instructions :

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

**IMPORTANT NOTE : THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL**

Materials permitted :  
Non-Programmable Scientific Calculator

Materials provided :  
Nil

Examiner(s) : Mr. Steven Khoo Boo Tap

Moderator : Dr. Ooi Beng Lee

*This paper consists of 12 printed pages, including the cover page.*

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)  
 EEE2101: INTRODUCTION TO DIGITAL ELECTRONICS  
 FINAL EXAMINATION: AUGUST 2018 SESSION

**Instructions:** This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

**Question 1**

A combinational logic circuit is required, which accepts BCD inputs 0000 to 1001 and displays the number '0123456789', respectively, as shown below in Figure 1(a). The BCD inputs are labelled as RSTU, R is the MSB and U is the LSB. Figure 1(b) shows a Common-Anode 16 segment display. Assume all unused inputs as don't care. Show all working clearly.

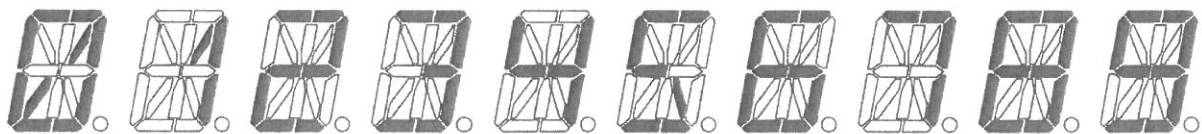


Figure 1(a)

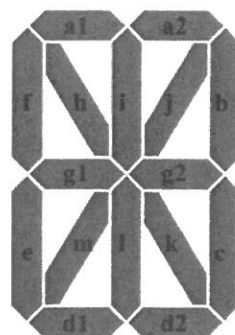


Figure 1(b)

- (a) Give the complete truth table for the inputs to segments a through m of the 16 segment including the unused inputs. (6 marks)
- (b) Find the simplest SOP form of the logic expression for segments e, f and g2 using Karnaugh map and/or Boolean algebra. (9 marks)
- (c) Design a logic circuit for segment e, f and g2 using only 2-input NAND gates with minimum gates consideration. State the number of 7400 ICs used. (10 marks)

**Question 2**

- (a) Table 2(a) and Table 2(b) show a portion of a dual positive edge-triggered JK flip-flops (DM7476) and a triple 3-input AND gate datasheet respectively. Figure 2(a) show the logic circuit diagram of an asynchronous counter which uses positive edge-triggered JK flip-flops with labelling of  $Q_A Q_B Q_C Q_D Q_E$  where  $Q_E$  is MSB and  $Q_A$  is LSB. Assume the environment is at  $T_A = 25^\circ\text{C}$  with  $V_{CC} = 5\text{V}$ .

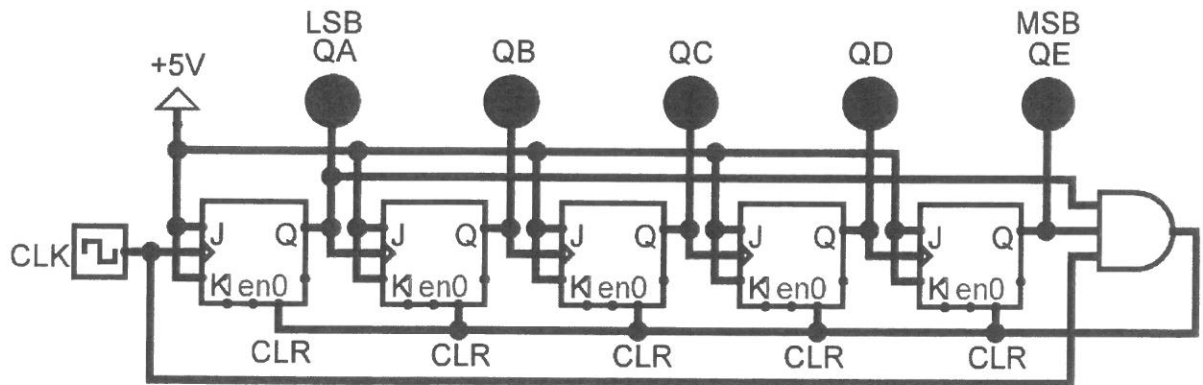


Figure 2(a)

Switching Characteristics					
at $V_{CC} = 5\text{V}$ and $T_A = 25^\circ\text{C}$					
Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega, C_L = 15\text{pF}$		Units
			Min	Max	
$f_{MAX}$	Maximum Clock Frequency		15		MHz
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	Preset to $\bar{Q}$		40	ns
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	Preset to Q		25	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Q		40	ns
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	Clear to $\bar{Q}$		25	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Q or $\bar{Q}$		40	ns
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Q or $\bar{Q}$		25	ns

Table 2(a) JK flip-flop

Symbol	From (Input)	To (Output)	Test Conditions	Min	Typ	Max	Units
$t_{PLH}$	A, B or C	Y	$C_L = 15\text{ pF}, R_L = 2\text{ k}\Omega$		8	27	ns
$t_{PHL}$					10	19	ns

Table 2(b) AND gate

- (i) Analyse its operation to determine whether the logic circuit of Figure 2(a) is working as a counter or not. If not working, justify and suggest a suitable modification for the logic circuit to function as a counter. (3 marks)
- (ii) Determine the total propagation delay from the given datasheets in Table 2(a) and Table 2(b). (3 marks)
- (iii) Find the maximum frequency at which the counter can be operated stably. (2 marks)
- (iv) Determine the output timing diagram of Figure 2(a) with proper labelling and state the exact function of this counter. (5 marks)
- (b) Find the following number system transformation. Show all workings clearly.
- (i)  $[127.35_8 - 1F.D8_{16}]$  to BCD equivalent with full BCD points accuracy. (4 marks)
- (ii)  $[216.01_8 \times 1010.1_2]$  to decimal equivalent with 5 decimal points accuracy. (4 marks)
- (iii)  $[163.75_{10} - 12.18_{16}]$  to binary equivalent with 5 binary points accuracy. (4 marks)

### Question 3

- (a) Table 3(a) shows a portion of quadruple 2-input XOR gates (DM7486) datasheet. Find the following parameters from this datasheet, show all working clearly:
- (i) Fan-out, a gate can safely drive. (3 marks)
- (ii) Average Power dissipation,  $P_{D(avg)}$  for one gate on a DM7486 IC. (3 marks)
- (iii) Noise Margin voltages,  $V_{NL}$  and  $V_{NH}$ . (3 marks)

### Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V <sub>CC</sub>	Supply Voltage	4.75	5	5.25	V
V <sub>IH</sub>	HIGH Level Input Voltage	2			V
V <sub>IL</sub>	LOW Level Input Voltage			0.8	V
I <sub>OH</sub>	HIGH Level Output Current			-0.4	mA
I <sub>OL</sub>	LOW Level Output Current			8	mA
T <sub>A</sub>	Free Air Operating Temperature	0		70	°C

### Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = -18 mA			-1.5	V
V <sub>OH</sub>	HIGH Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max, V <sub>IL</sub> = Max, V <sub>IH</sub> = Min	2.7	3.4		V
V <sub>OL</sub>	LOW Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max, V <sub>IL</sub> = Max, V <sub>IH</sub> = Min		0.35	0.5	V
		I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min		0.25	0.4	
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 7V			0.2	mA
I <sub>IH</sub>	HIGH Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 2.7V			40	μA
I <sub>IL</sub>	LOW Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V			-0.6	mA
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 3)	-20		-100	mA
I <sub>CCH</sub>	Supply Current with Outputs HIGH	V <sub>CC</sub> = Max (Note 4)		6.1	10	mA
I <sub>CCL</sub>	Supply Current with Outputs LOW	V <sub>CC</sub> = Max (Note 5)		9	15	mA

Note 2: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I<sub>CCH</sub> is measured with all outputs OPEN, one input at each gate at 4.5V, and the other inputs grounded.

Note 5: I<sub>CCL</sub> is measured with all outputs OPEN and all inputs grounded.

### Switching Characteristics

at V<sub>CC</sub> = 5V and T<sub>A</sub> = 25°C

Symbol	Parameter	Conditions	R <sub>L</sub> = 2 kΩ				Units
			C <sub>L</sub> = 15 pF		C <sub>L</sub> = 50 pF		
			Min	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay Time LOW-to-HIGH Level Output	Other Input		18		23	ns
t <sub>PHL</sub>	Propagation Delay Time HIGH-to-LOW Level Output	Low		17		21	ns
t <sub>PLH</sub>	Propagation Delay Time LOW-to-HIGH Level Output	Other Input		10		15	ns
t <sub>PHL</sub>	Propagation Delay Time HIGH-to-LOW Level Output	High		12		15	ns

Table 3(a)

- (b) Express Figure 3(b) to the simplest form using minimum gate count regardless of the types. Note that a NOT gate is also counted as one gate. Show working clearly.

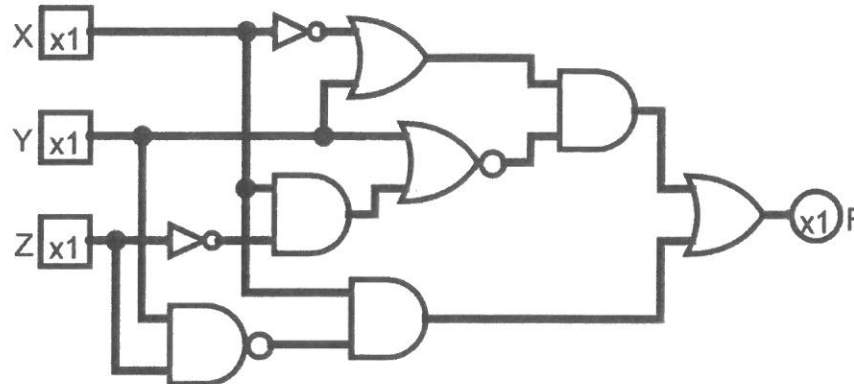


Figure 3(b)

(8 marks)

- (c) Figure 3(c) shows the pin diagram and logic symbol of 74LS283 4-bit adder with (pin numbers in parentheses). Show how two 74LS283 adders can be connected to form an 8-bit parallel adder. Show final output functions of the 8-bit parallel adder for the following 8-bit input numbers:

$$A_8A_7A_6A_5A_4A_3A_2A_1 = 10111001 \text{ and } B_8B_7B_6B_5B_4B_3B_2B_1 = 10011110.$$

Show the adders with proper interconnections labelling. Indicate the Low-order adder and High-order adder in details. Label the sum output as  $\Sigma_8\Sigma_7\Sigma_6\Sigma_5\Sigma_4\Sigma_3\Sigma_2\Sigma_1$  and the carry output as  $\Sigma_9$ .

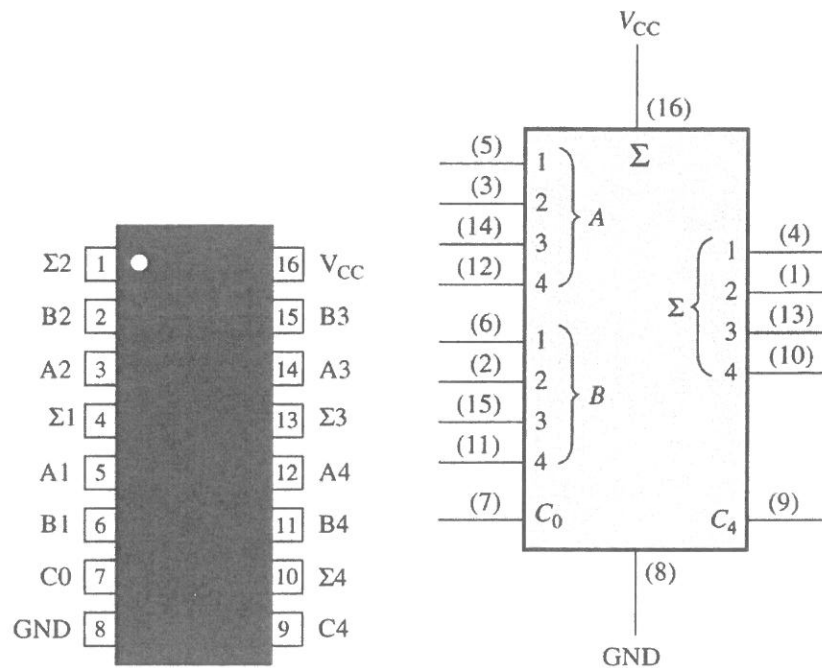


Figure 3(c)

(8 marks)

**Question 4**

- (a) For the given truth tables in Table 4a(i) and excitation tables in Table 4a(ii),
- (i) design a D flip-flop function using JK flip-flop. The design can be added with additional gates in order to fulfil the conversion. Show all working clearly for JK-to-D converter. (5 marks)
  - (ii) design a T flip-flop function using SR flip-flop. The design can be added with additional gates in order to fulfil the conversion. Show all working clearly for SR-to-T converter. (5 marks)

Table 4a(i) Flip-flop Truth Tables

Inputs		Outputs	
S	R	$Q_n$	$Q_{n+1}$
0	0	No Change	
0	1	Reset	
1	0	Set	
1	1	Invalid	

Inputs		Outputs	
J	K	$Q_n$	$Q_{n+1}$
0	0	No Change	
0	1	Reset	
1	0	Set	
1	1	Toggle	

Input	Outputs	
D	$Q_n$	$Q_{n+1}$
0	0	0
0	1	0
1	0	1
1	1	1

Input	Outputs	
T	$Q_n$	$Q_{n+1}$
0	0	0
0	1	1
1	0	1
1	1	0

$Q_n$ : Present State  
 $Q_{n+1}$ : Next State

Table 4a(ii) Flip-flop Excitation Tables

Outputs		Inputs	
$Q_n$	$Q_{n+1}$	S	R
0	0	0	×
0	1	1	0
1	0	0	1
1	1	×	0

Outputs		Inputs	
$Q_n$	$Q_{n+1}$	J	K
0	0	0	×
0	1	1	×
1	0	×	1
1	1	×	0

Outputs		Input
$Q_n$	$Q_{n+1}$	D
0	0	0
0	1	1
1	0	0
1	1	1

Outputs		Input
$Q_n$	$Q_{n+1}$	T
0	0	0
0	1	1
1	0	1
1	1	0

$Q_n$ : Present State  
 $Q_{n+1}$ : Next State

- (b) Refer to Figure 4(b) where an analog-to-digital converter is monitoring the dc voltage of a 15V storage battery on an orbiting spaceship. The converter's output is a 4-bit binary number, RSTU, corresponding to the battery voltage in steps of 1V, with R as the MSB. The converter's binary outputs are fed to a logic circuit that is to produce a HIGH output as long as the binary value is between  $0100_2 = 4_{10}$  and  $1100_2 = 12_{10}$ ; that is, the battery voltage is maintained between 4V and 12V. Show all working steps.

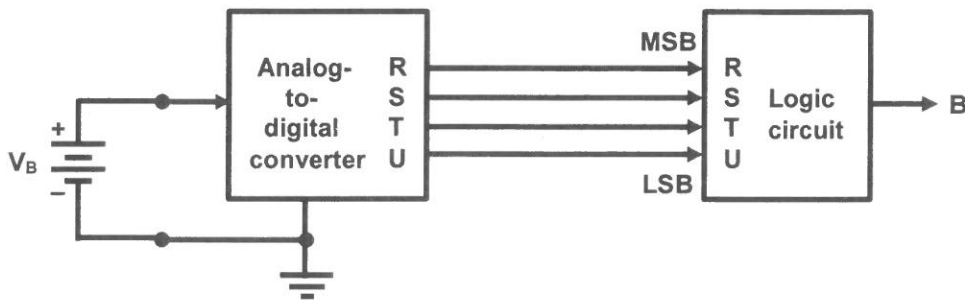


Figure 4(b)

- (i) Give the complete truth-table of the converter logic circuit system. (2 marks)
- (ii) Give the simplest expression for the converter logic circuit system using Karnaugh Map. (3 marks)
- (iii) Design the logic circuit for the converter logic circuit system using only NOR gates with minimum IC consideration. (3 marks)
- (iv) Build the expression obtained in Question 4(b)(ii) using an 4-to-1 MUX with S & T as the select lines. (4 marks)
- (v) If the company had decided to use only NAND gates for the converter logic design, design the complete simplest circuit for the converter logic circuit system with minimum gates consideration. (3 marks)

**Question 5**

- (a) Table 5(a) shows the current ratings of TTL series logic gates. A 74AS00 NAND gate output is driving a few other TTL outputs as shown in Figure 5(a). Determine if there is a loading problem.

(4 marks)

TTL Series	Output Drive		Input Loading	
	$I_{OH}$	$I_{OL}$	$I_{IH}$	$I_{IL}$
74	400 $\mu$ A	16mA	40 $\mu$ A	1.6mA
74S	1.0mA	20mA	50 $\mu$ A	2.0mA
74LS	400 $\mu$ A	8mA	20 $\mu$ A	400 $\mu$ A
74AS	2.0mA	20mA	200 $\mu$ A	2.0mA
74ALS	400 $\mu$ A	8mA	20 $\mu$ A	100 $\mu$ A
74F	1.0mA	20mA	20 $\mu$ A	600 $\mu$ A

Table 5(a)

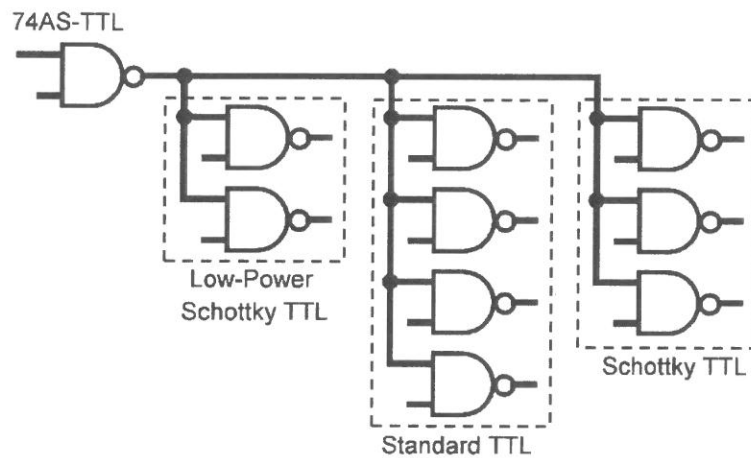


Figure 5(a)

The 74AS00 NAND gate output needs to be used to drive some 74AS inputs in addition to the load inputs. Determine how many additional 74AS inputs could the output drive without being overloaded?

(3 marks)

- (b) Express the following Boolean expression using Karnaugh Map and/or Boolean expression to the most simplified form:

(i)  $F_1(W, X, Y, Z) = \prod(3,4,6,7,8,10,12,14)$  to the simplest SOP form.

(4 marks)

(ii)  $F_2(R, S, T, U) = \sum(0,1,2,5,6,10,11,15)$  to the simplest POS form.

(4 marks)

- (c) Design a synchronous 3-bit up/down counter using positive edge-triggered SR flip-flop for MSB, T flip-flop for second bit and JK flip-flop for LSB. Assume  $S_2$  &  $R_2$  are the MSB input,  $T_1$  is the next flip-flop inputs and  $J_0$  &  $K_0$  are the LSB inputs. Assume all unused states as don't care.

Input  $Z$  will be used as the up/down control. The counter will count from  $0 \Rightarrow 7 \Rightarrow 6 \Rightarrow 5 \Rightarrow 4 \Rightarrow 3 \Rightarrow 0$  when input,  $Z = 0$  and  $3 \Rightarrow 4 \Rightarrow 5 \Rightarrow 6 \Rightarrow 7 \Rightarrow 0 \Rightarrow 3$  when input,  $Z = 1$  as shown below in Figure 5(c).

Use  $Q_2Q_1Q_0$  outputs labelling for  $S_2$  &  $R_2$ ,  $T_1$  and  $J_0$  &  $K_0$  inputs. Provide proper labelling for the designed logic circuit. Show all workings clearly. The design should be at minimum gates.

- (i) Prepare the transition table/next state table for the up/down counter. (3 marks)
- (ii) Simplify using Karnaugh map and/or Boolean algebra to the simplest form. (4 marks)
- (iii) Design the complete logic circuit diagram with proper label using minimum gates consideration. (3 marks)

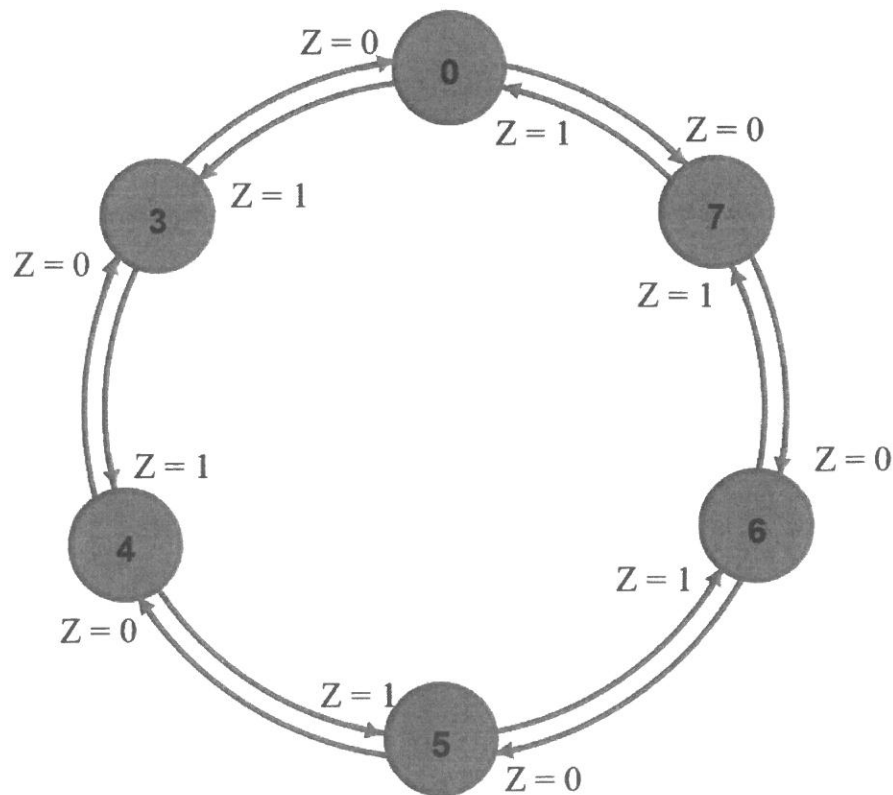
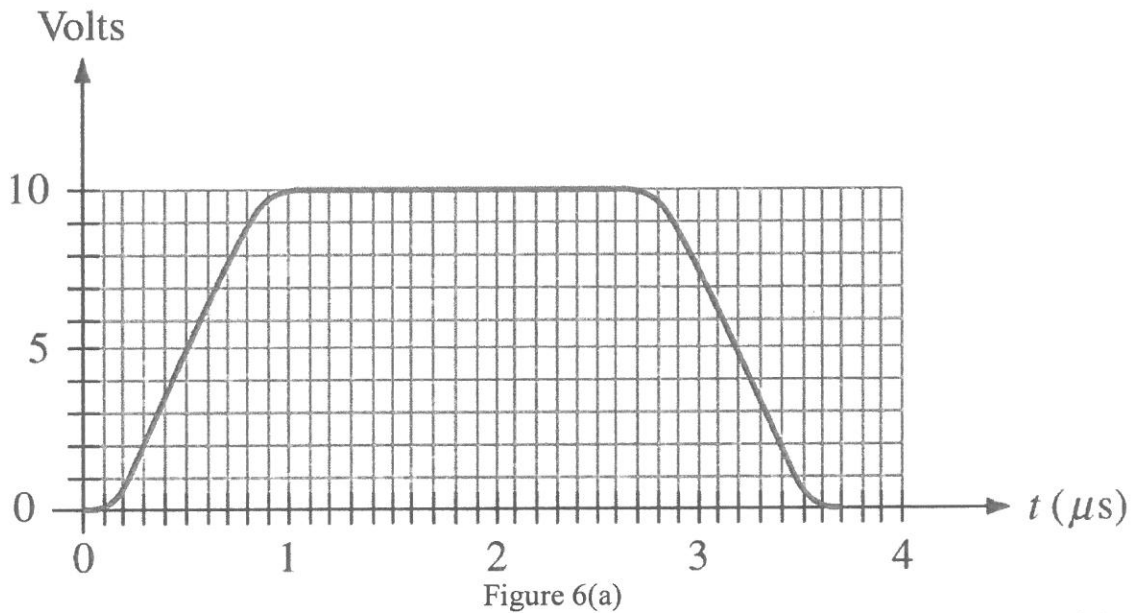


Figure 5(c)

**Question 6**

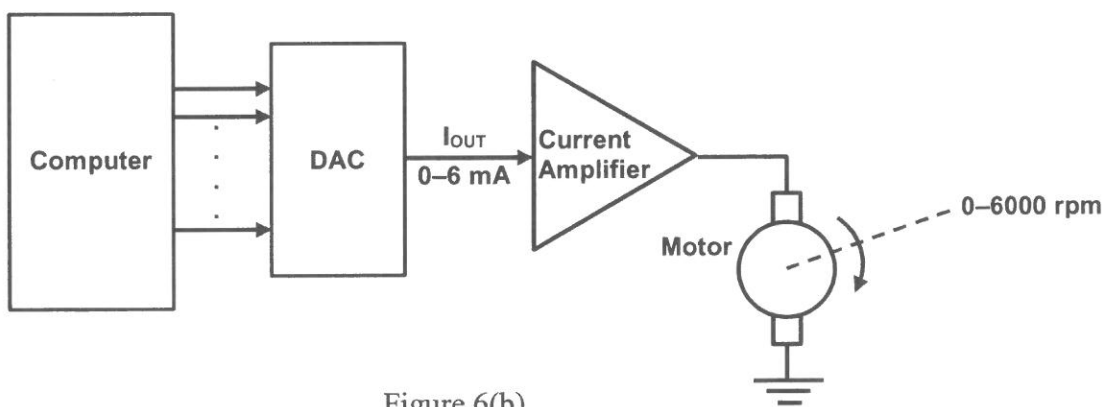
- (a) For the pulse shown in Figure 6(a) below, determine the Rise time, Fall time, Pulse time and Amplitude from the graph as accurate as possible.



(4 marks)

- (b) Figure 6(b) shows a computer controlling the speed of a motor. The 0 to 6mA analog current from the DAC is amplified to produce motor speeds from 0 to 6000 rpm (revolutions per minute). Explain how many bits should be used if the computer is to be able to produce a motor speed that is within 3 rpm of the desired speed?

(6 marks)



Using the number of bits obtained, explain how close to 832 rpm can the motor speed be adjusted?

(6 marks)

- (c) A 10-bit DAC produces an output current in proportion to its digital input. For a digital input of 0000101000, an output current of 75mA is produced.
- (i) Determine the output current be if the digital input is 0111000111. (3 marks)
  - (ii) Determine the maximum output current produced by this DAC. (3 marks)
  - (iii) Determine the digital input if a 105mA output current is required. (3 marks)

– THE END –

EEE2101(F)/Aug18/Steven Khoo/16/08/18