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INTERNATIONAL COLLEGE PENANG (507232-U)
LAUREATE INTERNATIONAL UNIVERSITIES

FINAL
Examination Paper

(COVER PAGE)

Session	:	**AUGUST 2014**
Programme	:	DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING
Course	:	**EEE 2101: INTRODUCTION TO DIGITAL ELECTRONICS**
Date of Examination	:	December 9, 2014 (Tuesday)
Time	:	5.00pm – 7.00pm Reading Time : Nil
Duration	:	2 Hours
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Students are not allowed to remove the question papers from the examination venue.

Materials permitted :

NON-PROGRAMMABLE SCIENTIFIC CALCULATOR

Materials provided :

Nil

Examiner(s)	:	**Mr. Steven Khoo**
Moderator	:	**Dr. Khoo Bee Ee**

This paper consists of 11 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEE/I)

EEE2101: INTRODUCTION TO DIGITAL ELECTRONICS
FINAL EXAMINATION: AUG2014 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

(a) Simplify the Boolean expression:
$F = (xyz + uv)(x + \overline{y} + \overline{z} + uv)$

i) Using Boolean algebra only.

(3 marks)

ii) Design using only basic logic gates (AND, OR, NOT) and draw the logic circuit with minimum IC usage and minimum gates consideration.

(4 marks)

(b) Perform the following number system transformation. Show all workings clearly.

i) 2014.2014_8 to decimal equivalent.

(3 marks)

ii) 2014.2014_{10} to hexadecimal equivalent.

(3 marks)

iii) $[010001100111_2 + 001101110111_2]$ to BCD equivalent.

(3 marks)

(c) Refer to Figure 1(c) where an analog-to-digital converter is monitoring the dc voltage of a 15V storage battery on an orbiting spaceship. The converter's output is a 4-bit binary number, ABCD, corresponding to the battery voltage in steps of 1V, with A as the MSB. The converter's binary outputs are fed to a logic circuit that is to produce a HIGH output as long as the binary value is between $1000_2 = 8_{10}$ and $1100_2 = 12_{10}$; that is, the battery voltage is maintained between 8V and 12V. Show all working steps.

i) Provide a truth table for the logic circuit.

(2 marks)

ii) Simplify the Boolean expression using Karnaugh map or Boolean Algebra.
(3 marks)

iii) Design the logic circuit using only SN7402 (2-input NOR gates).
(4 marks)

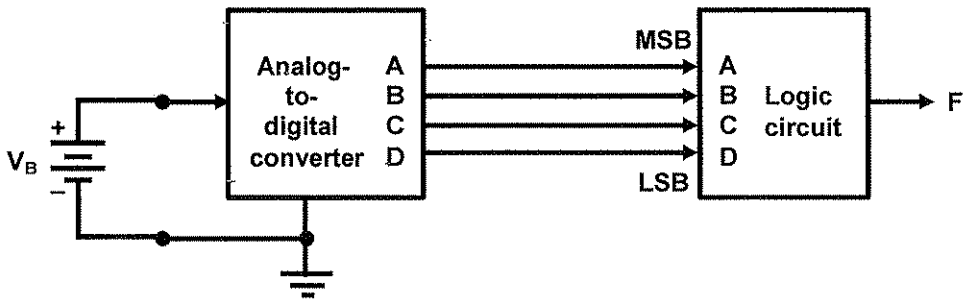


Figure 1(c)

Question 2

(a) The logic circuit in Figure 2(a) below is used to control the drive spindle motor for a turbine engine when the microcomputer is sending data to or receiving data from the turbine controller. The circuit will turn on the motor when SPIN = 1. Use the K, L and M test points to assist in determining the input conditions necessary to turn on the motor.

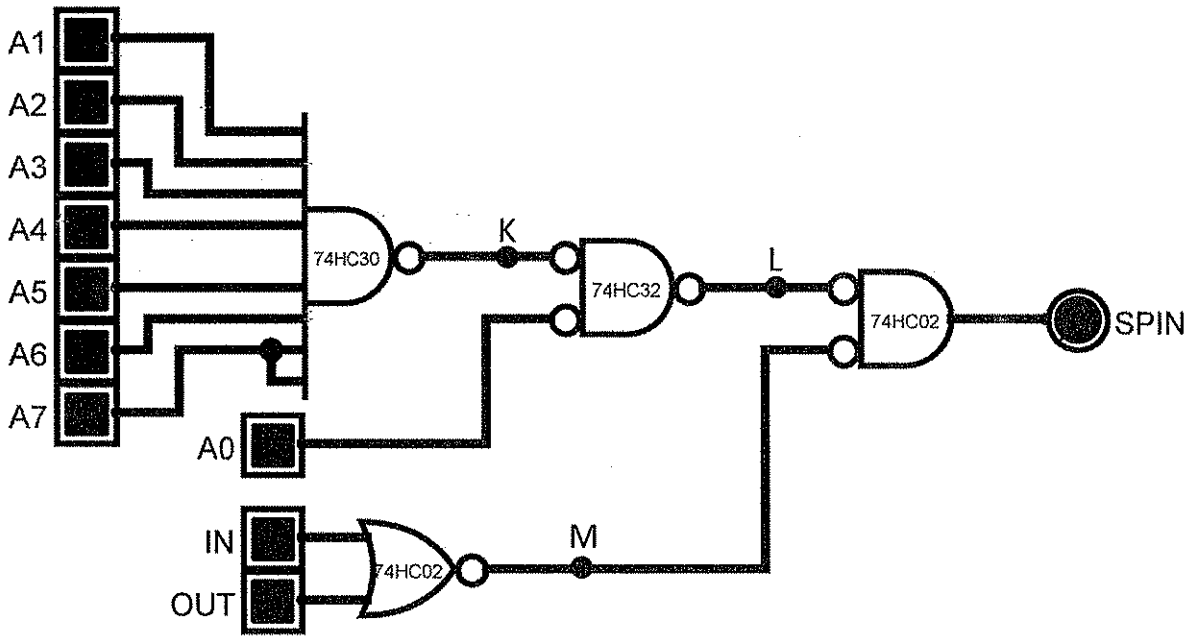


Figure 2(a)

(6 marks)

(b) Determine the input condition(s) needed to produce F = 0 in Figure 2(b).

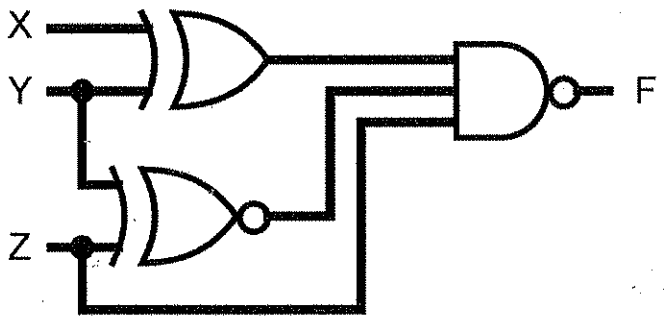


Figure 2(b)

(3 marks)

(c) Figure 2(c) below shows a four-bit parallel counter which is designed so that it does not sequence through the entire 16 binary states. Analyse its operation by determining its counting sequence. Assume that all flip-flops are initially in the 0 state. Flip-flop D is MSB. Show all workings clearly.

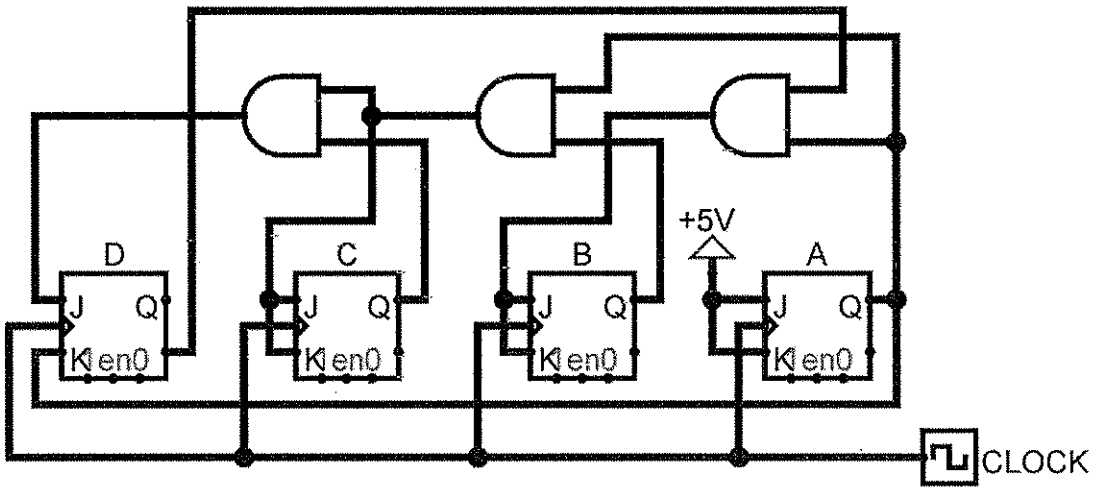


Figure 2(c)

i) Provide the Boolean expressions from the logic circuit.

(2 marks)

ii) Provide all Karnaugh maps according to the expressions.

(4 marks)

iii) Provide the transition table/ next state table with excitation table.

(5 marks)

iv) Draw the waveforms at each flip-flop output, state diagram and comment on the obtained.

(5 marks)

Question 3

(a) The logic circuit of Table 3(a) generates two outputs, MEM1 and MEM2 that are used to activate the memory ICs in a particular microcomputer as shown in the truth table below.

Inputs			Outputs	
R	S	T	MEM1	MEM2
0	0	0	0	0
0	0	1	0	1
0	1	x	1	0
1	0	x	0	1
1	1	x	1	0

Table 3(a)

i) Provide Boolean equations for outputs MEM1 and MEM2 in terms of R, S and T. (2 marks)

ii) Draw a logic circuit to carry out this truth table with minimum number of gates used for this implementation. Hint: compare among NAND gates only, NOR gates only and basic logic gates (AND, OR, NOT) implementation. (6 marks)

(b) Use the given Karnaugh map and Boolean algebra to obtain the minimum

i) SOP expression for the function, $F(R,S,T,U)=\sum(1,2,4,7,8,11,13,14)$.

RS \ TU	00	01	11	10
00				
01				
11				
10				

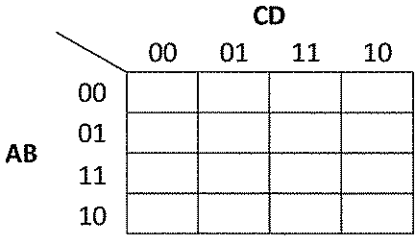
(3 marks)

ii) POS expression for the function, $F(W,X,Y,Z)=\sum(0,2,4,6,8,10,13,15)$.

WX \ YZ	00	01	11	10
00				
01				
11				
10				

(3 marks)

iii) SOP expression for the function, $F(A,B,C,D)=\sum m(0,4,5,8,10,15)+d(2,7,9,13)$.



(3 marks)

(c) Table 3(c) shows the current ratings of TTL series logic gates. A 74ALS02 NOR gate output is driving three 74S gate inputs and one 7405 input. Determine if there is a loading problem.

(4 marks)

TTL Series	Outputs		Inputs	
	I_{OH}	I_{OL}	I_{IH}	I_{IL}
74	–0.4mA	16mA	40μA	–1.6mA
74S	–1.0mA	20mA	50μA	–2.0mA
74LS	–0.4mA	8mA	20μA	–0.4mA
74AS	–2.0mA	20mA	20μA	–0.5mA
74ALS	–0.4mA	8mA	20μA	–0.1mA
74F	–1.0mA	20mA	20μA	–0.6mA

Table 3(c)

The 74ALS02 NOR gate output needs to be used to drive some 74ALS inputs in addition to the load inputs. How many additional 74ALS inputs could the output drive without being overloaded?

(4 marks)

Question 4

(a) Design a synchronous 3-bit up/down counter using positive edge-triggered JK flip-flop for MSB, T flip-flop for second bit and D flip-flop for LSB. Assume all unused states as don't care. Input S will be used as the up/down control. The counter will count from 1 ⇨ 3 ⇨ 5 ⇨ 7 ⇨ 1 when input, Z = 0 and 7 ⇨ 5 ⇨ 3 ⇨ 1 ⇨ 7 when input, Z = 1. Provide proper labelling for the designed logic circuit. Show all workings clearly.

i) Draw a state diagram with up/down condition.

(2 marks)

ii) Provide all excitation tables used.

(2 marks)

iii) Provide the transition table/ next state table.

(4 marks)

iv) Simplify using Karnaugh map or Boolean algebra.

(4 marks)

v) Draw the complete logic circuit diagram with proper label.

(3 marks)

(b) Figure 4(b) shows a computer controlling the speed of a motor. The 0 to 2mA analog current from the DAC is amplified to produce motor speeds from 0 to 1000 rpm (revolutions per minute). How many bits should be used if the computer is to be able to produce a motor speed that is within 2 rpm of the desired speed?

(5 marks)

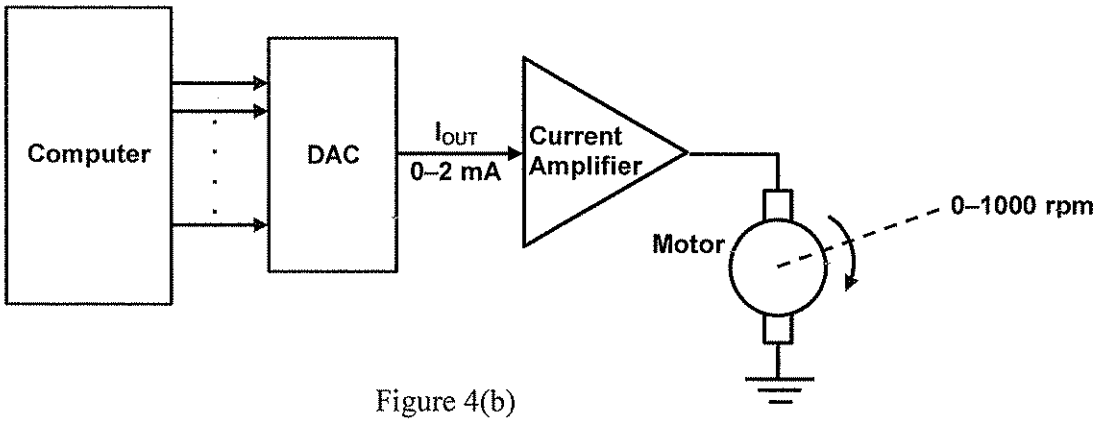


Figure 4(b)

Using the number of bits obtained, how close to 236 rpm can the motor speed be adjusted?

(5 marks)

Question 5

(a) Design a circuit with the following requirements:
An input for tail lights both on.
An input for right turn that lets the signal "OSC" control right tail light.
An input for left turn that lets the signal "OSC" control left tail light.

Note: "OSC" will make the light flash on and off as a turn indicator.
AND and OR gates with inversion bubbles are allowed.
There are four inputs "TAIL", "RIGHT", "LEFT" and "OSC".
There are two outputs "RIGHT_LEFT" and "LEFT_RIGHT".

i) Draw the required logic circuit with clear labelling.

(5 marks)

ii) A new requirement is added, the flashers must over ride all other signals and make "OSC" drive both right and left tail lights. Use input "FLASH" to build on the existing design in Q5a(i).

(4 marks)

(b) Figure 5(b) shows a simple DAC using an op-amp summing amplifier with binary-weighted resistors.

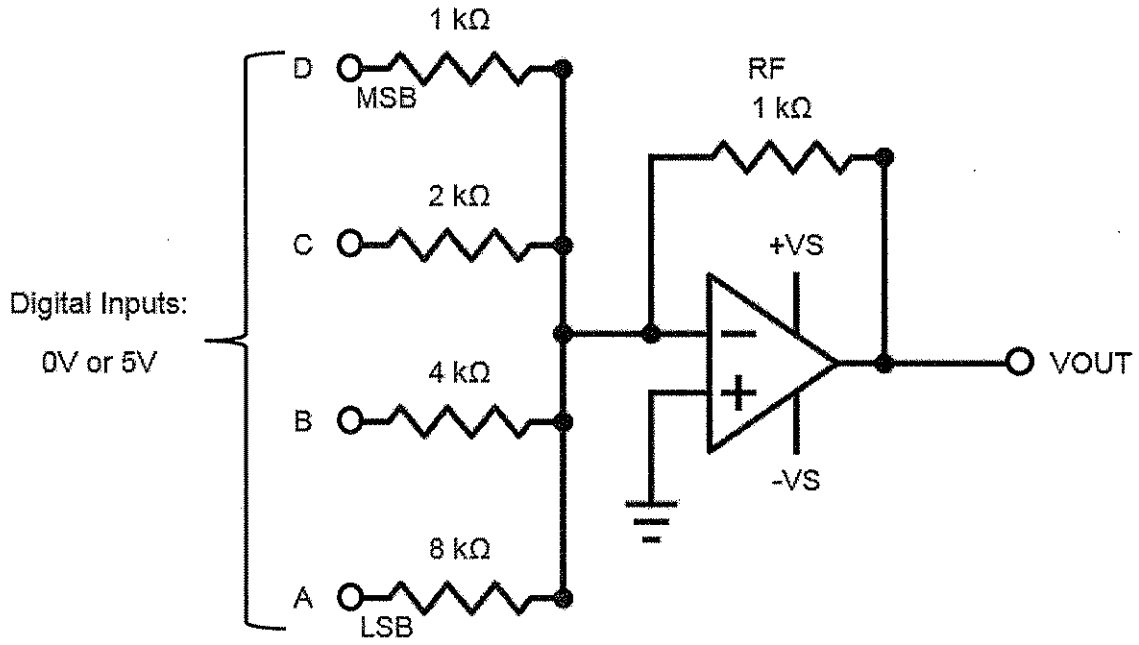


Figure 5(b)

i) Determine the weight of each input bit of Figure 5(b).

(4 marks)

ii) Change R_F to 125Ω and determine the full-scale output.

(3 marks)

(c) Figure Q5(c) has three inputs (A, B, C) and two outputs (Y, Z).
Table Q5c(i) shows a portion of quadruple 2-input AND gates datasheet.
Table Q5c(ii) shows a portion of quadruple 2-input OR gates datasheet.
Table Q5c(iii) shows a portion of quadruple 2-input XOR gates datasheet.

i) Using the datasheets given, determine the maximum propagation delay time. Show all working clearly.

(6 marks)

ii) What is minimum operating frequency that can be applied to this circuit without affecting the functionality of the circuit?

(2 marks)

iii) State the function of Figure Q5(c) circuit.

(1 mark)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	C_L = 15 pF R_L = 400Ω		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			19	ns

Table Q5c(i) AND gate

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	11	4	15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	11	4	15	ns

Table Q5c(ii) OR gate

Symbol	Parameter	Conditions	C_L = 15 pF, R_L = 400Ω		Units
			Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Other Input LOW		23	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			17	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Other Input HIGH		30	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			22	ns

Table Q5c(iii) XOR gate

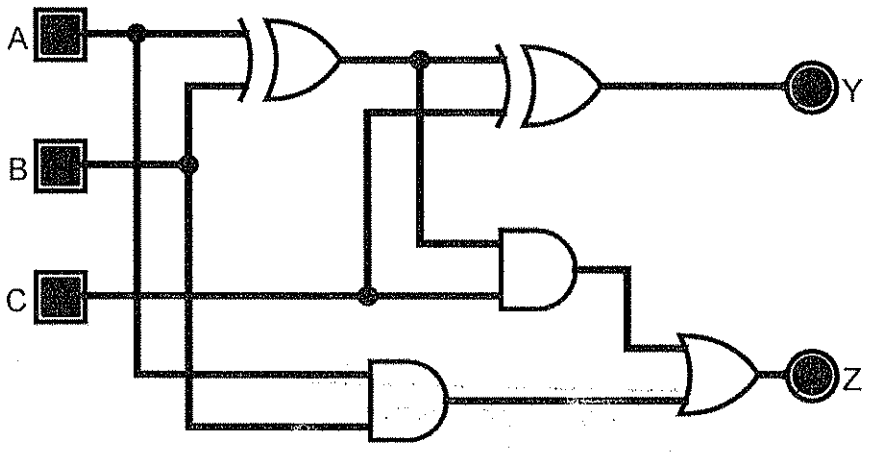


Figure 5(c)

Question 6

(a) Implement $F(X,Y,Z) = \Sigma(1,2,6,7)$ using the following in the simplest form:

i) SN7400N (2-input NAND gate) only.

(4 marks)

ii) SN74157N (2-to-1 Multiplexer) with X as select line and other logic gate(s).

(4 marks)

iii) SN74LS138N (3-to-8 Decoder) and other logic gate(s).

Inputs				Outputs							
E	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	X	X	X	1	1	1	1	1	1	1	1
1	0	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	0	1	1	1	1	1	1
1	0	1	0	1	1	0	1	1	1	1	1
1	0	1	1	1	1	1	0	1	1	1	1
1	1	0	0	1	1	1	1	0	1	1	1
1	1	0	1	1	1	1	1	1	0	1	1
1	1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	0

Table Q6(a)(iii) 3-to-8 active-low Decoder truth table

(4 marks)

(b) Figure 6(b) represents a multiplier circuit that takes two-bit binary numbers X_1X_0 and Y_1Y_0 and produces an output binary number $Z_3Z_2Z_1Z_0$ that is equal to the arithmetic product of the two input numbers.

Design the logic circuit for the multiplier. Show all working clearly. Hint: The logic circuit will have four inputs and four outputs.

i) Write down the truth table for the circuit.

(3 marks)

ii) Simplify the Boolean expression using Karnaugh map or Boolean algebra.

(4 marks)

iii) Implement the logic circuit of the simplest Boolean expression using only SN7400N (2-input NAND gate).

(6 marks)

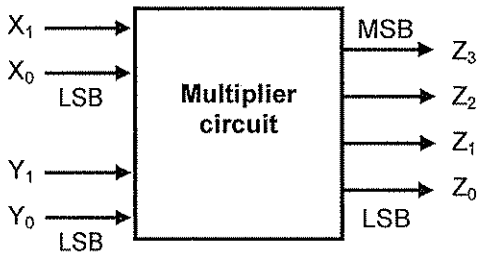


Figure 6(b)

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