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FINAL
Examination Paper

(COVER PAGE)

Session	:	**AUGUST 2014**
Programmes	:	Diploma in Electrical and Electronic Engineering (DEEI)
Course	:	**CIRCUIT THEORY AND ELECTRONIC DEVICES (EEE1105)**
Date of Examination	:	December 12, 2014 (Friday)
Time	:	5.00pm – 7.00pm Reading Time: Nil
Duration	:	2 Hours
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Students are not allowed to remove this question paper from the examination venue.

Materials permitted : Non-programmable scientific calculator

Materials provided: **Worksheet for Q3(b)**

Examiner(s)	:	**Mr. Chan Tse Wei**
Moderator	:	**Dr. Cheah Kean Seng**

This paper consists of 9 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)

EEE1105 : CIRCUIT THEORY AND ELECTRONIC DEVICES
FINAL EXAMINATION : AUGUST 2014 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks. The marks allocated to each sub-question are shown in square brackets at the right-hand margin.

Question 1

a. Calculate the value and direction of the current flowing through the 40Ω resistor in the circuit shown in Figure-Q1 using Thevenin's Theorem. [8]

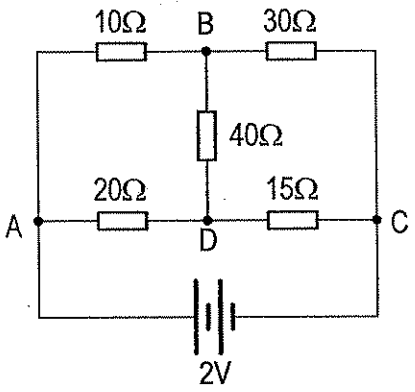

Figure-Q1

b. Justify your answer in part (a) using Nodal Analysis. [8]

c. Base on the effort in part (a) and part (b), comment on the advantage of Nodal Analysis as compared to Thevenin's Theorem. [4]

d. Do Nodal Analysis and Thevenin's Theorem provide a direct approach to determine the total current drawn from the 2V supply voltage in Figure-Q1(a)? Explain your answer. [5]

Question 2

a. Figure-Q2(a) shows a sinusoidal current signal superimposed with a DC current component. Calculate,

i. The DC current component of the signal. [2]

ii. The frequency of the signal. [2]

iii. The RMS value of the signal. Show the derivation of the formula used in the calculation. [6]

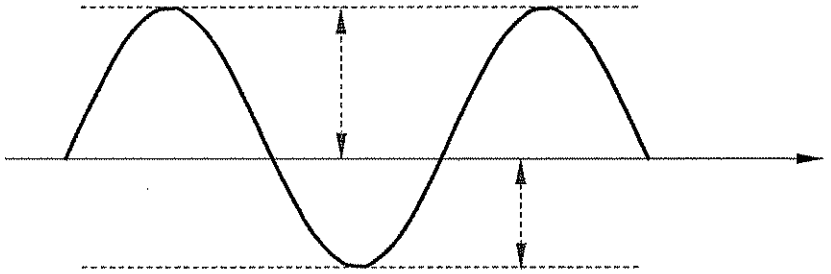

Figure-Q2(a)

b. A 15Ω resistor is connected in series with a coil of inductance 0.08H. The combined circuit is connected to a 240V, 50Hz supply. Calculate,

i. The reactance of the coil. [2]

ii. The impedance the circuit in polar form. [2]

iii. The current flowing in the circuit in polar form. [2]

iv. The power factor of the circuit. [2]

v. The active power absorbed by the circuit. [2]

c. Convert the T-network in Figure-Q2(c) to its equivalent π-network. [5]

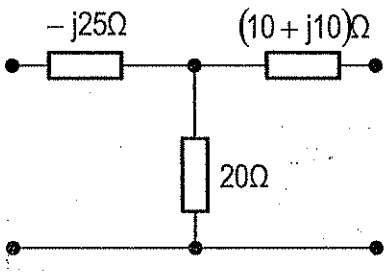

Figure-Q2(c)

Question 3

a. The forward bias IV curve of a diode is as shown in Figure-Q3(a).

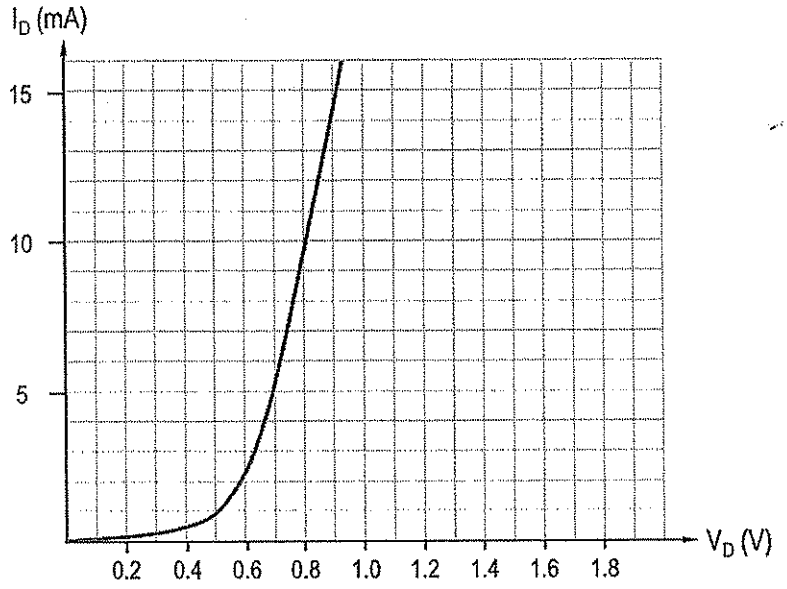

Figure-Q3(a)

i. Approximate the knee voltage of the diode. [2]

ii. Calculate the diode's static resistance if 0.8V is applied across the diode. [3]

b. Figure-Q3(b) shows a simple diode circuit in which the diode has an IV characteristic similar to the one shown in Figure-Q3(a).

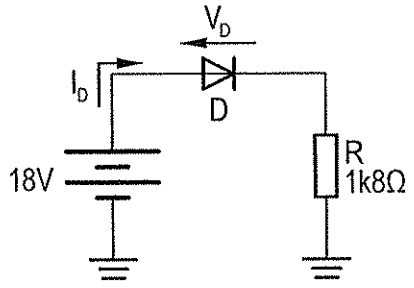

Figure-Q3(b)

i. Write the circuit current expression, I_D in terms of V_D. [2]

ii. Draw the DC load line of the circuit in Figure-Q3(b) on the accompanying worksheet. [4]

iii. Hence, determine the quiescent current and voltage of the diode. [2]

iv. If an AC voltage component of 0.1V peak is superimposed across the quiescent diode voltage in Figure-Q3(b), sketch the voltage waveform across resistor R, showing clearly its maximum and minimum voltage. [6]

c. i. Figure-Q3(c) shows a piecewise model of the diode in part (a). Determine the value of V_{D0} and r_d. [4]

ii. Base on the piecewise model in Figure-Q3(c), what is the diode current if 0.5V is applied across the diode? [2]

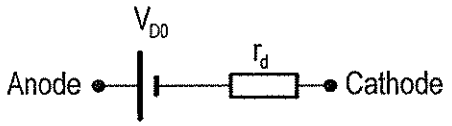

Figure-Q3(c)

Question 4

a. Complete Table-Q4(a) by stating if the corresponding junctions should be forward or reverse biased for each of the listed BJT operating mode. Copy the table into your answer booklet. [6]

Mode of Operation	B-E Junction Biasing Condition	B-C Junction Biasing Condition
ON switch		
OFF switch		
Amplifying		

Table-Q4(a)

b. A transistor with $\alpha = 0.98$ is biased so that $I_{B_Q} = 0.1\text{mA}$. Calculate,

i. I_{C_Q} [4]

ii. I_{E_Q} [2]

c. Figure-Q4(b) shows a common BJT biasing circuit.

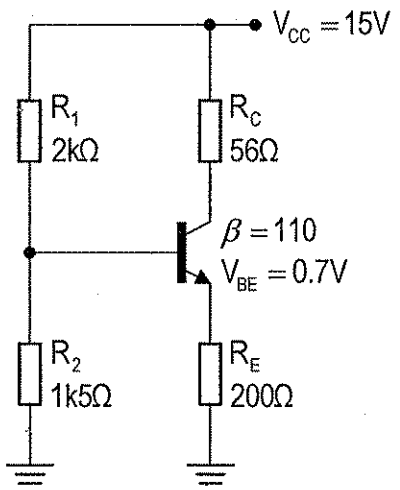

Figure-Q4(b)

i. State the name of the biasing circuit. [2]

ii. State the main advantage of the biasing circuit. [2]

iii. Calculate the quiescent emitter current, I_{E_Q} of the circuit with the assumption that $I_{B_Q} \neq 0$ A. [6]

iv. By taking into consideration that $I_{C_Q} \neq I_{E_Q}$, calculate V_{CE_Q}. [3]

Question 5

a. i. Draw the respective symbols for the n-channel E-MOSFET and n-channel D-MOSFET. [4]

ii. State ONE difference between E-MOSFET and D-MOSFET when the gates of both transistors are left unconnected. [2]

b. An n-channel JFET has the following characteristics: $I_{DSS} = 10mA$, $V_{GS_{off}} = -7V$

i. Explain the parameters I_{DSS} and $V_{GS_{off}}$ of a JFET. [4]

ii. If –3V is applied across the gate-source terminals of the n-channel JFET, calculate the expected drain current flowing through the transistor? [3]

iii. If 6mA is desired for the drain current, calculate the voltage that should be applied across the gate-source terminals. [3]

iv. If the n-channel JFET is biased by the circuit shown in Figure-Q5(b), determine the value of V_{DS_Q}. [9]

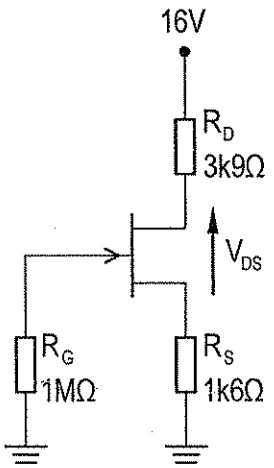

Figure-Q5(b)

Question 6

a. For the network shown in Figure-Q6(a), the transistor has the following characteristics: $V_{GS_{off}} = -8\text{V}$ and $I_{DSS} = 8\text{mA}$.

Calculate,

i. I_{D_Q} [6]

ii. V_{GS_Q} [2]

iii. V_{S_Q} [2]

iv. V_{DS_Q} [3]

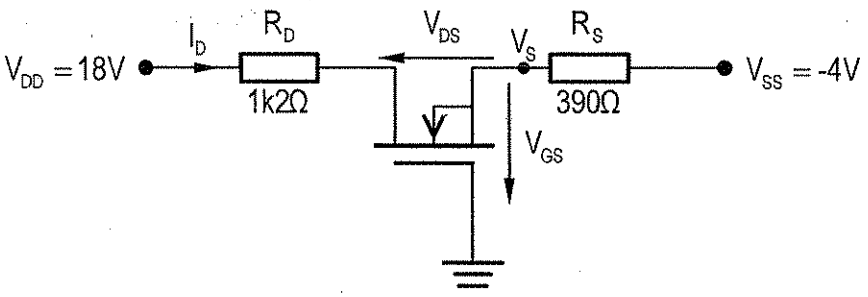

Figure-Q6(a)

b. For the network shown in Figure-Q6(b), the transistor has the following characteristics: $V_{BE_Q} = 0.65\text{V}$ and $\beta = 120$.

Calculate,

i. I_{B_Q} [4]

ii. I_{C_Q} [2]

iii. V_{CE_Q} [3]

iv. V_{C_Q} [1]

v. The current flowing through resistor R_E if resistor R_C is open-circuited. [2]

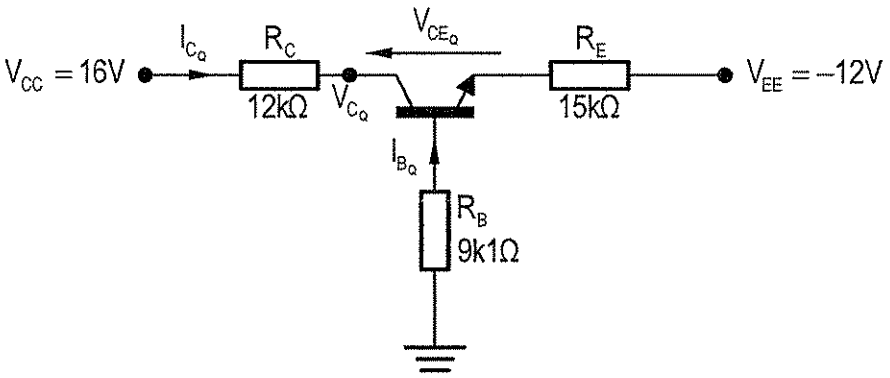

Figure-Q6(b)

– THE END –

Worksheet for Question 3(b)