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FINAL
Examination Paper

(COVER PAGE)

Session	:	**AUGUST 2014**
Programmes	:	Diploma in Electrical and Electronic Engineering (DEEI)
Course	:	**ELECTRONIC DEVICES AND CIRCUIT THEORY 2 (EEE1103)**
Date of Examination	:	December 13, 2014 (Saturday)
Time	:	5.00pm – 7.00pm Reading Time: Nil
Duration	:	2 Hours
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Students are not allowed to remove this question paper from the examination venue.

Materials permitted :

Non-programmable scientific calculator

Materials provided:

NIL

Examiner(s)	:	**Mr. Chan Tse Wei**
Moderator	:	**Dr. Ooi Beng Lee**

This paper consists of 8 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)

EEE1103 : ELECTRONIC DEVICES AND CIRCUIT THEORY 2
FINAL EXAMINATION : AUGUST 2014 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks. The marks allocated to each sub-question are shown in square brackets at the right-hand margin.

Question 1

a. Figure-Q1(a)(i) and (ii) shows two class-A power amplifiers.

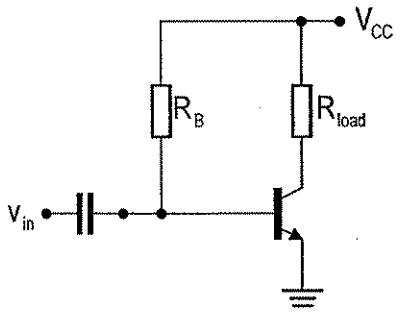

Figure-Q1(a)(i)

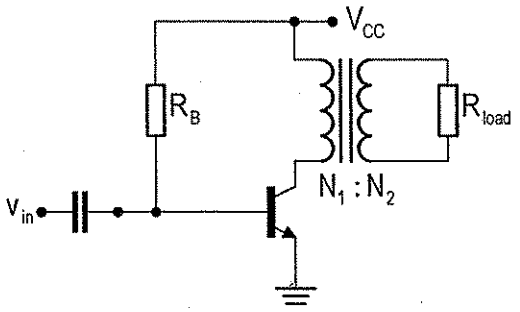

Figure-Q1(a)(ii)

i. Which power amplifier in Figure-Q1(a) has a higher power efficiency? [2]

ii. Qualitatively justify your answer in part (a)(i). [4]

iii. Sketch the respective AC load lines for each power amplifier in Figure-Q1(a). Assume that the transformer in Figure-Q1(a)(ii) has negligible wiring resistance. [6]

b. The peak voltage and current swings of a power amplifier circuit are shown in Figure Q1(b). Calculate the output power and the power efficiency of the circuit. [6]

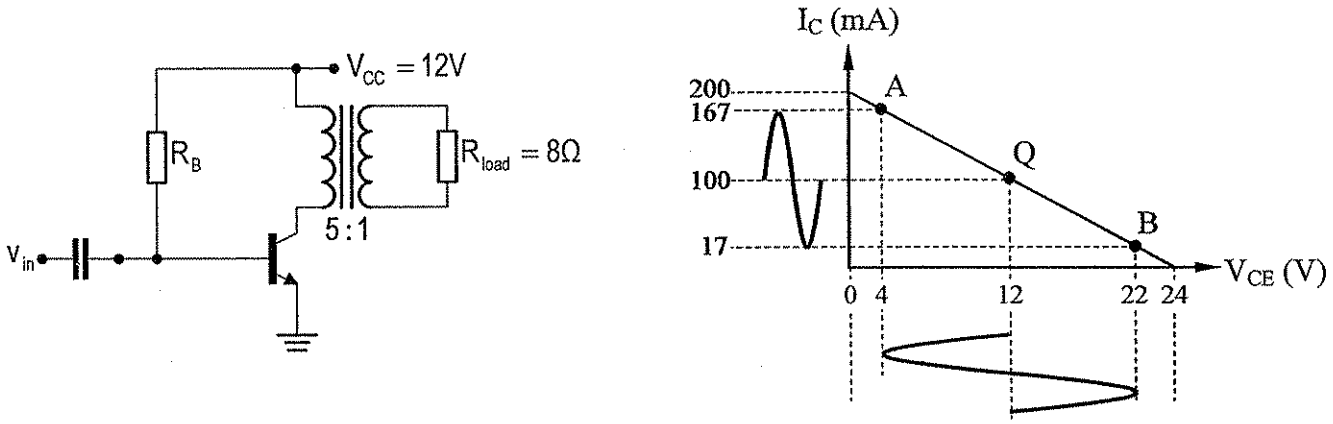

Figure-Q1(b)

c. Illustrate in detail the power dissipation in a transistor using appropriate thermal analogy. [7]

Question 2

a. i. Sketch the generic frequency response curve of a transistor based voltage amplifier, clearly showing its cutoff frequencies. [5]

ii. If the amplifier system is configured as an audio amplifier system, what should be the theoretical cutoff frequencies of the system? [2]

b. Figure Q2(b) shows a FET based amplifier circuit. The lower cutoff frequency of the amplifier circuit is to be set at 240Hz±1%.

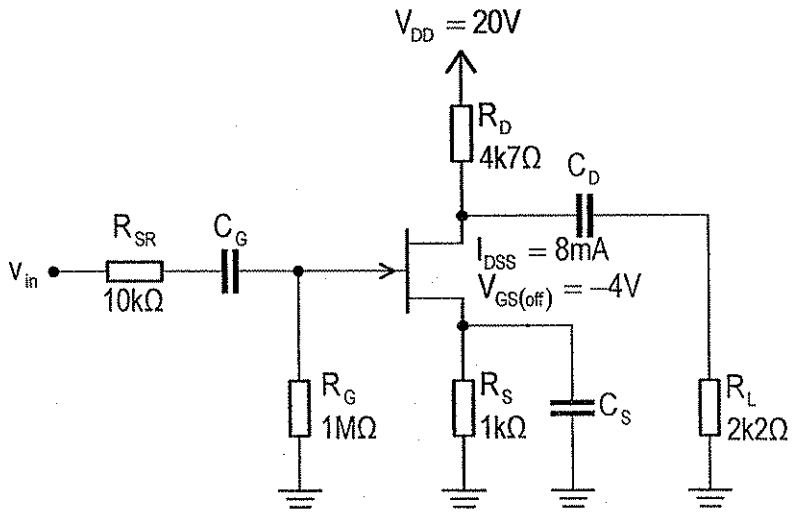

Figure-Q2(b)

i. Draw the DC equivalent circuit for the amplifier in Figure-Q2(b). [2]

ii. Hence, determine the transconductance (g_m) of the FET transistor at its operating point. [4]

iii. With the transconductance obtained in part (b)(ii), draw the AC equivalent circuit for the amplifier in Figure-Q2(b). [3]

iv. If the given cutoff frequency for the amplifier circuit is to be solely contributed by capacitor C_S in Figure-Q2(b), calculate the appropriate value for C_S. [5]

v. If capacitors C_G and C_D in Figure-Q2(b) are to contribute a cutoff frequency which is a decade lower than 240Hz, calculate the appropriate value for these capacitors. [4]

Question 3

a. Figure-Q3(a) shows an inverting amplifier circuit.

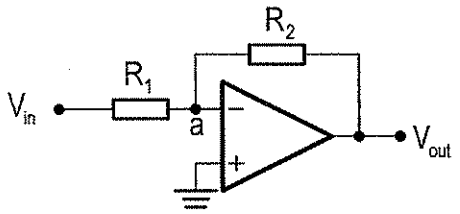

Figure-Q3(a)

i. State the voltage at node-*a* in Figure-Q3(a). Why is the voltage as such? [2]

ii. What is the voltage gain of the circuit in Figure-Q3(a) if $R_1 = 2.4\text{k}\Omega$ and $R_2 = 36\text{k}\Omega$? [2]

iii. State two possibilities that can cause the output voltage in Figure-Q3(a) to saturate. For each given possibility, state the reason. [4]

iv. If V_{in} and the ground point connections in Figure-Q3(a) is interchanged, what is the voltage gain of the circuit? [4]

b. Figure-Q3(b)(i) shows a non-inverting Schmitt Trigger Comparator and Figure-Q3(b)(ii) shows the voltage transfer curve of the comparator to be implemented. The op-amp used in the comparator circuit is assumed ideal

i. Identify the upper and lower threshold points (UTP and LTP) of the design. [2]

ii. Show that the node voltage at the non-inverting input of the op-amp can be expressed as, [3]

$$V^+ = \frac{R_2 V_{in} \pm 12 R_1}{R_1 + R_2}$$

iii. Show that, to implement the voltage transfer curve in Figure-Q3(b)(ii), $R_2 = 24R_1$. [6]

iv. Determine the required value of V_{ref} in Figure-Q3(b)(i) if $R_1 = 1\text{k}\Omega$. [2]

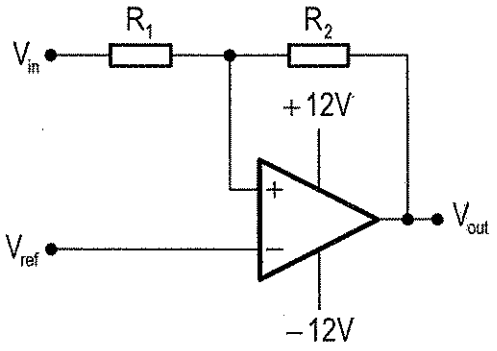

Figure-Q3(b)(i)

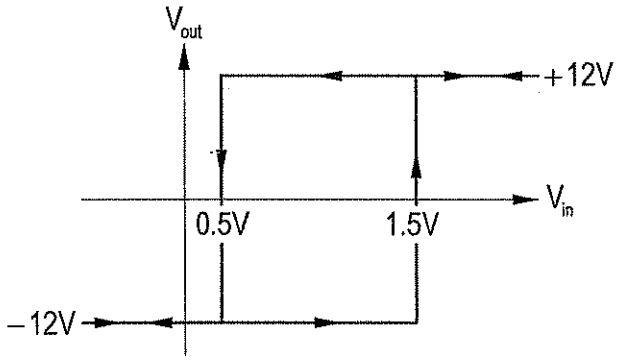

Figure-Q3(b)(ii)

Question 4

a. i. Explain how a low pass active filter and a high pass active filter may be utilized to form a band pass filter. [2]

ii. State one design constrain of the band pass filter implemented in part (a)(i). [2]

iii. State the general transfer function of the band pass filter implemented in part (a)(i) if only 1st order active filters are utilized. [4]

iv. Draw the circuit diagram of the band pass filter implemented in part (a)(iii). [4]

b. Figure-Q4(b) shows a second order active filter circuit that is commonly called as *universal filter*.

i. Identify all the virtual ground points in the circuit and hence derive the voltage expression at node-a in terms of V_{out2}. [2]

ii. By writing nodal equations at relevant virtual ground points, derive the voltage expressions for V_{out1}, V_{out2} and V_{out3} in terms of V_{in}, R and C. [8]

iii. Hence, determine the three respective output functions of the filter circuit. [3]

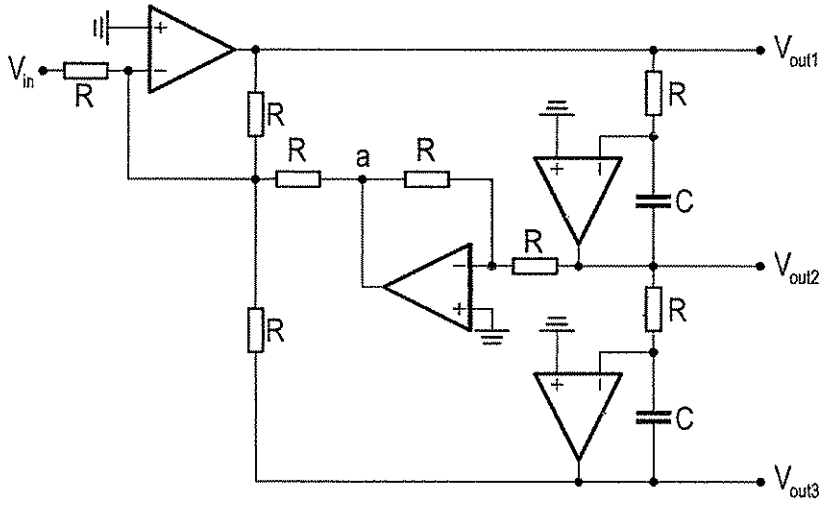

Figure-Q4(b)

Question 5

a. i. Draw a schematic diagram of a square wave generator using only ONE (1) operational amplifier and some passive components. [3]

ii. State the oscillation frequency (f_o) expression of the generator in terms of the circuit elements drawn in part (a)(i). [2]

iii. Briefly elaborate the circuit operation to produce the desired square wave. [4]

iv. Suggest suitable circuit component values to produce an oscillation frequency of 10 kHz. [3]

b. Figure-Q5(b) shows a block diagram of a harmonic oscillator.

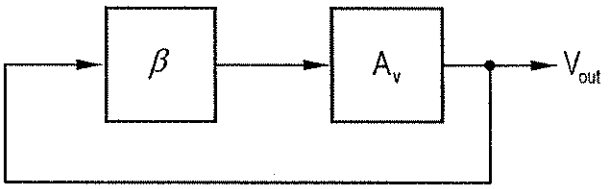

Figure-Q5(b)

i. If $\beta = -0.02$, what type of amplifier circuit should be chosen to implement A_v and what is the amplifier gain to sustain output oscillation? [4]

ii. If $|A_v| = 30$ in Figure-Q5(b) due to component variations, how does it affect the output of [3]

the oscillator circuit?

iii. State the two most probable root causes if the output oscillation saturates. [4]

iv. State the two oscillator circuits that is implemented based on the block diagram in Figure-Q5(b). [2]

Question 6

a. A dc voltage supply provides 60 V when the output is unloaded. When connected to full load, the output drops to 56 V. Calculate the value of the voltage regulation with reference to the full-load voltage in percentage. [4]

Figure-Q6(b) shows a pin-out diagram of an IC voltage regulator.

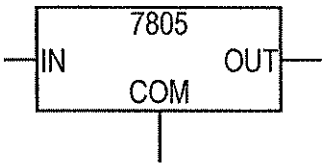

Figure-Q6(b)

i. Under normal operating condition, what is the expected output voltage of the voltage regulator in Figure-Q6(b)? [2]

ii. The voltage regulator in Figure-Q6(b) has a minimum drop out voltage of 2V, what does that mean? [2]

iii. Draw the schematic diagram of a voltage regulator utilizing the one in Figure-Q6(b) so that a 5.7V regulated output voltage is obtained. [2]

c. The nominal maximum output current for the IC voltage regulator in Figure-Q6(b) is approximately 1.0A. In order to support a load that draws more than 1.0A from the voltage regulator, the circuit in Figure-Q6(c) can be implemented. Explain the significant operation of the circuit in Figure-Q6(c). [5]

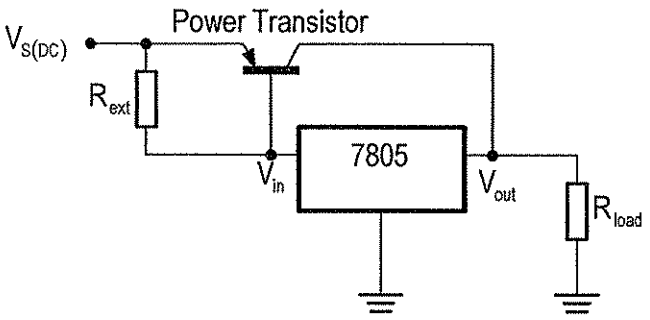

Figure-Q6(c)

d. Figure-Q6(d) shows an example of a voltage regulator circuit.

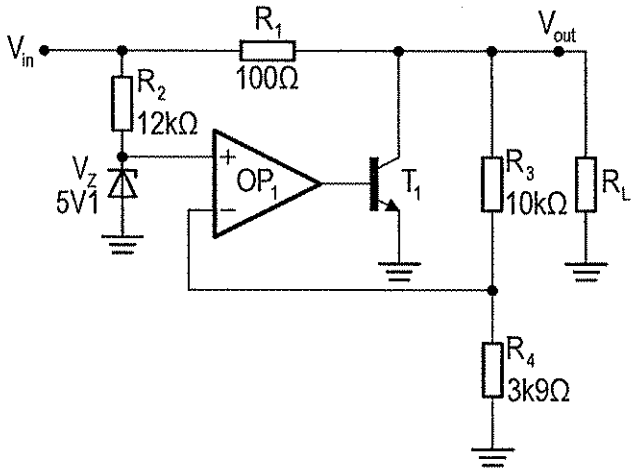

Figure-Q6(d)

i. Assume that the output voltage of the regulator circuit in Figure-Q6(d) is perfectly regulated, determine the change in collector current if the input voltage changes by 1V. [3]

ii. Determine the output voltage value that is being regulated in Figure-Q6(d). [3]

iii. In Figure-Q6(d), if V_{in} = 30V and the power rating of resistor R_1 is 1W, determine the lowest value for load resistor R_L that can be connected across the voltage regulator output. [4]

– THE END –