

**FINAL
ALTERNATIVE ASSESSMENT**

(COVER PAGE)

Session : April 2022

Programme : Diploma in Electrical and Electronic Engineering (DEEI)

Course : EGE1101: Introduction to Programmable Logic Controller

Date of Examination : 02 August 2022 (Tuesday)

Time : 12.00pm-03.00pm Reading Time : Nil

Duration : 3 hours

Special Instructions :

This paper consists of **FOUR (4)** questions. Answer **ALL** questions.

Material permitted : Non-Programmable Scientific Calculator

Materials provided : Nil

Examiner(s) : Steven Khoo Boo Tap

Chief Moderator : Dr Su Hsiao Wei

This paper consists of 9 printed pages, including the cover page

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EGE1101: INTRODUCTION TO PROGRAMMABLE LOGIC CONTROLLER
FINAL ALTERNATIVE ASSESSMENT: APRIL 2022 SESSION

Instructions: This paper consists of **FOUR (4)** questions. Answer **ALL** questions. All questions carry equal marks.

Question 1

- (a) All PLCs contain different amounts of Random Access Memory (RAM) and Read Only Memory (ROM) depending on the design of the Programmable Logic Controller (PLC) manufacturer.
- (i) Explain the reason why system memory is considered as the scratch pad for the PLC's operating system. (3 marks)
- (ii) Explain the reason why user program memory is required in a PLC. (3 marks)
- (b) The central processing unit (CPU) is built into single-unit fixed PLCs while modular type PLCs use a plug-in module.
- (i) Illustrate the PLC system with the PLC processor module using an appropriate block diagram. The block diagram should also include other related modules. (4 marks)
- (ii) Explain those sections inside the processor module. (3 marks)
- (c) There are many advantages that a PLC system holds over a relay control system. Explain in detail the following two advantages of a PLC system over a relay control system.
- (i) Easy to Troubleshoot (3 marks)
- (ii) Communication Capability (3 marks)

(d) Select ONE answer for each of the following sub-question and justify the reason for the selected answer.

(i) Main difference between online and offline PLC programming is:

- A. whether the programming computer has internet connectivity.
- B. whether the PLC is running or stopped.
- C. where the edited program resides.
- D. the type of program used.

(3 marks)

(ii) For a 16-bit register, which is the largest integer number a PLC counter function can reach:

- A. 32,768.
- B. 65,535.
- C. 65,536.
- D. 32,767.

(3 marks)

Question 2

(a) The methods used by user to communicate information with PLC is known as PLC programming language as shown in Figure 2(a).

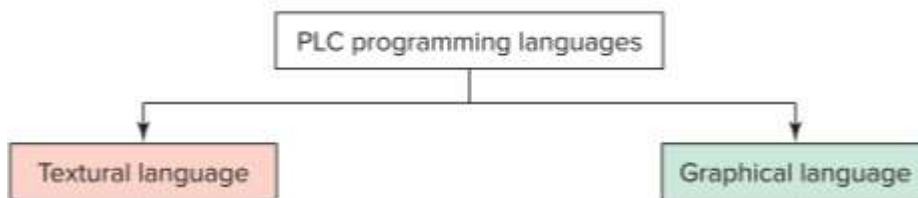


Figure 2(a)

(i) Describe all types of PLC programming languages: Graphical Languages and Textural Languages.

(5 marks)

(ii) Provide ONE (1) advantage and ONE (1) disadvantage of ladder logic diagram used as PLC language.

(3 marks)

- (b) Using KV-N14DT Keyence PLC, produce a KV programming script for the ladder logic diagram shown in Figure 2(b).

Hint: The length of the script should be as short as possible.



Figure 2(b)

(5 marks)

- (c) A continuous filling operation system as shown in Figure 2(c) requires boxes to be moved on a conveyor to be automatically positioned and filled.

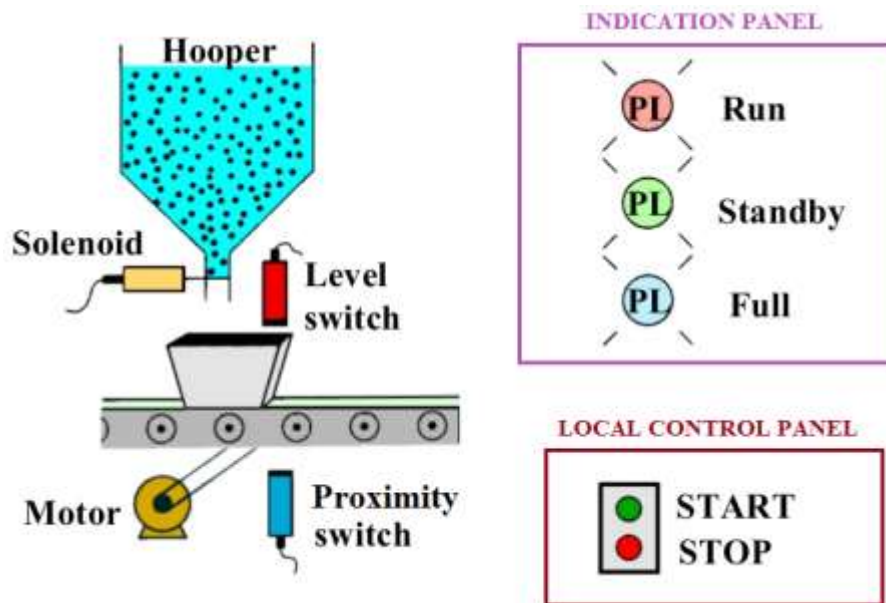


Figure 2(c)

Conditions:

- The purpose of the solenoid is to control the product filing from the hooper. Solenoid will be activated after the box positioned (proximity switch activation) and again deactivated after the level switch activated (level full).
- Indication panel will be indicated using Pilot light with 3 colours to display the batch status.
- The I/O assignment of the system is given in Table 2(c).

Table 2(c)

Input	Device	Output	Device
R000	Stop	R500	Motor
R001	Start	R501	Solenoid
R002	Level Switch Sensor	R502	Run (Red)
R003	Proximity Switch Sensor	R503	Stand By (Green)
		R504	Full (Blue)

Assume those sensors, pushbuttons and output light can be operated with 24 VDC supply. The KV-N14DT PLC is being supplied with MS2-H50 switching power supply unit.

- (i) Construct a relay schematic diagram using hardwired relay method with the aid of an industrial relay. Label all the components. (4 marks)

- (ii) Construct a ladder diagram using KV-N14DT PLC method with proper labelling. Comment on the type of contact the switch sensors should be used for this application. (8 marks)

Question 3

- (a) Suggest TWO (2) different timers that can be used to produce 8.765 seconds delay. Show and explain with the aid of ladder diagram each type of timers used to produce the required delay. (6 marks)

- (b) Given the following mnemonics list of a PLC as shown in Table 3(b). Change the mnemonics list to ladder logic diagram and explain the function of the program. Also, explain the purpose of MR100 relay.

Table 3(b)

Mnemonics	
LD	R001
AND	MR100
OUT	R501
LD	MR100
C	#1 #2 R001
LD	C1
OUT	R502
LD	R000
TMR	#0 #20
LD	T0

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OUT R500
END
ENDH
    
```

(7 marks)

- (c) Justify how the processor handles the arrangement of series instructions of a rung programmed for a given ladder logic diagram as shown in Figure 3(c). Use the given figure to aid your explanation. Indicate the most likely to be False contact(s).



Figure 3(c)

(6 marks)

- (d) An equivalent logic gate circuit of a PLC control system is shown in Figure 3(d). Construct the ladder logic diagram for the PLC control system shown in Figure 3(d). Also, provide the Boolean expression of output, Y. Input A (R011), input B (R012), input C (R013), input D (R014) and input E (R015) are represented by Pushbuttons and output Y (R500) is represented by Pilot Light.

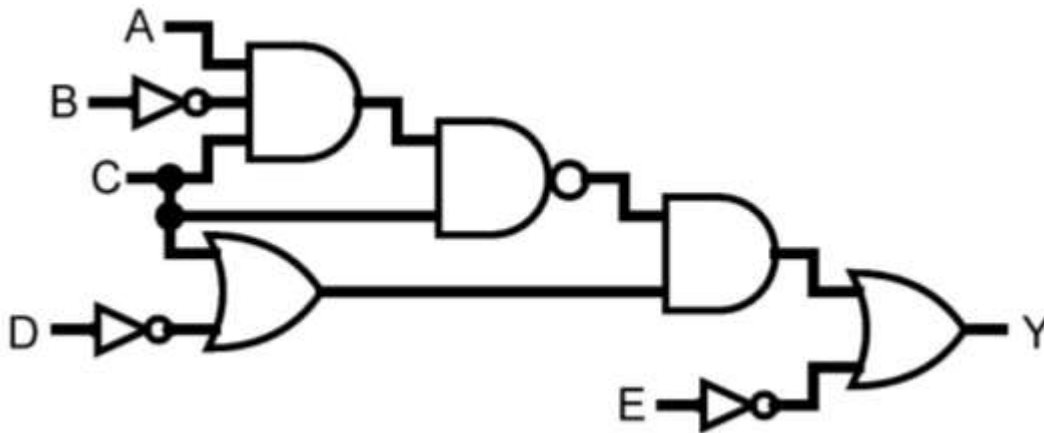


Figure 3(d)

(6 marks)

Question 4

(a) Figure 4(a)(ii) shows a 240VAC output module of a PLC. Show the complete wiring connection of controlling the level of water in a storage tank as shown in Figure 4(a)(i) with the following output connection information:

- Motor pump connects to Output 1 (OUT 1)
- Pump running light connects to Output 3 (OUT 3)
- Low level light connects to Output 5 (OUT 5)
- High level light connects to Output 7 (OUT 7).

Assume the status indicating lights as follows:

- Water pump running light (green).
- Low water level status light (red).
- High water level status light (yellow).

Assume all the inputs buttons and sensors are already connected to the input module. Use appropriate symbols for the devices.

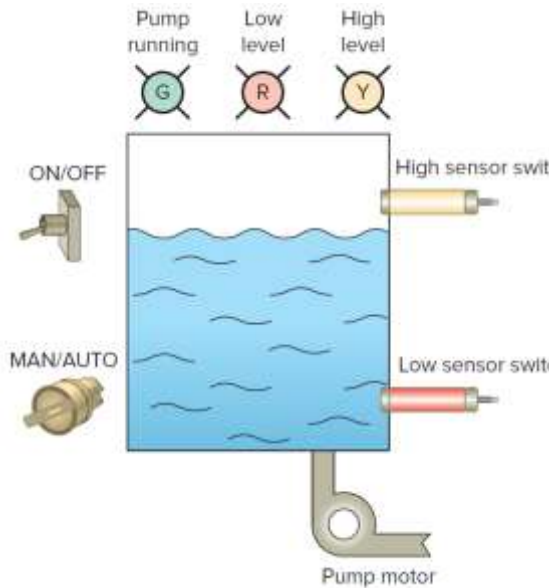


Figure 4(a)(i)

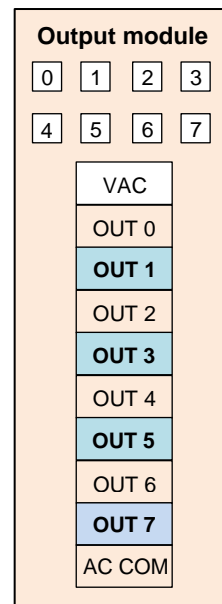


Figure 4(a)(ii)

(6 marks)

- (b) Using a portion of Keyence EZ-8M proximity sensor datasheet as shown in Table 4(b), determine:

Table 4(b)

Model		EZ-8M
Type		Shielded, Threaded
Detecting distance		1.5mm ± 10%
Standard target (iron, t=1mm)		10 × 10 mm
Hysteresis		10% max. of detecting distance
Response frequency		800 Hz
Operation mode		N.O./N.C.
Temperature characteristics		±10% max. of detecting distance at 23°C, within -25 to +70°C
Control output		NPN open collector 100 mA max. (40 V max.), Residual voltage: 1 V max.
Rating	Power voltage	12 to 24 VDC ±10%, Ripple (P-P) 10% or less
	Current consumption	13 mA or less
Environmental resistance	Ambient temperature	-25 to +80 °C (No freezing)
	Relative humidity	35 to 95 % RH (No condensation)
	Vibration resistance	10 to 55 Hz, Double amplitude 1.5 mm, 2 hours in each of the X, Y, and Z directions
	Shock resistance	500 m/s ² , 3 times in each of the X, Y, and Z directions
Weight		Approx. 50 g

- (i) The detecting distance range. (3 marks)
- (ii) The maximum power consumption of this sensor. (4 marks)
- (c) A control system uses two start pushbuttons and two stop pushbuttons to control a motor. Only when both start pushbuttons are depressed, the motor runs. By the use of a seal-in contact, it continues to run when both start pushbuttons are released. Either stop pushbutton stops the motor when it is depressed.
- Produce the ladder logic diagram of the control system and its equivalent logic gate circuit. Use label R101 and R102 for start buttons, label R201 and R202 for stop buttons and label R900 for motor in the equivalent logic gate circuit. (8 marks)

- (d) Construct an equivalent logic gate circuit for the ladder logic diagram shown in Figure 4(d). Provide minimum gates in the equivalent logic gate circuit.



Figure 4(d)

(4 marks)

~THE END~