

**FINAL  
ALTERNATIVE ASSESSMENT**

(COVER PAGE)

Session : April 2022

Programme : Diploma in Electrical and Electronic Engineering (DEEI)

Course : EEE2101: Introduction to Digital Electronics

Date of Examination : 05 August 2022(Friday)

Time : 12.00pm-03.00pm Reading Time : Nil

Duration : 3 hours

**Special Instructions :**

This paper consists of **FOUR (4)** questions. Answer **ALL** questions.

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Material permitted : Non-Programmable Scientific Calculator

Materials provided : Nil

Examiner(s) : Steven Khoo Boo Tap

Chief Moderator : Hii Ing Hui

*This paper consists of 8 printed pages, including the cover page*

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)  
 EEE2101: INTRODUCTION TO DIGITAL ELECTRONICS  
 FINAL ALTERNATIVE ASSESSMENT: APRIL 2022 SESSION

Instructions: This paper consists of **FOUR (4)** questions. Answer **ALL** questions. All questions carry equal marks.

**Question 1**

(a) Present the following Boolean expressions to the stated simplest form, using the specified method:

(i)  $F_1(W, X, Y, Z) = \prod(0,2,4,6,8,10,13,15)$   
 Simplest Form: Any type of gate(s) implementation deemed appropriate.  
 Method: Karnaugh Map and/or Boolean Algebra. (5 marks)

(ii)  $F_2(R, S, T, U) = \sum m(0,1,2,3,5,6,7,8) + d(10,11,12,13,14,15)$   
 Simplest Form: Any type of gate(s) implementation deemed appropriate.  
 Method: Karnaugh Map and/or Boolean Algebra. (5 marks)

(b) Produce the Boolean expression for Z in Figure 1(b) and show the Boolean expression using 4-input NAND gate representation only. State the number of 7420 IC required to implement the Boolean expression. Show all workings clearly.

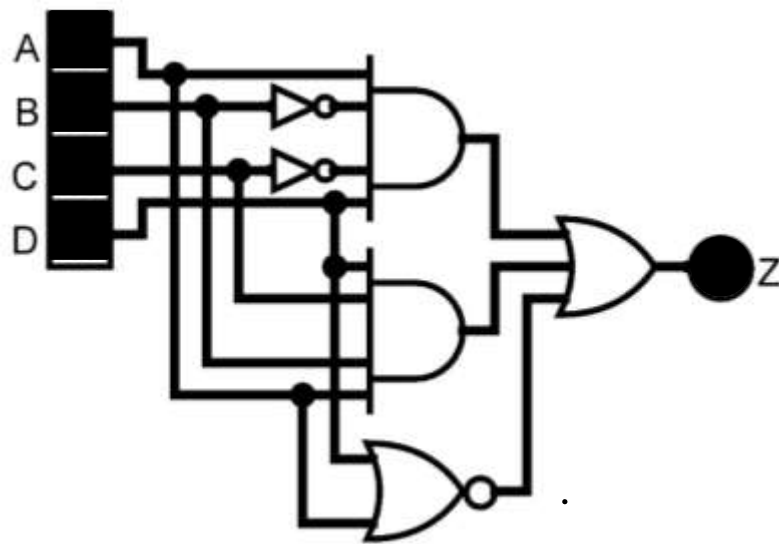


Figure 1(b)

(10 marks)

- (c) Solve the numbering system transformation of  $[127.65_8 - 18.28_{16}]$  to its BCD equivalent with full BCD points accuracy. Show all workings clearly. (5 marks)

**Question 2**

- (a) A NOR SR latch is driven by a 2-bit binary counter with outputs designated  $B_1B_0$  ( $B_1$  is the MSB) through a combinational logic circuit. Output  $B_1$  is ANDed with  $(B_1 \oplus B_0)$  and drives the R input of the SR latch.  $B_0$  is also ANDed with  $(B_1 \oplus B_0)$  and drives the S input.

- (i) Sketch the logic circuit showing the inputs,  $B_1$  &  $B_0$  and output,  $Q$  of the NOR SR latch with detail labelling. (4 marks)

- (ii) Construct a table to record the output,  $Q$  of the NOR SR latch as the counter steps through its 4 states beginning with  $B_1B_0 = 00$ . Assume the output is initially RESET. (4 marks)

- (b) Figure 2(b) shows a 4-bit synchronous counter, which is designed to perform a specific counting sequence.

Flip-flop FF3 is MSB and flip-flop FF0 is LSB. Flip-flop T<sub>3</sub> has outputs  $Q_3$  and  $\overline{Q_3}$ , flip-flop T<sub>2</sub> has outputs  $Q_2$  and  $\overline{Q_2}$ , flip-flop T<sub>1</sub> has outputs  $Q_1$  and  $\overline{Q_1}$ , and flip-flop T<sub>0</sub> has outputs  $Q_0$  and  $\overline{Q_0}$ . Assume all flip-flops are initially in 0000 (State 0) for  $Q_3Q_2Q_1Q_0$ .

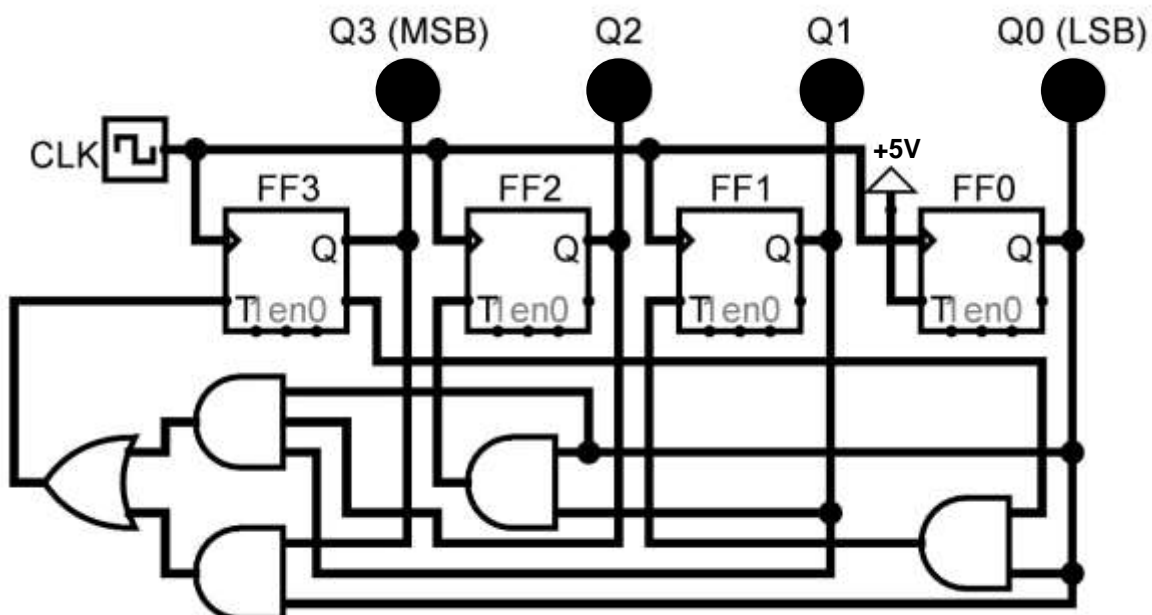


Figure 2(b)

Show all workings clearly according to the procedures listed in part (b)(i), (b)(ii), (b)(iii) and (b)(iv).

- (i) Provide all the output Boolean expressions obtained from Figure 2(b). (3 marks)
- (ii) Produce the Karnaugh maps according to the Boolean expressions obtained in part (b)(i). (6 marks)
- (iii) Build the transition table/next state table from the Karnaugh maps obtained in part (b)(ii). (4 marks)
- (iv) Sketch the state diagram(s) obtained in part (b)(iii) and comment on the states obtained. (4 marks)

**Question 3**

- (a) Solve the numbering system transformation of  $[126.01_{16} \times 1010.1_2]$  to its octal equivalent with 3 octal points accuracy. Show all workings clearly. (5 marks)
- (b) Table 3(b) shows a portion of quadruple 2-input AND gates (DM74LS08) datasheet. Compute the following parameters from this datasheet, show all working clearly:
  - (i) Power dissipation,  $P_{D(max)}$  on a DM74LS08 IC when the input conditions applied to DM74LS08 IC are as shown in the breadboard layout of Figure 3(b). (3 marks)



Figure 3(b)

- (ii) Fan-out, the number of gates from the same IC family that can be safely driven by an output under worst-case consideration.

(3 marks)

Table 3(b)

Symbol	Parameter	DM54LS08			DM74LS08			Units
		Min	Nom	Max	Min	Nom	Max	
$V_{CC}$	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$	High Level Input Voltage	2			2			V
$V_{IL}$	Low Level Input Voltage			0.7			0.8	V
$I_{OH}$	High Level Input Current			-0.4			-0.4	mA
$I_{OL}$	Low Level Input Current			4			8	mA
$T_A$	Free Air Operating Temperature	-55		125	0		70	°C

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
$V_i$	Input Clamp Voltage	$V_{CC} = \text{Min}, I_i = -18\text{mA}$			-1.5	V
$V_{OH}$	High Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max}, V_{IH} = \text{Min}$	DM54	2.5	3.4	
			DM74	2.7	3.4	
$V_{OL}$	Low Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max}, V_{IL} = \text{Max}$ $I_{OL} = 4 \text{ mA}, V_{CC} = \text{Min}$	DM54		0.25	0.4
			DM74		0.35	0.5
			DM74		0.25	0.4
$I_i$	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}, V_i = 7\text{V}$			0.1	mA
$I_{IH}$	High Level Input Current	$V_{CC} = \text{Max}, V_i = 2.7\text{V}$			20	$\mu\text{A}$
$I_{IL}$	Low Level Input Current	$V_{CC} = \text{Max}, V_i = 0.4\text{V}$			-0.36	mA
$I_{OS}$	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 3)	DM54	-20		-100
			DM74	-20		-100
$I_{CCH}$	Supply Current with Outputs High	$V_{CC} = \text{Max}$		2.4	4.8	mA
$I_{CCL}$	Supply Current with Outputs Low	$V_{CC} = \text{Max}$		4.4	8.8	mA

- (c) Explain the reason for connecting input B as shown in Figure 3(c). Provide another diagram connection that is also performing the same outcome as Figure 3(c). Assume that Figure 3(c) is a TTL gate.

(6 marks)

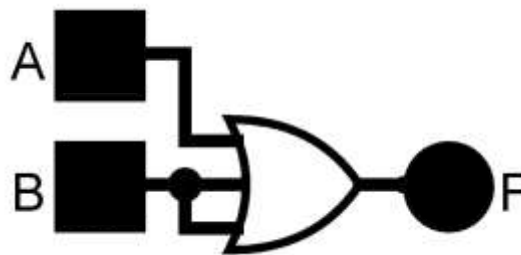


Figure 3(c)

- (d) Figure 3(d) has four inputs (A, B, C, D) and three outputs (X, Y, Z).  
 Table 3d(i) shows a portion of quadruple 3-input AND gates datasheet.  
 Table 3d(ii) shows a portion of quadruple 2-input OR gates datasheet.  
 Table 3d(iii) shows a portion of quadruple 2-input NAND gates datasheet.  
 Table 3d(iv) shows a portion of hextuple NOT gates datasheet.

(i) Using the datasheets given, determine the maximum propagation delay time. Show all the important pathways of Figure 3(d) clearly. (7 marks)

(ii) Determine the maximum operating frequency that can be applied to Figure 3(d) without affecting its functionality. Show all working clearly. (1 mark)

Table 3d(i)

Symbol (DM74LS11)	Parameter	$R_L = 2\text{ k}\Omega$				Units
		$C_L = 15\text{ pF}$		$C_L = 50\text{ pF}$		
		Min	Max	Min	Max	
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	4	13	6	18	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	3	11	5	18	ns

Table 3d(ii)

Symbol (DM74LS32)	Parameter	$R_L = 2\text{ k}\Omega$				Units
		$C_L = 15\text{ pF}$		$C_L = 50\text{ pF}$		
		Min	Max	Min	Max	
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	3	11	4	18	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	3	11	4	20	ns

Table 3d(iii)

Symbol (DM74LS00)	Parameter	$R_L = 2\text{ k}\Omega$				Units
		$C_L = 15\text{ pF}$		$C_L = 50\text{ pF}$		
		Min	Max	Min	Max	
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	3	10	4	15	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	3	10	4	15	ns

Table 3d(iv)

Symbol (DM74LS04)	Parameter	$R_L = 2\text{ k}\Omega$				Units
		$C_L = 15\text{ pF}$		$C_L = 50\text{ pF}$		
		Min	Max	Min	Max	
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	3	10	4	16	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	3	10	4	16	ns

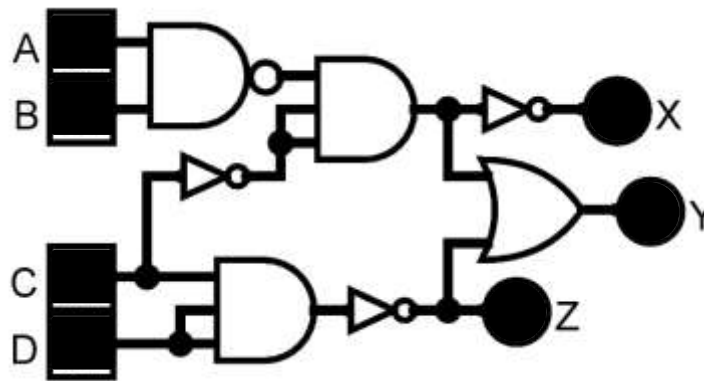


Figure 3(d)

**Question 4**

(a) Compute the 2's complement number of  $-318.125_{10}$  in signed binary numbering system. Assuming the binary system is 10-bit system with 4 binary points. Show all workings clearly.

(5 marks)

(b) Figure 4(b) shows a computer controlling the speed of a motor. The 0 to 2mA analog current from the DAC is amplified to produce motor speeds from 0 to 4000 rpm (revolutions per minute).

(i) Compute the number of bits should be used if the computer is able to produce a motor speed accuracy that is within 2 rpm of the desired speed.

(5 marks)

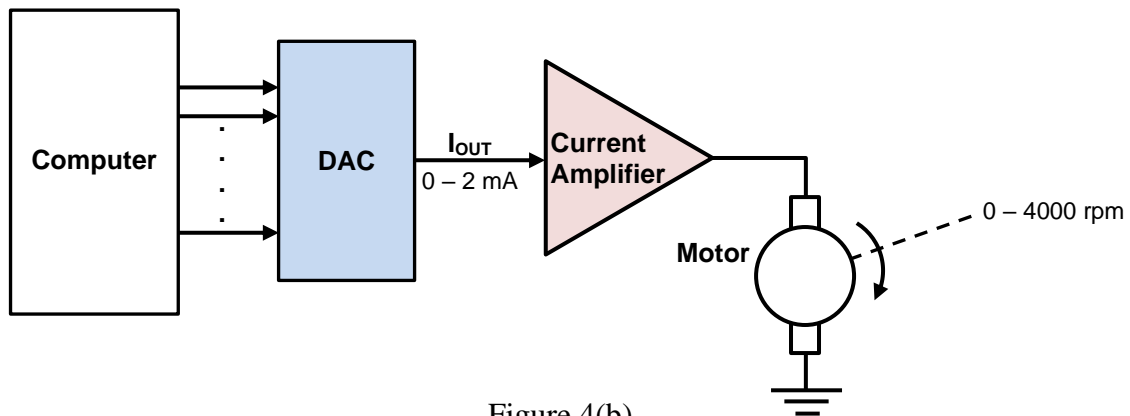


Figure 4(b)

(ii) Using the number of bits obtained in part (b)(i), compute the nearest motor speed (in rpm) achievable if 2985 rpm is required. Justify your answer.

(5 marks)

- (c) Analog to Digital Converter (ADC) is an important element in signal processing for digital conversion of sensor signal. In the case of digitizing an Illuminance signal measured by a photometric sensor with the characteristics shown in Table 4(c).

Table 4(c)

<b>Sensitivity</b>	0.5 mV/lux
<b>Measurement Range</b>	0 to 5000 lux
<b>Current Drawn</b>	10 $\mu$ A (maximum)
<b>Power Supply</b>	5 to 24 V DC
<b>Response Time</b>	Less than 1 ms
<b>Mass (with 5m of cable)</b>	140 gram
<b>Operating Environment</b>	-40°C to 70°C; 0 to 100% relative humidity

Assume the formula given is  $resolution = \frac{V_{range}}{2^n - 1}$ .

Apply an ADC according to this sensor application by computing the:

- (i) Number of bits. Justify your answer. (7 marks)
- (ii) Resolution. (3 marks)

**~THE END~**

EEE2101 (F)/ April 2022 Session/ formatted