INTI International College Penang

FINAL
ALTERNATIVE ASSESSMENT

(COVER PAGE)

Session	:	**April 2020**
Programme	:	Diploma in Electrical & Electronic Engineering (DEEI)
Course	:	**EEE2101: Introduction to Digital Electronics**
Date of Examination	:	4 August 2020 (Tuesday)
Time	:	2.00pm – 5.00pm Reading Time : Nil
Duration	:	3 Hours

Special Instructions :

This paper consists of **FOUR (4)** questions. Answer **ALL** questions. All questions carry equal marks.

Material permitted :

Nil

Materials provided :

Nil

Examiner(s)	:	**Mr Steven Khoo Boo Tap**
Chief Moderator	:	Mr Chan Tse Wei

*This paper consists of **7** printed pages, including the cover page*

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE2101: INTRODUCTION TO DIGITAL ELECTRONICS
FINAL ALTERNATIVE ASSESSMENT: APRIL 2020 SESSION

Instructions: This paper consists of **FOUR (4)** questions. Answer **ALL** questions. All questions carry equal marks.

Question 1

(a) Present the following Boolean expression using Karnaugh Map and/or Boolean algebra to the most simplified form:

(i) $F_1(X,Y,Z) = (X+Y+Z)(X+\bar{Y}+Z)(\bar{X}+Y+Z)(\bar{X}+Y+\bar{Z})$ to the simplest POS form.

(3 marks)

(ii) $F_2(A,B,C,D) = \sum m(0,1,2,5,8,9) + d(10,11,12,13,14,15)$ to the minimum gates implementation. State the number of minimum gates used.

(4 marks)

(iii) $F_3(K,L,M,N) = \prod M(1,5,7,11,12,14) \cdot \prod d(3,9)$ to the minimum gates implementation. State the number of minimum gates used.

(5 marks)

(b) Produce the simplest Boolean expressions for Y and Z in Figure 1(b) and interpret the expression to minimum 2-input NAND gate implementation only. State the minimum number of NAND gates and 7400 ICs (Integrated Circuits) used for the design. Show working clearly.

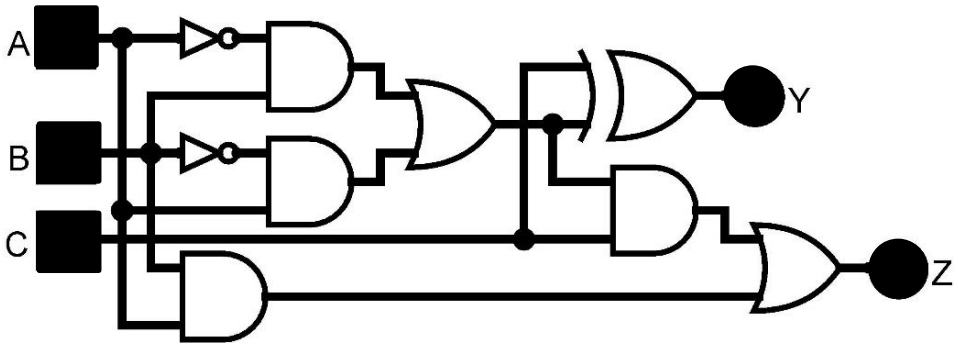

Figure 1(b)

(8 marks)

(c) Solve the numbering system transformation of [161.328125_{10} – 101.11_8 + $FA.DE_{16}$] to hexadecimal equivalent with 2 hexadecimal points accuracy. Show all workings clearly.

(5 marks)

Question 2

(a) Figure 2(a) shows the logic circuit diagram of an asynchronous counter, which uses positive edge-triggered T flip-flops with labelling of $Q_AQ_BQ_C$ where Q_C is MSB and Q_A is LSB.

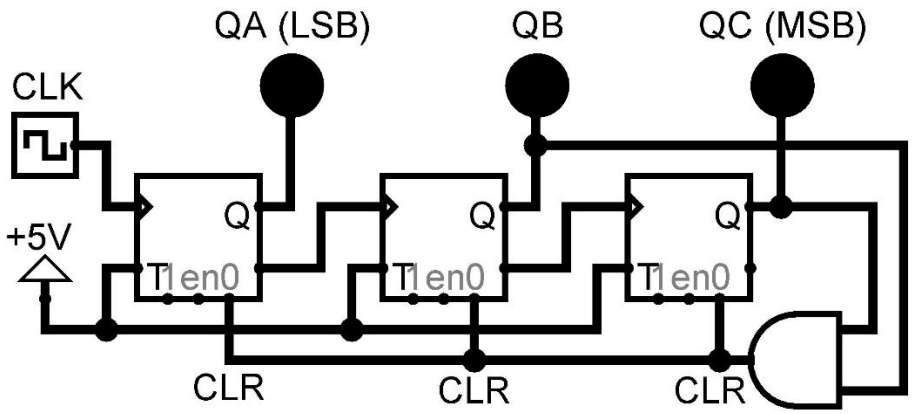

Figure 2(a)

(i) Verify the counter operation whether the logic circuit of Figure 2(a) is working as an up counter or down counter. Also, state the modulus and function of this counter.
(5 marks)

(ii) Show the outputs, Q_A, Q_B, Q_C timing diagrams of Figure 2(a) with proper labelling for this counter.
(5 marks)

(b) Produce a synchronous 3-bit up/down counter using positive edge-triggered D flip-flop for MSB, JK flip-flop for second bit and SR flip-flop for LSB. Assume D_A is the MSB input, J_B & K_B are the next flip-flop inputs and S_C & R_C are the LSB inputs. Assume all unused states as don't care if applicable.

Input Z will be used as the up/down control. The counter will count from 0 ⇨ 1 ⇨ 3 ⇨ 2 ⇨ 6 ⇨ 7 ⇨ 5 ⇨ 4 ⇨ 0 when input, Z = 0 and 0 ⇨ 4 ⇨ 5 ⇨ 7 ⇨ 6 ⇨ 2 ⇨ 3 ⇨ 1 ⇨ 0 when input, Z = 1 as shown below in Figure 2(c). Flip-flop D_A has output Q_A, flip-flop J_BK_B has output Q_B and flip-flop S_CR_C has output Q_C. Provide proper labelling for the designed logic circuit. Show all workings clearly. Use the flip-flop excitation tables provide in Table 2(b).

Table 2(b)

Outputs		Inputs	
Q_n	Q_{n+1}	S	R
0	0	0	×
0	1	1	0
1	0	0	1
1	1	×	0

Outputs		Inputs	
Q_n	Q_{n+1}	J	K
0	0	0	×
0	1	1	×
1	0	×	1
1	1	×	0

Outputs		Input
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Outputs		Input
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Q_n: Present State
Q_{n+1}: Next State

(i) Prepare the transition table/next state table for the up/down counter.

(4 marks)

(ii) Produce the simplest Boolean expressions for D_A, J_B, K_B, S_C and R_C inputs using Karnaugh map and/or Boolean algebra.

(5 marks)

(iii) Construct the logic circuit diagram for the simplified Boolean expressions obtained in part (b)(ii) using D, JK, SR flip-flops and other logic gates with proper labelling.

(6 marks)

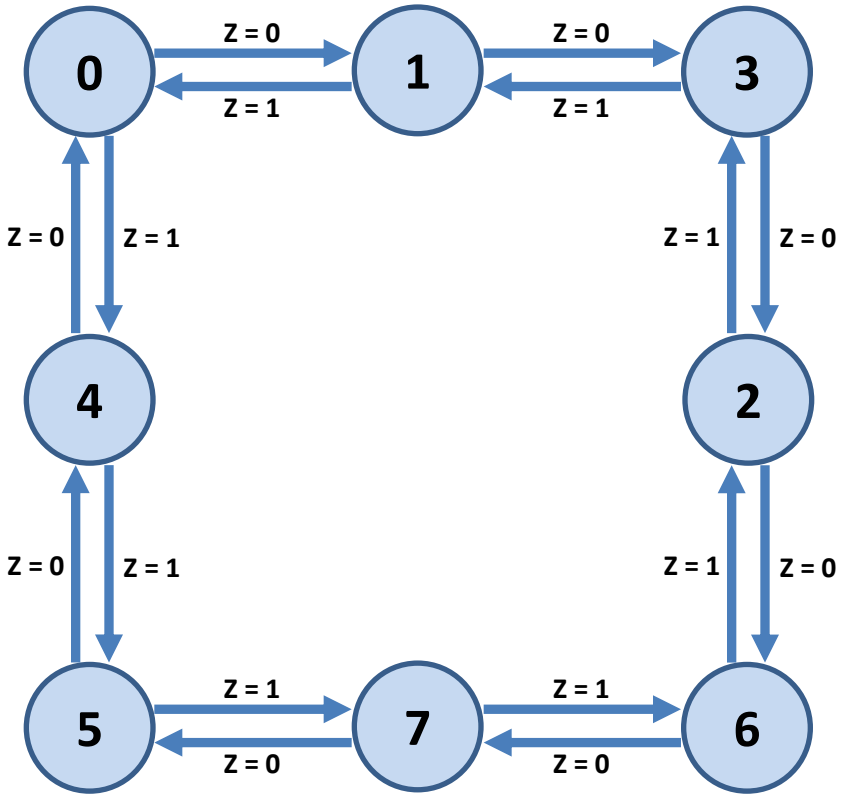

Figure 2(c)

Question 3

(a) Solve the numbering system transformation of $[2020.02_8 \times 20.25_{10}]$ to hexadecimal equivalent with 2 hexadecimal points accuracy. Show all workings clearly.

(5 marks)

(b) Table 3(b) shows a portion of hex NOT gates (DM7404) datasheet. Compute the following parameters from this datasheet, show all working clearly:

(i) Power dissipation, $P_{D(max)}$ on a DM7404 IC when the output condition is as shown in Figure 3(b). Assume that the V_{CC} used is 5.5V.

(6 marks)

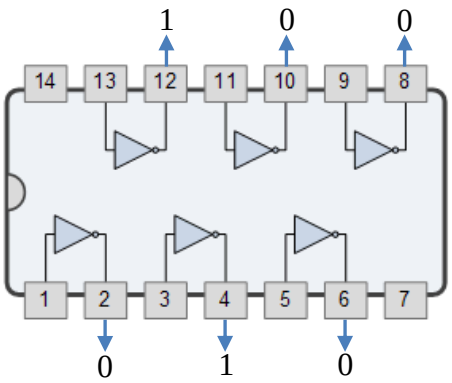

Figure 3(b)

(ii) Fan-out, a gate can safely drive.

(3 marks)

(iii) Noise Margin voltages, V_{NL} and V_{NH}.

(3 marks)

Table 3(b)

Recommended Operating Conditions

Symbol	Parameter	DM5404			DM7404			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			6	12	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			18	33	mA

(c) Table 3(c) shows the current ratings of TTL series logic gates. A 74F32 OR gate output is driving a few other TTL inputs as shown in Figure 3(c).

(i) Discover through calculation whether there is a loading problem.

(5 marks)

TTL Series	Output Drive		Input Loading	
	I_{OH}	I_{OL}	I_{IH}	I_{IL}
74	400μA	16mA	40μA	1.6mA
74S	1.0mA	20mA	50μA	2.0mA
74LS	400μA	8mA	20μA	400μA
74AS	2.0mA	20mA	200μA	2.0mA
74ALS	400μA	8mA	20μA	100μA
74F	1.0mA	20mA	20μA	600μA

Table 3(c)

(ii) The 74F32 OR gate output needs to be used to drive some 74AS inputs in addition to the load inputs. Compute how many additional 74AS inputs could the output drive without being overloaded?

(3 marks)

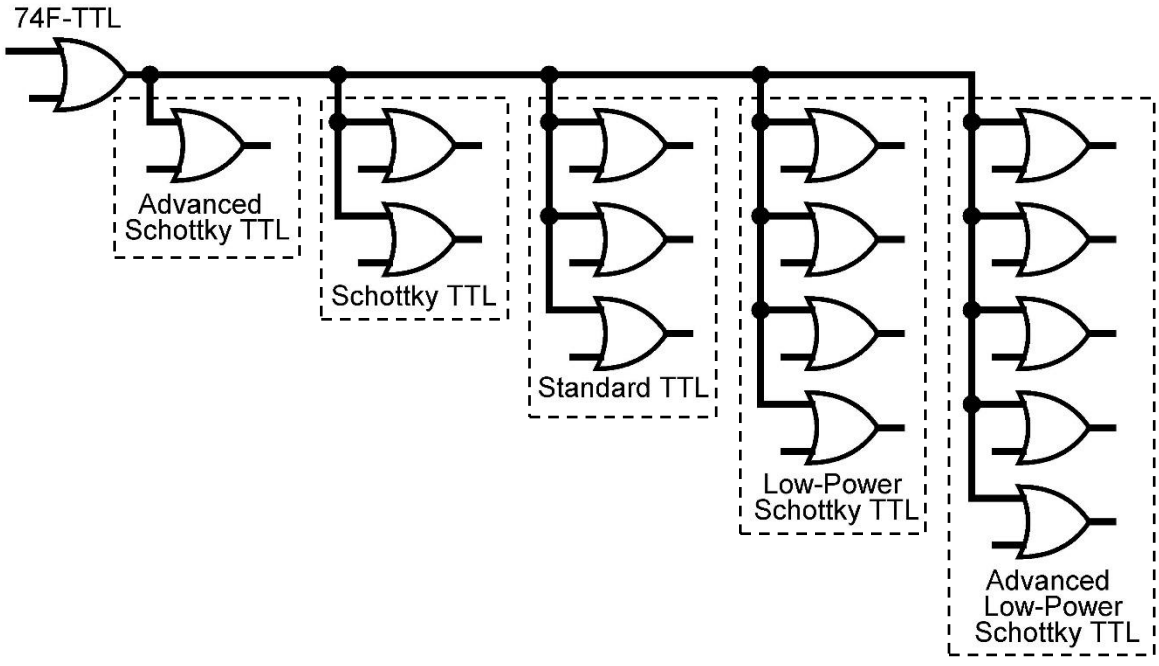

Figure 3(c)

Question 4

(a) Compute the 2's complement number of -88.53125_{10} in signed binary numbering system. Assuming the binary system is 8-bit system with 8 binary points. Show all workings clearly.

(5 marks)

(b) Figure 4(b) shows a computer controlling the speed of a motor. The 0 to 2mA analog current from the DAC is amplified to produce motor speeds from 0 to 1000 rpm (revolutions per minute).

(i) Compute how many bits should be used if the computer is to be able to produce a motor speed that is within 2 rpm of the desired speed?

(5 marks)

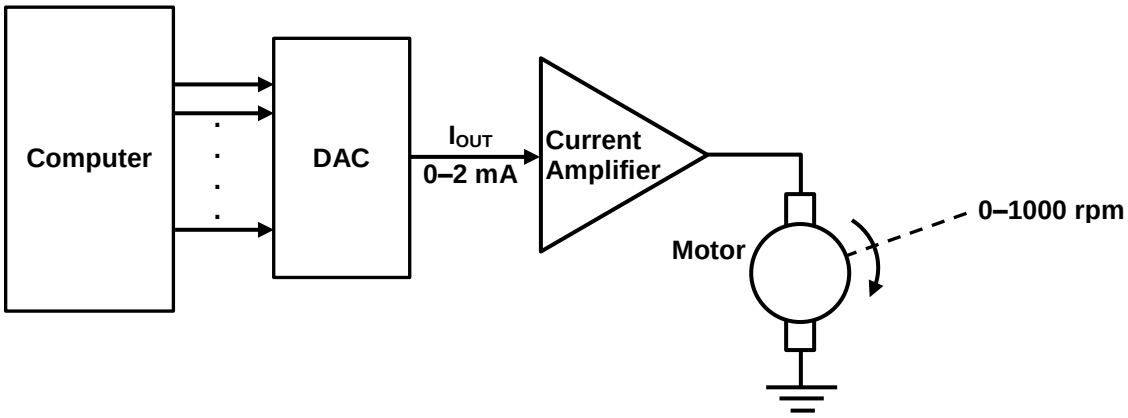

Figure 4(b)

(ii) Using the number of bits obtained, compute how close to 250 rpm can the motor speed be adjusted?

(5 marks)

(c) An 10-bit digital ramp ADC with a 5V full-scale value output uses a clock frequency of 16MHz. Assume the number of steps is using $2^n - 1$. Compute the following values:-

(i) the resolution and percentage of resolution.

(4 marks)

(ii) the digital output for an analog voltage of 2.020 V.

(2 marks)

(iii) the maximum and average conversion times.

(4 marks)

– THE END –