



**FINAL
ALTERNATIVE ASSESSMENT**

(COVER PAGE)

Session : April 2020

Programme : Diploma in Electrical & Electronic Engineering (DEEI)

Course : EEE1106: Analogue Electronics

Date of Examination : 4 August 2020 (Tuesday)

Time : 8.00am – 11.00am Reading Time : Nil

Duration : 3 Hours

Special Instructions :

This paper consists of **FOUR (4)** questions. Answer **ALL FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Material permitted : Non-Programmable Scientific Calculator

Materials provided : Nil

Examiner(s) : Dr. Su Hsiao Wei

Chief Moderator : Mr Johnny Wong

This paper consists of 8 printed pages, including the cover page

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DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
 EEE1106: ANALOGUE ELECTRONICS
 FINAL ALTERNATIVE ASSESSMENT: APRIL 2020 SESSION

Instructions: This paper consists of **FOUR (4)** questions. Answer **ALL FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

- (a) Figure 1(a) shows a single stage FET amplifier and its voltage gain frequency response.

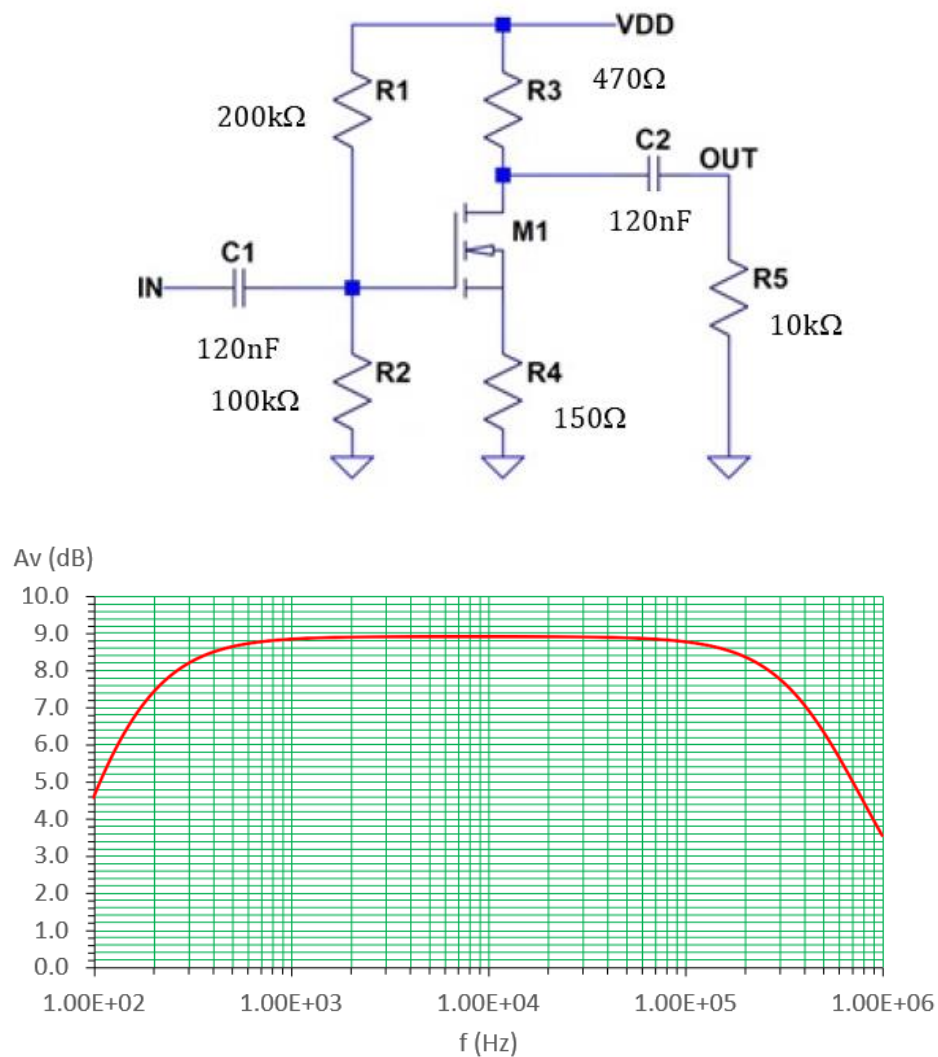


Figure 1(a)

- (i) Explain the state of the circuit, in terms of the behavior of the capacitors, which exhibits maximum voltage gain (approximately 8.9 dB in this case) at the mid-band frequency spectrum. (2 marks)
- (ii) Explain the root cause of the gain reduction at the low frequency spectrum. (2 marks)
- (iii) Explain the root cause of the gain reduction at the high frequency spectrum. (2 marks)

(b) Figure 1(b) shows the voltage gain frequency response of an amplifier.

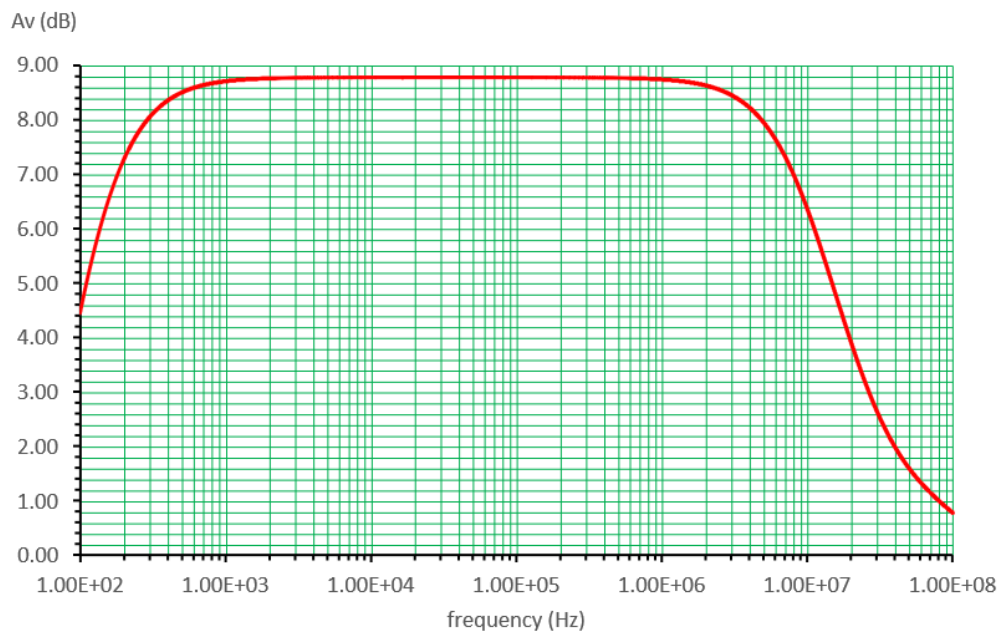


Figure 1(b)

- (i) Calculate the maximum output voltage of the amplifier in volts if the input voltage is a sinusoidal signal having a peak value of 4.0 V at 200 kHz. (4 marks)
- (ii) Estimate the bandwidth of the amplifier. (5 marks)
- (c) Figure 1(c) shows the AC equivalent circuit model of an FET voltage amplifier.

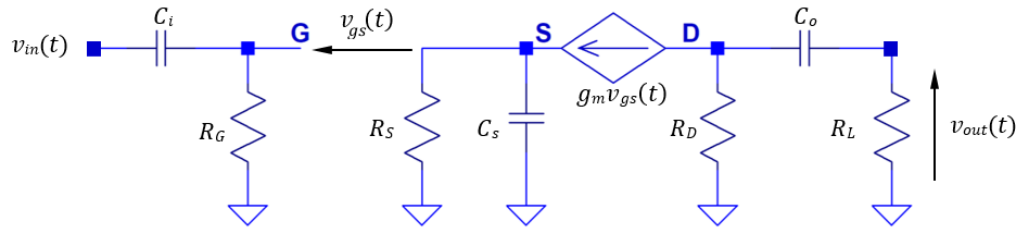


Figure 1(c)

- (i) Draw an AC equivalent circuit model for the amplifier to evaluate the cutoff frequency contributed by capacitor C_s . (3 marks)
- (ii) Utilizing the AC equivalent circuit model obtained in part 1(c)(i), show that the voltage transfer function of $V_S(s)/V_G(s)$ can be expressed in the form of,
- $$\frac{V_S(s)}{V_G(s)} = \frac{a_0}{s + \omega_o}$$
- and state a_0 and ω_o in terms of the relevant passive components and transistor parameter, g_m . (5 marks)
- (iii) Determine the cutoff frequency expression of the amplifier which is contributed by capacitor C_s . (2 marks)

Question 2

- (a)
- (i) Draw the schematic diagram of an inverting amplifier utilizing a single op-amp, operating in dual supply mode. (2 marks)
- (ii) State the voltage transfer function expression of the amplifier given in part 2(a)(i). (1 mark)
- (iii) Explain the reason for naming the circuit as "inverting amplifier". (2 marks)
- (b) Figure 2(b) shows an inverting summing amplifier. The op-amp used is assumed ideal.

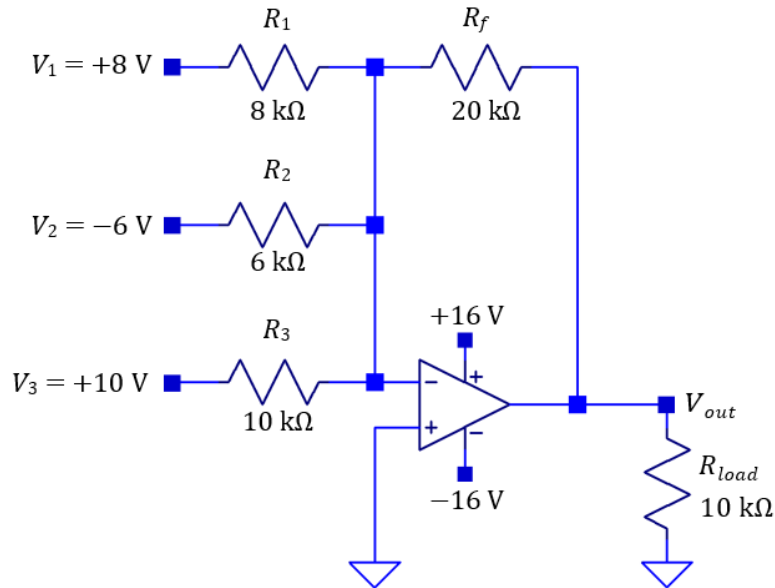


Figure 2(b)

- (i) Calculate the value of the output voltage V_{out} . (5 marks)
- (ii) Calculate the maximum current drawn from the op-amp. (5 marks)
- (c) Figure 2(c) shows an inverting Schmitt Triggered Comparator. The op-amp used is assumed ideal. The input voltage, V_{in} , is taken from a sensor output which varies between 0 V and 5 V levels. V_{ref} is a reference voltage targeted to concurrently adjust the upper and lower threshold values of the comparator. Identify the range of V_{ref} such that the comparator maintain a valid hysteresis characteristic. Show your analysis clearly. (10 marks)

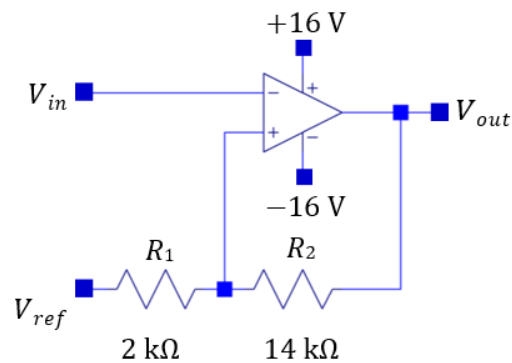


Figure 2(c)

Question 3

- (a) Clearly state in a table form, four differences in the frequency response between an ideal analogue filter and a practical one in general.

(4 marks)

- (b) The voltage transfer function of a filter circuit is given as,

$$T(s) = \frac{a_0}{s^2 + b_1s + b_0}$$

- (i) Identify the type and order of the filter that has the given transfer function.

(2 marks)

- (ii) Identify the cut-off frequency of the filter circuit.

(1 mark)

- (iii) Draw the schematic diagram of a passive filter that has the similar voltage transfer function and derive the voltage transfer function.

(5 marks)

- (iv) Draw the schematic diagram of a passive filter that has the similar voltage transfer function and derive the voltage transfer function.

(3 marks)

- (c) Figure 3(c) shows an example of an analogue filter.

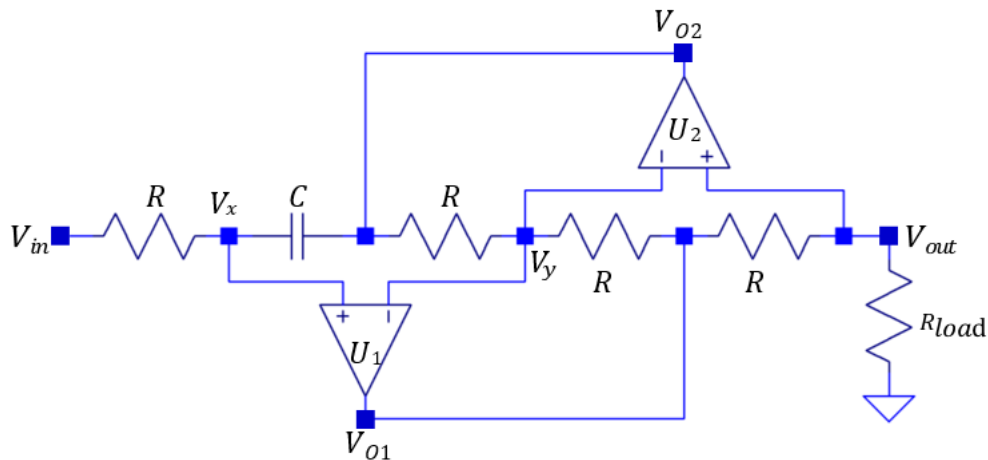


Figure 3(c)

- (i) Assuming that op-amps U_1 and U_2 are operating linearly, determine the relationship between V_x , V_y and V_{out} .

(3 marks)

- (ii) Derive the voltage transfer function expression of the filter, $V_{out}(s)/V_{in}(s)$.
(5 marks)
- (iii) Determine the type of filter that is implemented by the circuit based on the voltage transfer function obtained in part 3(c)(ii).
(2 marks)

Question 4

- (a) Explain,
- (i) the function of a harmonic oscillator.
(2 marks)
- (ii) the oscillation criteria of an RC feedback harmonic oscillator.
(3 marks)
- (b) Figure 4(b) shows the schematic diagram of a Wien Bridge oscillator. R_T is a thermistor in which its resistance reduces when its body temperature increases.

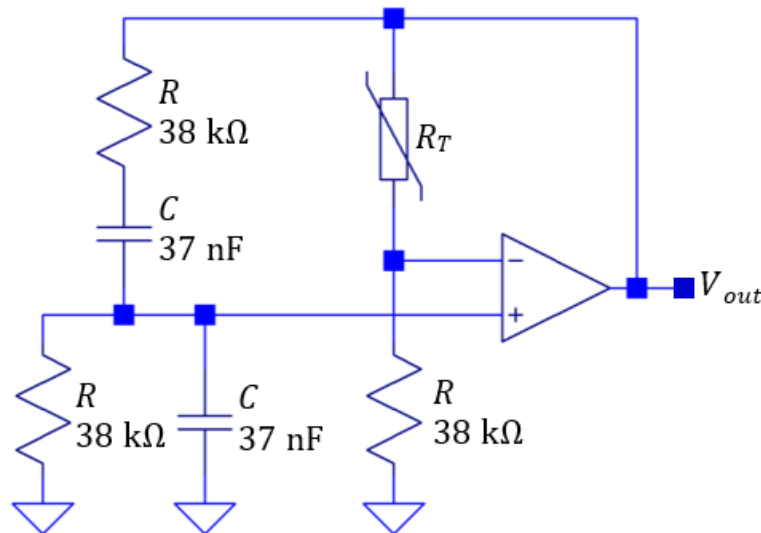


Figure 4(b)

- (i) Calculate the expected frequency of V_{out} .
(3 marks)
- (ii) To initiate oscillation, R_T needs to be at least 10% higher than its resistance value that sustain output oscillation, calculate the minimum value of R_T to initiate oscillation.
(3 marks)

- (iii) If the implemented thermistor, R_T has a characteristic as shown in Figure 4(b)(iii), estimate the expected RMS value of output voltage, V_{out} . (4 marks)

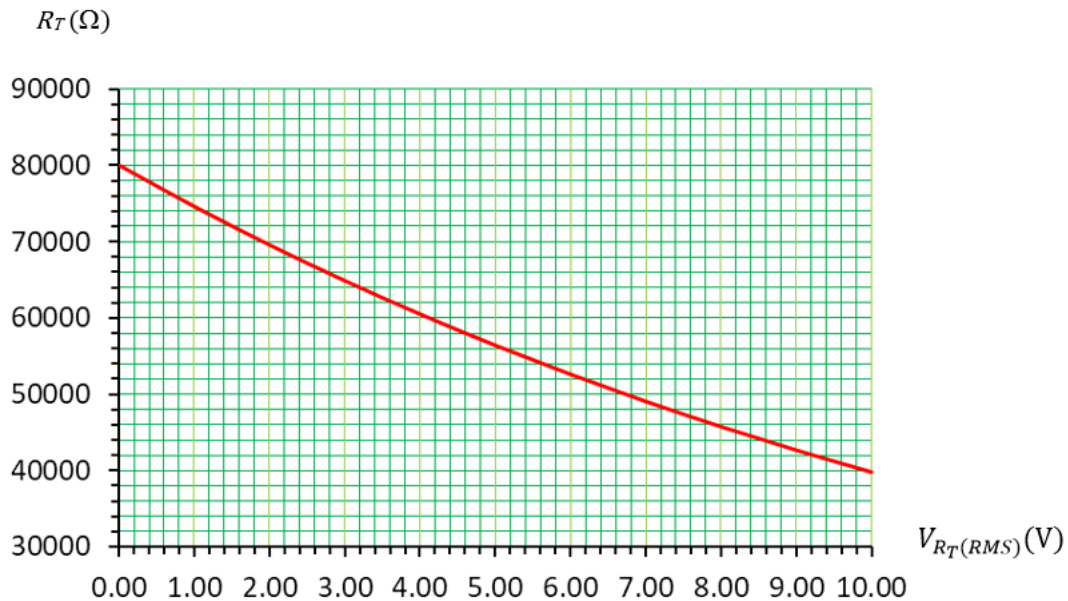


Figure 4(b)(iii)

- (c) Figure 4(c) shows the schematic diagram of a Sallen-Key low pass filter modified to implement a harmonic oscillator. The modification involved grounding its input terminal and replacing one of its amplifier's feedback resistor with a thermistor identical to the one shown in part 4(b).

Determine the expression of R_T in terms of the passive components in the circuit to sustain output oscillation. Show all workings clearly.

(10 marks)

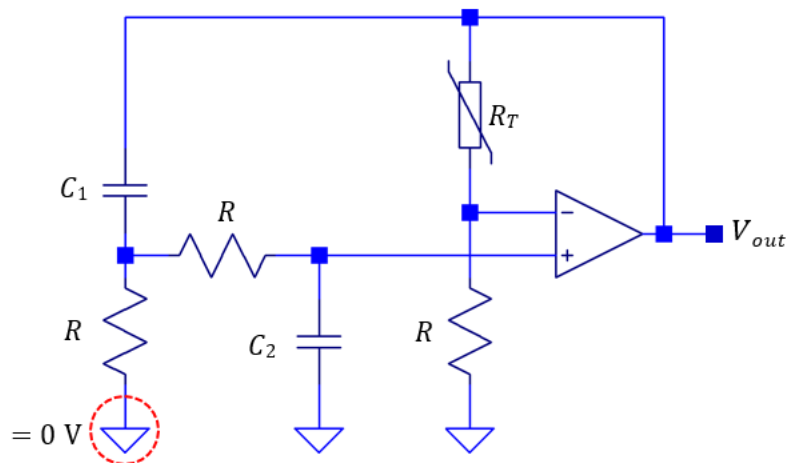


Figure 4(c)