INTI
International College Penang

FINAL
Examination Paper

(COVER PAGE)

Session	:	**April 2019**
Programme	:	Diploma in Electrical and Electronic Engineering (DEEI)
Course	:	**EEE 2101: Introduction to Digital Electronics**
Date of Examination	:	29 July 2019 (Monday)
Time	:	11:00am – 1:00pm Reading Time : Nil
Duration	:	2 Hours
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL

Materials permitted :

Non-Programmable Scientific Calculator

Materials provided :

Nil

Examiner(s)	:	**Mr. Steven Khoo Boo Tap**
Moderator	:	Dr. Ooi Beng Lee

*This paper consists of **12** printed pages, including the cover page.*

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE2101: INTRODUCTION TO DIGITAL ELECTRONICS
FINAL EXAMINATION: APRIL 2019 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

A combinational logic circuit is required, which accepts BCD inputs 0000 to 1001 and displays the alphanumeric '*INTl2019>', respectively, as shown below in Figure 1(a). The BCD inputs are labelled as WXYZ, W is the MSB and Z is the LSB. Figure 1(b) shows a Common-Cathode 16 segment display. Assume all unused inputs as don't care. Show all working clearly.

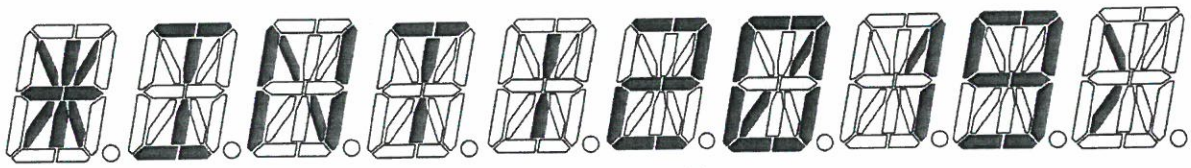

Figure 1(a)

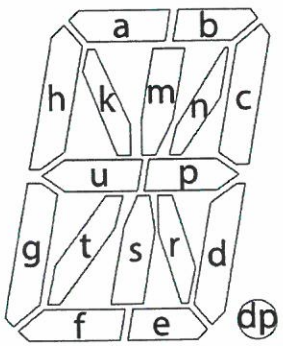

Figure 1(b)

(a) Give the complete truth table for the inputs to segments a through u of the 7 segment including the unused inputs.

(6 marks)

(b) Find the simplest SOP form of the logic expression for segments b, c and d using Karnaugh map and Boolean algebra.

(9 marks)

(c) Design a logic circuit for segment b, c and d using only 2-input NAND gates with minimum gates consideration. State the number of 7400 ICs used.

(10 marks)

Question 2

(a) Table 2(a) and Table 2(b) show a portion of a dual positive edge-triggered D flip-flops (DM7474) and a triple 3-input NOR gate (DM74LS27) datasheet respectively. Figure 2(a) shows the logic circuit diagram of an asynchronous counter which uses positive edge-triggered D flip-flops with labelling of $Q_AQ_BQ_C$ where Q_C is MSB and Q_A is LSB. Assume the environment is at $T_A = 25°C$ with $V_{CC} = 5V$ and the load capacitance is $15pF$.

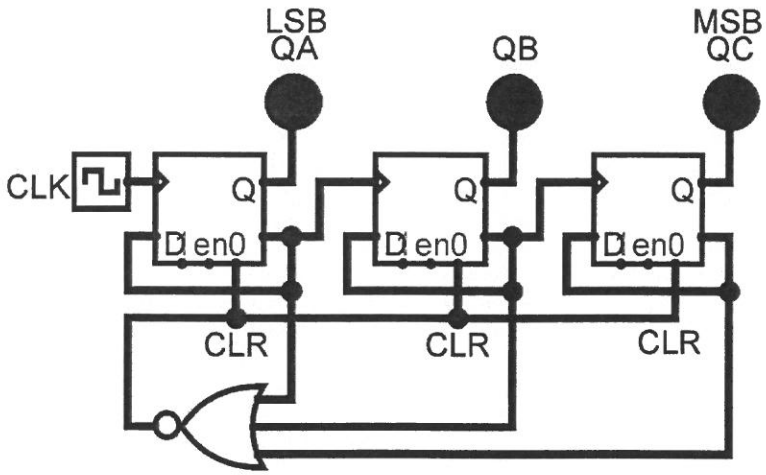

Figure 2(a)

Table 2(a) D flip-flop

Switching Characteristics at V_{CC} = 5V and T_A = 25°C					
Symbol	**Parameter**	**From (Input) To (Output)**	**R_L = 400Ω, C_L = 15pF**		**Units**
			Min	**Max**	
f_{MAX}	Maximum Clock Frequency		15		MHz
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Q		40	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clear to $\overline{Q}$		25	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Q or $\overline{Q}$		40	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Q or $\overline{Q}$		25	ns

Table 2(b) NOR gate

Symbol	**Parameter**	**R_L = 2 kΩ**				**Units**
		C_L = 15 pF		**C_L = 50 pF**		
		Min	**Max**	**Min**	**Max**	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	13	5	18	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	10	4	15	ns

(i) Analyse its operation to determine whether the logic circuit of Figure 2(a) is working as an up counter or down counter. Also, state the modulus and function of this counter.

(4 marks)

(ii) Determine the total propagation delay from the given datasheets in Table 2(a) and Table 2(b).

(3 marks)

(iii) Find the maximum frequency at which the counter can be operated stably.

(2 marks)

(iv) Determine the output timing diagram of Figure 2(a) with proper labelling for this counter.

(4 marks)

(b) Find the following number system transformation. Show all workings clearly.

(i) $[1401.1401_8 - 101.101_{16}]$ to decimal equivalent with 3 decimal points accuracy.

(4 marks)

(ii) $[129.328125_{10} \times 1101.11_2]$ to octal equivalent with 3 octal points accuracy.

(4 marks)

(iii) $[12.5_8 + 12.48_{16}]$ to BCD equivalent with full BCD points accuracy.

(4 marks)

Question 3

(a) Table 3(a) shows a portion of quadruple 2-input OR gates (DM74LS32) datasheet. Find the following parameters from this datasheet, show all working clearly:

(i) Fan-out, a gate can safely drive.

(3 marks)

(ii) Average Power dissipation, $P_{D\,(avg)}$ for one gate on a DM74LS32 IC.

(3 marks)

(iii) Noise Margin voltages, V_{NL} and V_{NH}.

(3 marks)

Table 3(a) DM74LS32 (2-input OR gate)

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V	DM54LS and 54LS	−55°C to +125°C
Input Voltage	7V	DM74LS	0°C to +70°C
Operating Free Air Temperature Range		Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS32			DM74LS32			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			3.1	6.2	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			4.9	9.8	mA

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	11	4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	11	4	15	ns

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

(b) Find the Boolean expression of Z in Figure 3(b) and present the expression to the minimum using Boolean simplification only. Use one IC of your choice to represent the simplified expression. Show working clearly.

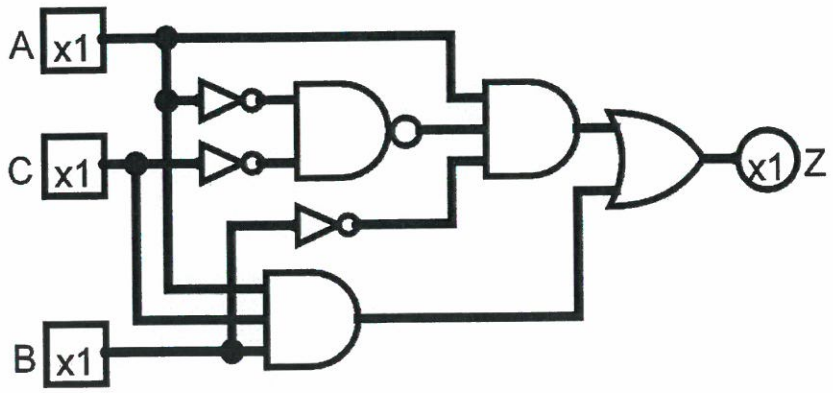

Figure 3(b)

(8 marks)

(c) Table 3(c) shows the truth table of 2-bit Adder using A_1, A_0, B_1 and B_0 as inputs with S_1 (Sum1), S_0 (Sum0) and C_o (Carry Out) as outputs.

Table 3(c) Truth Table for 2-bit Adder

Inputs				Outputs		
A_1	A_0	B_1	B_0	C_o	S_1	S_0
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	1	0	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	1
1	1	1	1	1	1	0

Using 2:1 Multiplexers, design the Product outputs (S_0 and C_o) for 2-bit Adder. Use input B_1 as the select line. Show the Multiplexer mapping of S_0 and C_o. Additional gates can be used in conjunction with the multiplexers.

(8 marks)

Question 4

(a) For the given truth tables in Table 4a(i) and excitation tables in Table 4a(ii),

(i) design a D flip-flop function using SR flip-flop. The design can be added with additional gates in order to fulfil the conversion. Show all working clearly for SR-to-D converter.

(5 marks)

(ii) design a T flip-flop function using JK flip-flop. The design can be added with additional gates in order to fulfil the conversion. Show all working clearly for JK-to-T converter.

(5 marks)

Table 4a(i) Flip-flop Truth Tables

Inputs		Outputs	
S	R	Q_n	Q_{n+1}
0	0	No Change	
0	1	Reset	
1	0	Set	
1	1	Invalid	

Inputs		Outputs	
J	K	Q_n	Q_{n+1}
0	0	No Change	
0	1	Reset	
1	0	Set	
1	1	Toggle	

Input	Outputs	
D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Input	Outputs	
T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Q_n: Present State
Q_{n+1}: Next State

Table 4a(ii) Flip-flop Excitation Tables

Outputs		Inputs	
Q_n	Q_{n+1}	S	R
0	0	0	×
0	1	1	0
1	0	0	1
1	1	×	0

Outputs		Inputs	
Q_n	Q_{n+1}	J	K
0	0	0	×
0	1	1	×
1	0	×	1
1	1	×	0

Outputs		Input
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Outputs		Input
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Q_n: Present State
Q_{n+1}: Next State

(b) Figure 4(b) shows a BCD counter that produces a four-bit output representing the BCD code for the number of pulses that have been applied to the counter input. For example, after four pulses have occurred, the counter outputs are $DCBA = 0100_2 = 4_{10}$. The counter resets to 0000_2 on the tenth pulse and starts counting over again. In other words, the $DCBA$ outputs will never represent a number greater than $1001_2 = 9_{10}$. The logic circuit that produces a HIGH output whenever the count is 2, 3, 7 or 9. Take advantage of the don't-care conditions. Show all working steps clearly.

(i) Give the complete truth table for the logic circuit.

(3 marks)

(ii) Give the simplest Boolean expression for the logic circuit using Karnaugh Map.

(3 marks)

(iii) Design the logic circuit using only 2-input NOR gates with minimum gates consideration.

(5 marks)

(iv) Build the expression obtained in Question 4(b)(ii) using only 2-to-4 Decoders and logic gates (if needed).

(4 marks)

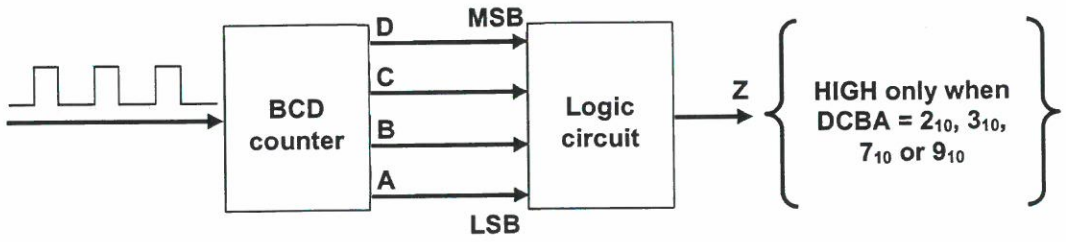

Figure 4(b)

Question 5

(a) Table 5(a) shows the current ratings of TTL series logic gates. A 74S04 NOT gate output is driving a few other TTL outputs as shown in Figure 5(a). Determine if there is a loading problem.

(4 marks)

Table 5(a) TTL series logic gates

TTL Series	Output Drive		Input Loading	
	I_{OH}	I_{OL}	I_{IH}	I_{IL}
74	400μA	16mA	40μA	1.6mA
74S	1.0mA	20mA	50μA	2.0mA
74LS	400μA	8mA	20μA	400μA
74AS	2.0mA	20mA	200μA	2.0mA
74ALS	400μA	8mA	20μA	100μA
74F	1.0mA	20mA	20μA	600μA

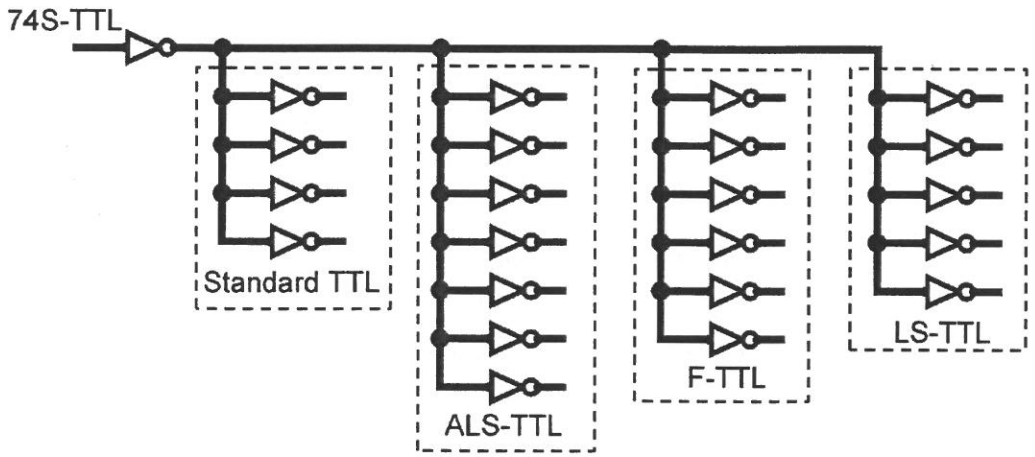

Figure 5(a)

The 74S04 NOT gate output needs to be used to drive some 74S inputs in addition to the load inputs. Determine how many additional 74S inputs could the output drive without being overloaded?

(3 marks)

(b) Express the following Boolean expression using Karnaugh Map and Boolean expression to the most simplified form:

(i) $F_1(W,X,Y,Z) = \prod(0,1,4,5,6,7,11,13)$ to the simplest SOP form.

(4 marks)

(ii) $F_2(R,S,T,U) = \sum m(0,1,3,7,15) + d(12,13,14)$ to the simplest POS form.

(4 marks)

(c) Design a synchronous 3-bit up/down counter using positive edge-triggered JK flip-flop for MSB, D flip-flop for second bit and SR flip-flop for LSB. Assume J_2 & K_2 are the MSB input, D_1 is the next flip-flop inputs and S_0 & R_0 are the LSB inputs. Assume all unused states as don't care.

Input Z will be used as the up/down control. The counter will count from 0 ⇨ 3 ⇨ 4 ⇨ 5 ⇨ 6 ⇨ 7 ⇨ 0 when input, Z = 1 and 7 ⇨ 6 ⇨ 5 ⇨ 4 ⇨ 3 ⇨ 0 ⇨ 7 when input, Z = 0 as shown below in Figure 5(c).

Use $Q_2Q_1Q_0$ outputs labelling for J_2 & K_2, D_1 and S_0 & R_0 inputs. Provide proper labelling for the designed logic circuit. Show all workings clearly.

(i) Prepare the transition table/next state table for the up/down counter.

(5 marks)

(ii) Design the simplified Boolean expression for J_2, K_2, D_1, S_0 and R_0 inputs using Karnaugh map and Boolean algebra to the simplest form. Logic circuit implementation diagram is not required.

(5 marks)

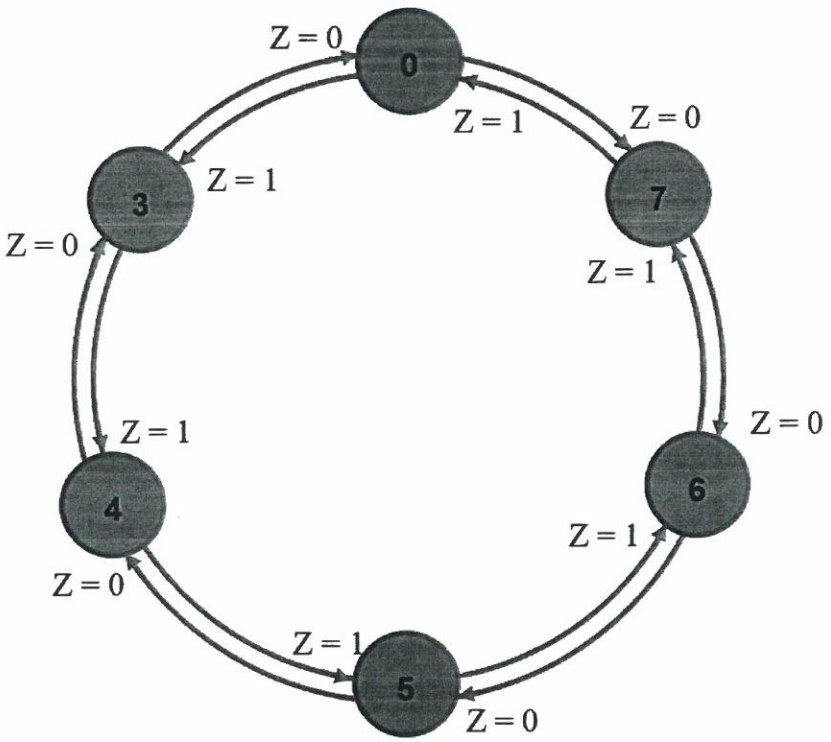

Figure 5(c)

Question 6

(a) A binary-weighted-input DAC is shown in Figure 6(a). If the LSB bit resistor has a value of $120k\Omega$, determine the values of the other input resistors. Also, calculate the V_{out} if the DAC has a binary input of 1101 with Logic 1 (HIGH) as +5.0V and Logic 0 (LOW) as 0V. Assume that R_f equals to $10k\Omega$. State the disadvantages of using this method of DAC.

(7 marks)

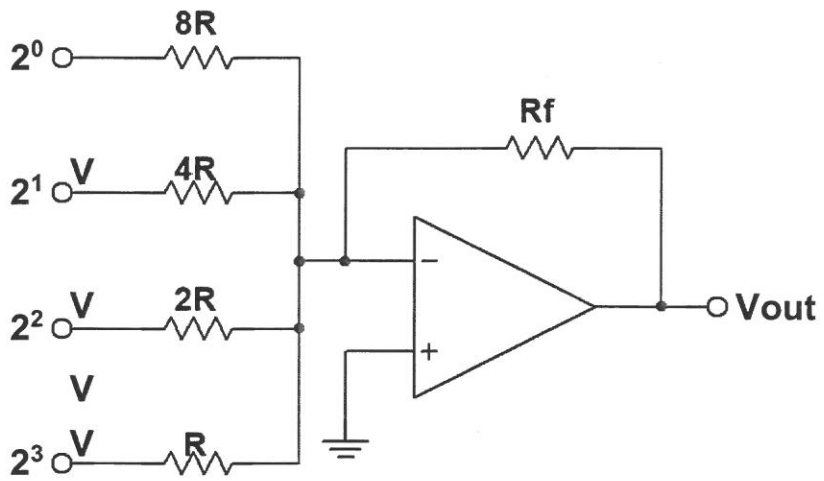

Figure 6(a)

(b) Figure 6(b) shows a computer controlling the speed of a motor. The 0 to 8mA analog current from the DAC is amplified to produce motor speeds from 0 to 8000 rpm (revolutions per minute). Explain how many bits should be used if the computer is to be able to produce a motor speed that is within 2 rpm of the desired speed?

(5 marks)

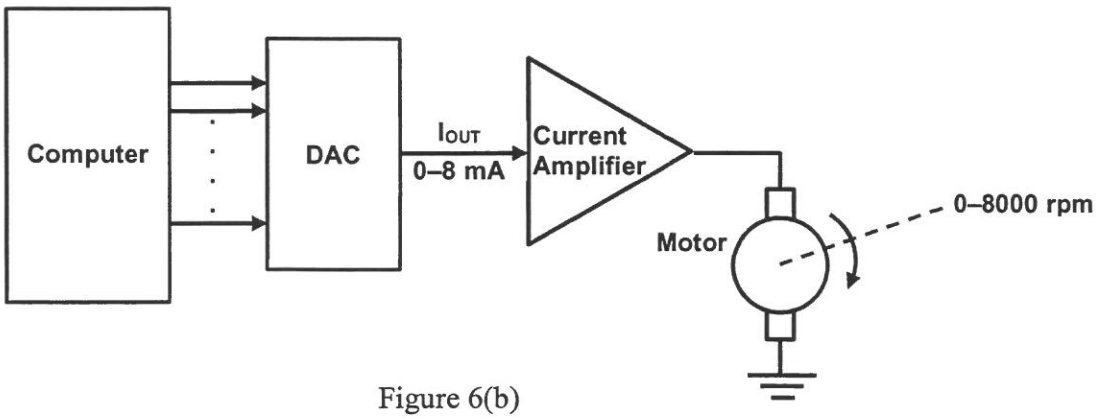

Figure 6(b)

Using the number of bits obtained, explain how close to 1832 rpm can the motor speed be adjusted?

(5 marks)

(c) A 12-bit DAC produces an output current in proportion to its digital input. For a digital input of 000010100000, an output current of 40mA is produced.

(i) Determine the output current be if the digital input is 110001111010.

(4 marks)

(ii) Determine the digital input if a 1009mA output current is required.

(4 marks)

– THE END –

EEE2101(F)/Apr19/Steven Khoo/06/04/19