



INTI International College Penang

FINAL
Examination Paper

(COVER PAGE)

Session : April 2019

Programmes : Diploma in Electrical and Electronic Engineering (DEEI)

Course : EEE1106: Analogue Electronics

Date of Examination : 2 August 2019 (Friday)

Time : 11:00am – 1:00pm

Duration : 2 Hours Reading Time Nil

Special Instructions :

This paper consists of SIX (6) questions. Answer any FOUR (4) questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL BY THE STUDENTS.

Materials Permitted :

Non-programmable Calculator (e.g. Model fx570 Series)

Materials Provided :

Worksheet for Q2(c)

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Moderator : Prof. Ir. Dr. Mandeep Singh

This paper consists of 10 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
 EEE1106: ANALOGUE ELECTRONICS
 FINAL EXAMINATIONS: APRIL 2019 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks. The marks allocated to each sub-question are shown in square brackets at the right-hand margin. Present your answers neatly and clearly. The assessor reserves the rights to ignore your answers if they are ambiguous.

Question 1

- a. State and explain the main parameters of a voltage amplifier, which are obtainable from the frequency response plot of the voltage amplifier. [5]
- b. Figure-Q1(b) shows the AC equivalent circuit model of the input stage of a voltage amplifier. I_S and R_S form the current source model, C_i is the input coupling capacitor while R_i is the effective input resistance, and I_i is the input current of the amplifier.

Apply relevant circuit principles to show that the cutoff frequency contributed by this input stage is given as,

$$f_c = \frac{1}{2\pi(R_S + R_{in})C_{in}} \quad [10]$$

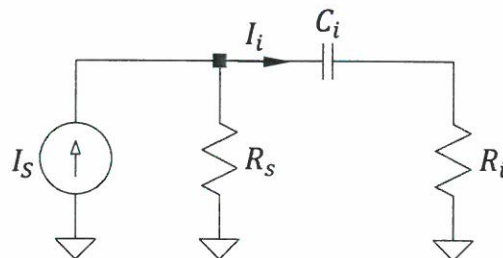


Figure-Q1(b)

- c. Figure-Q1(c) shows the AC equivalent circuit of an FET-based amplifier circuit at mid-band frequency. The FET used in the amplifier has 8 mS of transconductance, g_m .

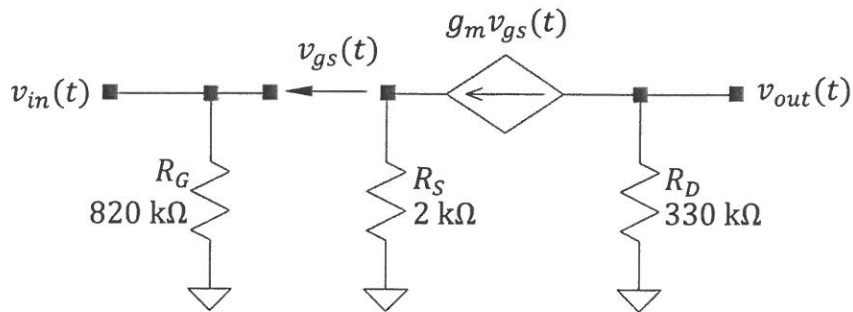


Figure-Q1(c)

- i. Analyze the amplifier in Figure-Q1(c) to quantify its mid-band voltage gain, v_{out}/v_{in} . [4]
- ii. If the output is connected to an oscilloscope that has an input channel impedance characterized as a 1 MΩ grounded resistor in parallel with a 15 pF capacitor. Identify the impact of this connection towards the upper cutoff frequency of the amplifier. [6]

Question 2

- a. Explain crossover distortion in power amplifier and name the type of power amplifier that exhibits such distortion. [5]

- b. A power amplifier circuit and its output AC characteristic graph are shown in Figure-Q2(b)(i) and Figure-Q2(b)(ii) respectively. Also shown in Figure-Q2(b)(ii), are the amplifier's output voltage and its corresponding output current swing. Transformer T_1 is considered ideal, such that its wiring resistance and power dissipation are negligible.

Calculate the,

- i. Transformer turn ratio, N . [4]
- ii. Power conversion efficiency of the power amplifier. [6]

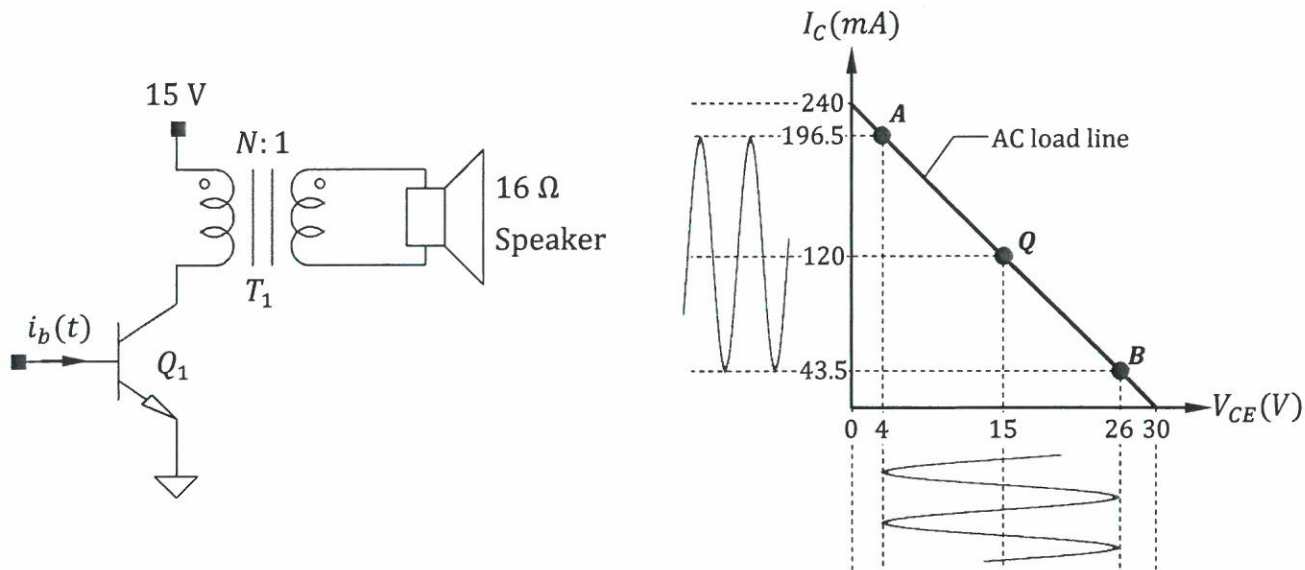


Figure-Q2(b)(i)

Figure-Q2(b)(ii)

c. Figure-Q2(c) shows a pre-biased power amplifier. The two diodes, D_1 and D_2 , have forward bias voltages of 0.8 V and this voltage matches well with the respective B-E junction biasing voltage of transistors Q_1 and Q_2 .

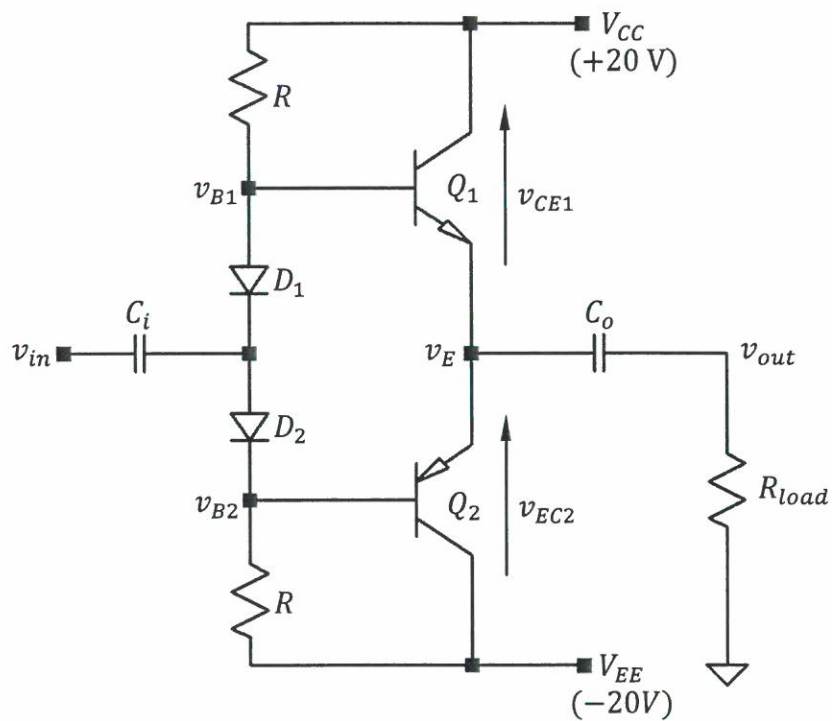


Figure-Q2(c)

If $v_{in} = 4\sin(\omega t)$ and assume that the coupling capacitors C_i and C_o couple the AC signal into and out of the power amplifier without causing any loss in signal, sketch on the attached worksheet, "Worksheet for Q2(c)", the synchronized timing diagrams of

- i. $v_{B1}(t)$ [2]
- ii. $v_{B2}(t)$ [2]

- iii. $v_{CE1}(t)$ [2]
- iv. $v_{CE2}(t)$ [2]
- v. $v_{out}(t)$ [2]

Question 3

- a. Clearly explain the difference between the respective output voltage of the two op-amp circuits shown in Figure-Q3(a) when both circuits are subjected to a pure sinusoidal voltage. [5]

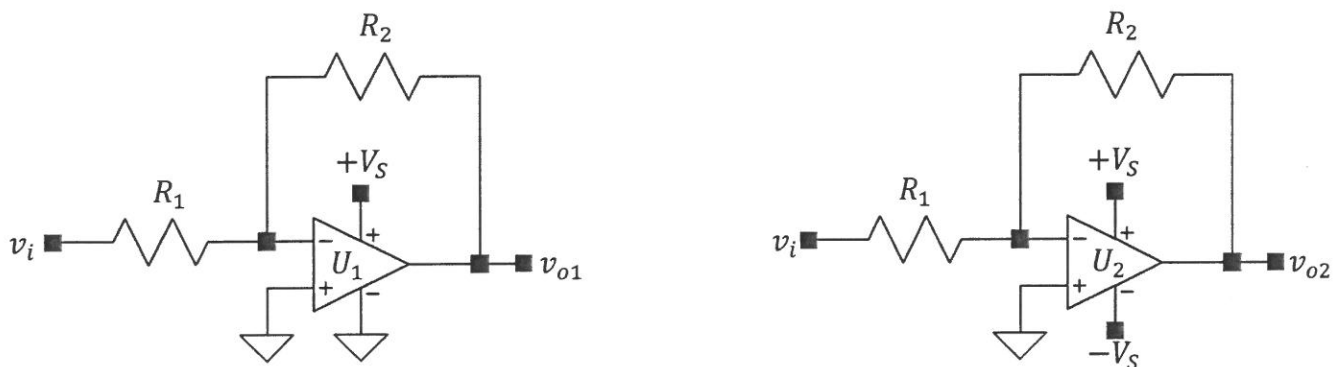


Figure-Q3(a)

- b. Figure-Q3(b) shows a Schmitt triggered comparator. Sketch the voltage transfer curve of the comparator circuit by clearly showing the saturated output voltage levels, the upper and lower threshold points of the circuit. Assume that the op-amps used in the circuit have rail-to-rail output. Show all your workings clearly. [10]

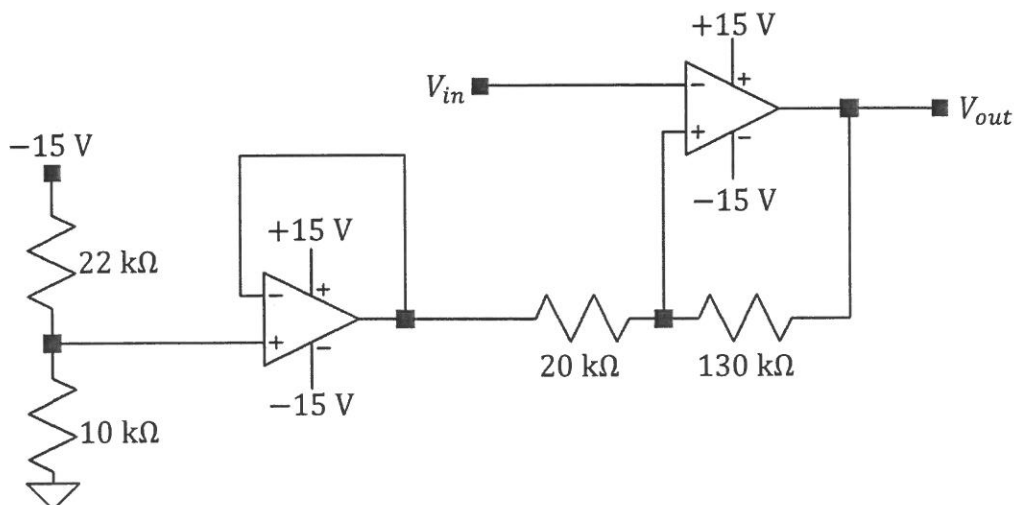


Figure-Q3(b)

- c. Figure-Q3(c) shows a non-inverting amplifier implemented using an op-amp with the following specifications:

$$V_{supply(max)} = \pm 18 \text{ V}$$

$$\text{Slew Rate} = 13 \text{ V}/\mu\text{s}$$

$$|V_{o(sat)}| = |V_{supply}| - 1 \text{ V}$$

If $v_{in} = 2 \sin(400000\pi t)$, analyze the amplifier circuit to determine the suitability of the op-amp implementation. Justify your answer clearly. [10]

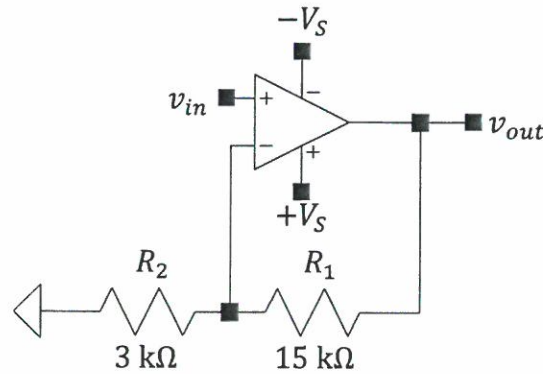


Figure-Q3(c)

Question 4

- a. Express the general transfer function of a 2nd order band pass filter and explain how the filter's characteristics can be obtained from this transfer function expression. [5]
- b. i. Draw a 2nd order passive band pass filter using only an inductor, a capacitor and a resistor. [2]
- ii. Derive the quality factor of the filter drawn in part (b)(i) in terms of the component values L , C and R . [8]
- c. Figure-Q4(c)(i) shows a Sallen-Key filter circuit and Figure-Q4(c)(ii) shows its corresponding Butterworth frequency response. Identify the design requirements on all the passive components in the circuit to achieve the given frequency response. [10]

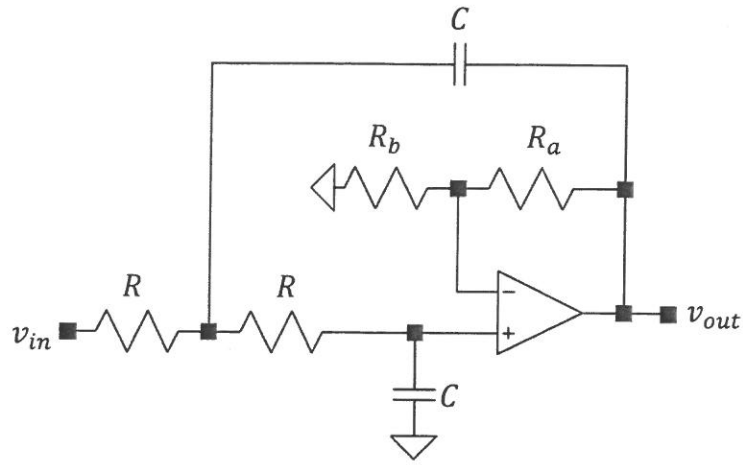


Figure-Q4(c)(i)

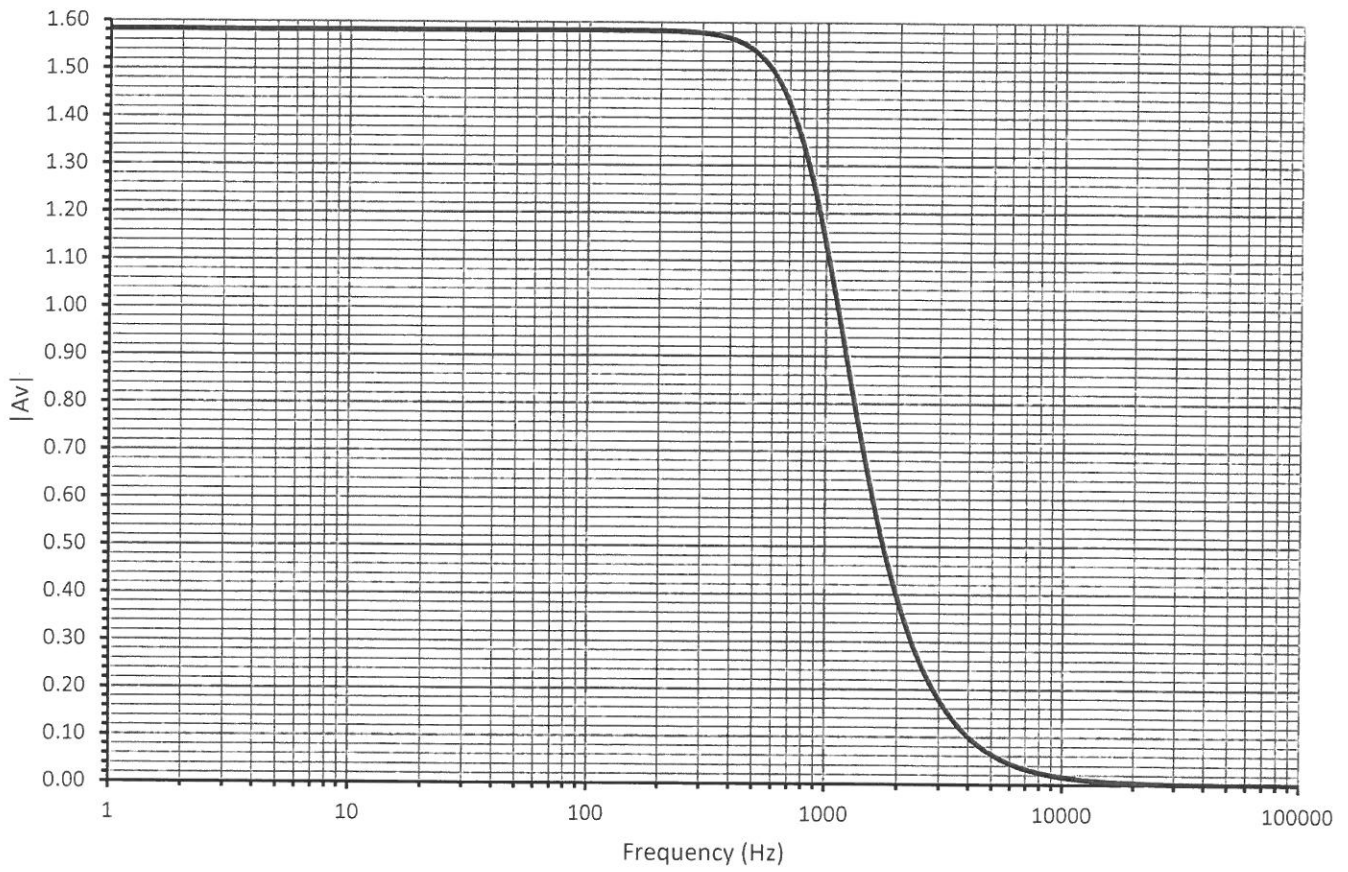


Figure-Q4(c)(ii)

Question 5

- a. Explain oscillator circuit and its basic output design requirements. [5]
- b. Figure-Q5(b) shows an example of a relaxation oscillator assembled from a 555 timer IC.

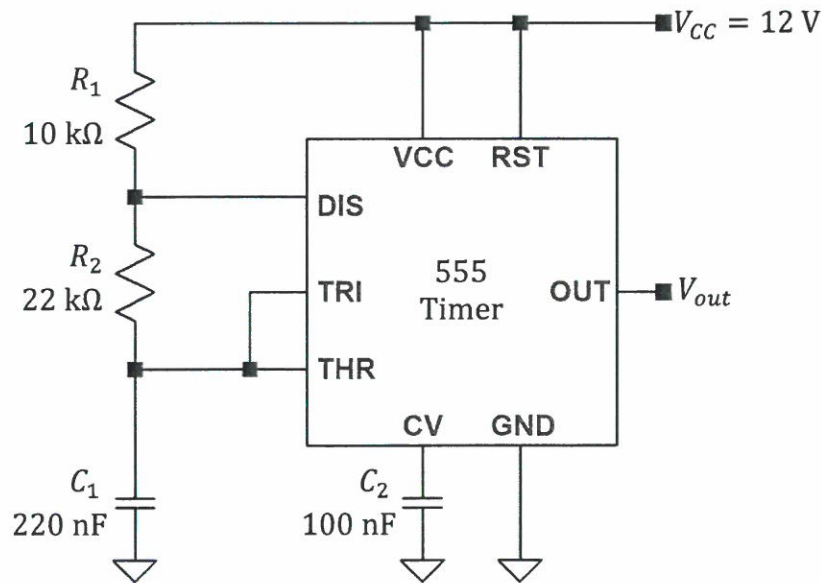


Figure-Q5(b)

- i. Calculate the frequency of the output signal. [3]
- ii. Calculate the duty cycle of the output signal in %. [3]
- iii. Suggest and explain the method to allow this oscillator to produce an output signal with duty cycle which is less than 50%. [2]
- iv. State the limitation of the method suggested in part (b)(iii). [2]
- c. Figure-Q5(c) shows a simple circuit to produce a square wave. The op-amp is assumed ideal and is operating in dual supply mode. Formulate the relationship between the period of oscillation and the product of C and R . [10]

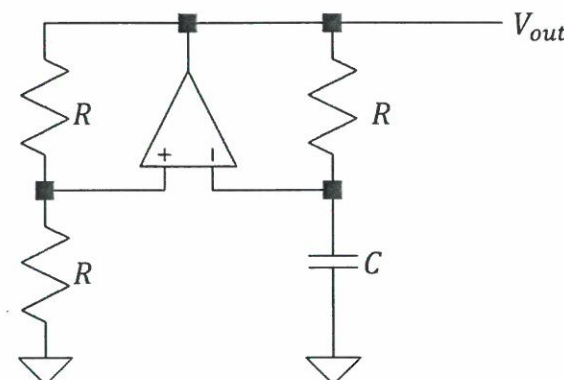


Figure-Q5(c)

Question 6

- a. Figure-Q6(a) shows a sinusoidal voltage source, v_s , applied across a $12\ \Omega$ resistive load. Under no-load condition, the peak sinusoidal voltage produced by the source is $10\ \text{V}$ and the output resistance of source is $50\ \Omega$. Apply a relevant op-amp circuit such that the $12\ \Omega$ resistive load ideally receives approximately $10\ \text{V}$ peak sinusoidal voltage drop across it. State the necessary circuit requirements. [5]

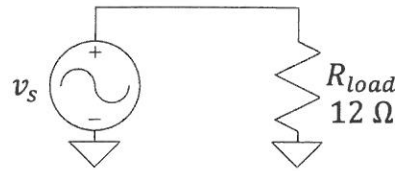


Figure-Q6(a)

- b. Figure-Q6(b) shows a widely used op-amp circuit that eliminates output signal chattering. The upper and lower threshold levels (UTL & LTL) of the circuit is respectively given by,

$$UTL = V_{ref} \left(\frac{R_1}{R_2} + 1 \right) - \frac{R_1}{R_2} V_{out(min)}$$

$$LTL = V_{ref} \left(\frac{R_1}{R_2} + 1 \right) - \frac{R_1}{R_2} V_{out(max)}$$

Where V_{ref} is the reference voltage of the circuit, $V_{out(max)}$ and $V_{out(min)}$ are the saturated voltages of the op-amp.

Illustrate the voltage transfer diagram of the op-amp circuit by assume ideal op-amp operation. [10]

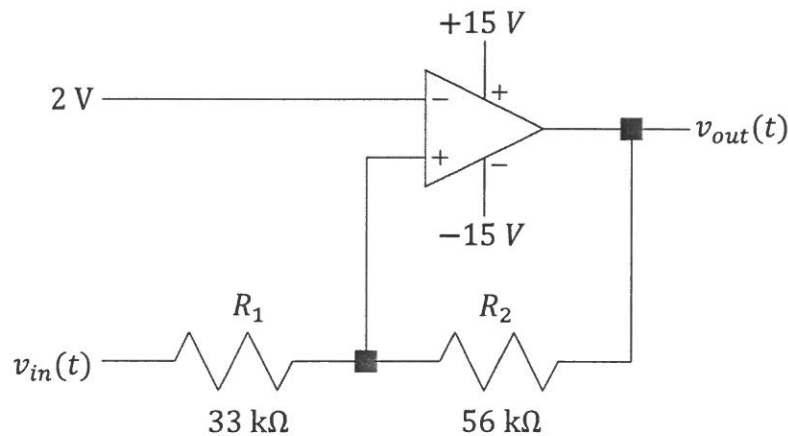


Figure-Q6(b)

- c. Figure-Q6(c) shows a circuit to be used as a simple audio amplifier. The amplifier circuit is to exhibit a mid-band voltage gain (v_{out}/v_{in}) of $9\ \text{dB}$.

Evaluate the needed transconductance (g_m) for the Q_1 n-channel MOSFET. State any assumption made in your evaluation. [10]

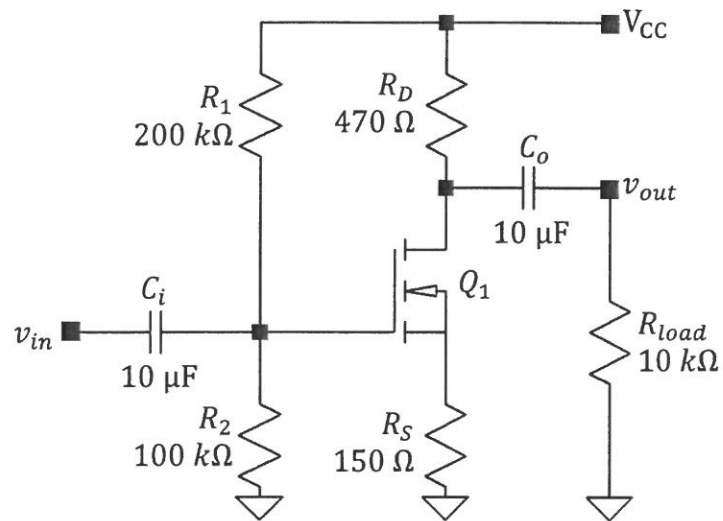


Figure-Q6(c)

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