INTI
International College Penang

FINAL
Examination Paper

(COVER PAGE)

Session	:	**April 2019**
Programme	:	Diploma in Electrical and Electronic Engineering (DEEI)
Course	:	**EEE 1105: Circuit Theory & Electronic Devices**
Date of Examination	:	25 July 2019 (Thursday)
Time	:	11:00am – 1:00pm Reading Time : Nil
Duration	:	2 Hours
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL

Materials permitted :

Non-Programmable Scientific Calculator

Materials provided :

Graph Paper (A4 size)

Examiner(s)	:	**Mr. Steven Khoo Boo Tap**
Moderator	:	Prof. Ir. Dr. Mandeep Singh

*This paper consists of **11** printed pages, including the cover page.*

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE1105: CIRCUIT THEORY & ELECTRONIC DEVICES
FINAL EXAMINATION: APRIL 2019 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

(a) Compute the current passing through 40Ω resistor as shown in Figure 1(a). (7 marks)

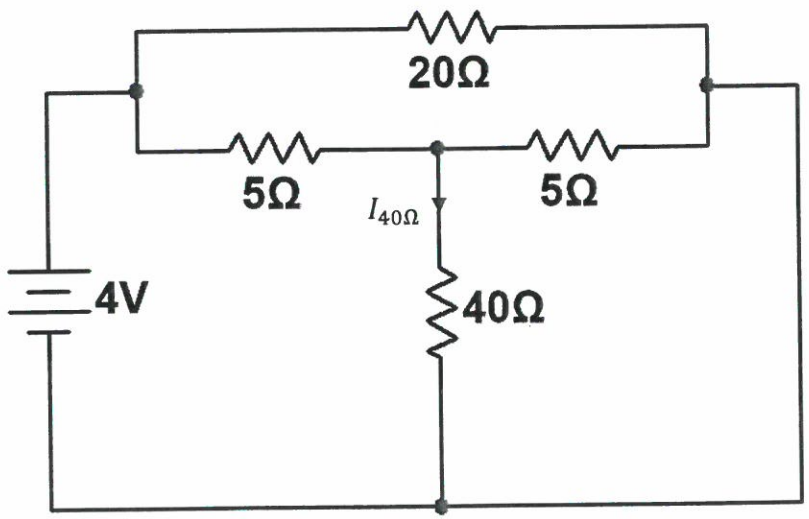

Figure 1(a)

(b) A network is arranged as shown in Figure 1(b). Compute the value of the current passing flowing through 5Ω resistor with clear working using the:-

(i) Nodal analysis. (9 marks)

(ii) Mesh analysis. (9 marks)

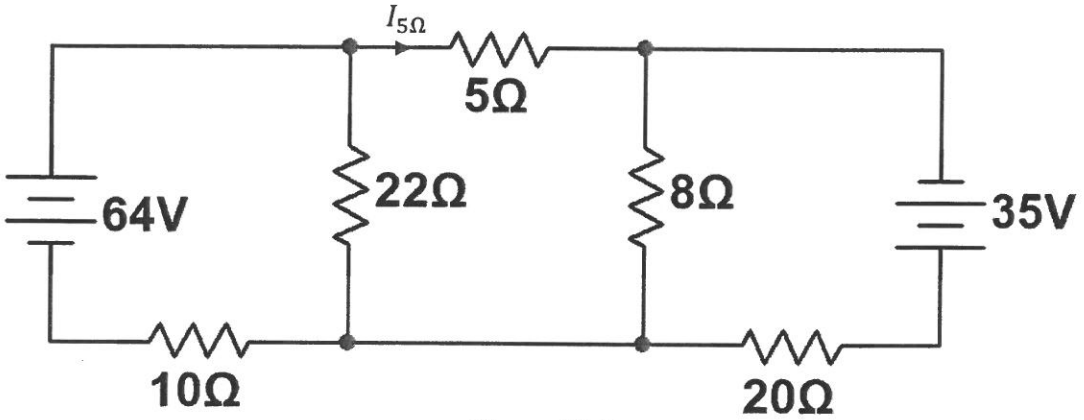

Figure 1(b)

Question 2

(a) A circuit as shown in Figure 2(a) is connected across a $250\angle 0°V, 60Hz$ supply. Compute the:-

(i) Total impedance.

(4 marks)

(ii) Total current and the current passing through each components.

(5 marks)

(iii) Voltages across R, C and L.

(4 marks)

Express all answers in Polar form.

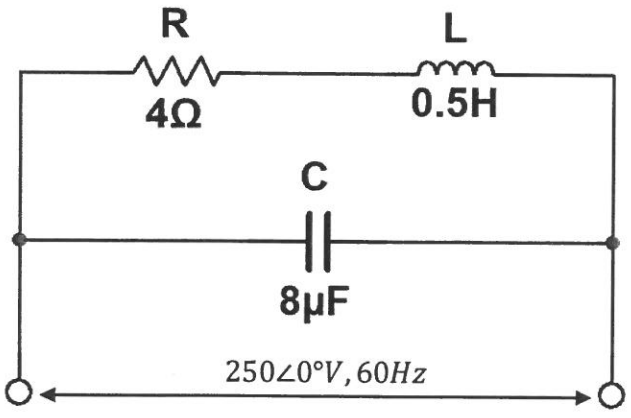

Figure 2(a)

(b) A circuit is arranged as shown in Figure 2(b). Compute the:-

(i) Resistance R_T (equivalent resistance "seen" by the voltage source V_1). (6 marks)

(ii) Current I_7 (the current that flows through resistor R_7). (2 marks)

(iii) Current I_2 (the current that flows through resistor R_2). (4 marks)

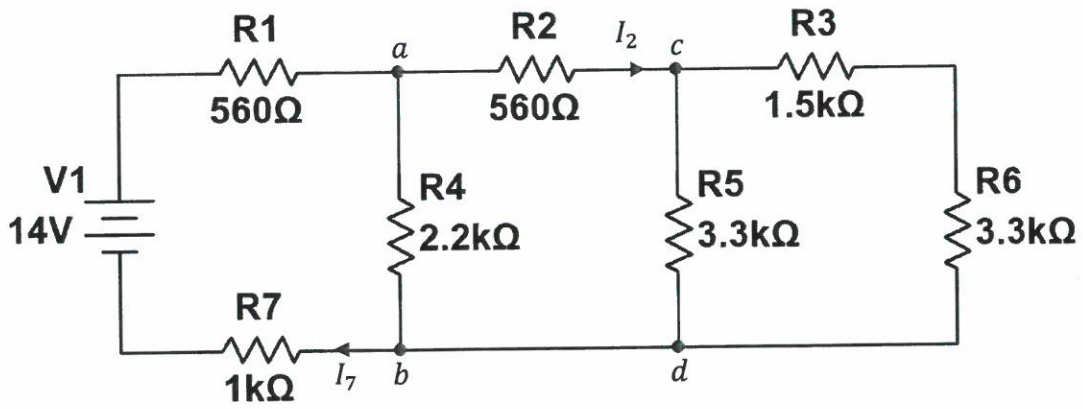

Figure 2(b)

Question 3

(a) The circuit shown in Figure 3(a) contains a non-ideal diode that has $V_{D(on)} = 1.5V$. Find the power absorbed by the diode. (7 marks)

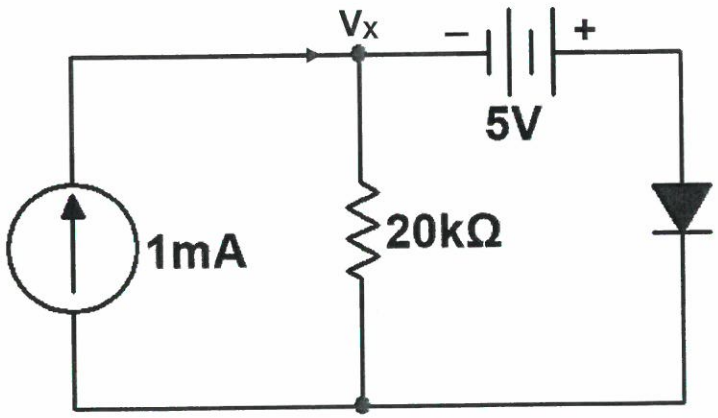

Figure 3(a)

(b) Determine I, V_1, V_2 and V_0 for the series dc configuration of Figure 3(b). Show the working clearly.

(7 marks)

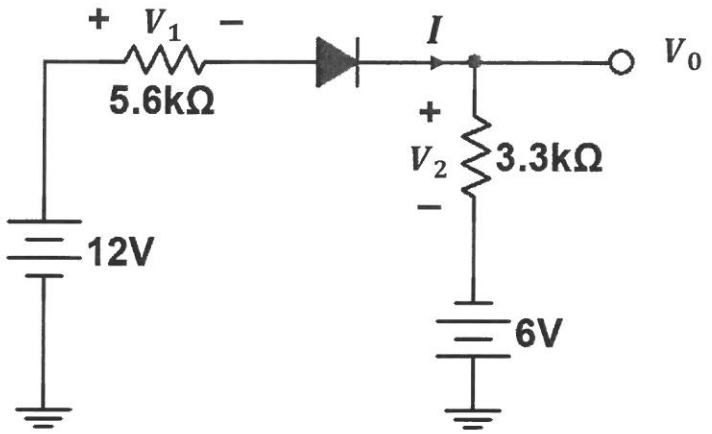

Figure 3(b)

(c) For the Zener diode network of Figure 3(c), calculate the:-

(i) Voltages at references V_1 and V_2.

(4 marks)

(ii) Current through blue LED and the power delivered by the supply. Assume that the blue LED has a forward voltage of 2.8V.

(3 marks)

(iii) Power absorbed by the blue LED compare to the 3.3V Zener diode.

(4 marks)

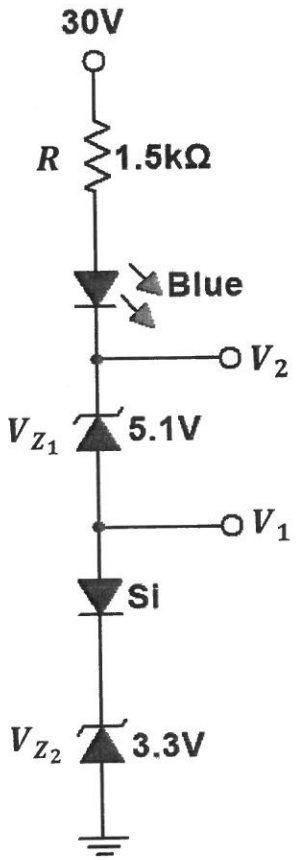

Figure 3(c)

Question 4

(a) Find the common-emitter forward-current amplification, β_{ac} for the transistor characteristics of Figure 4(a) at $I_C = 7\ mA$ and $V_{CE} = 5\ V$.

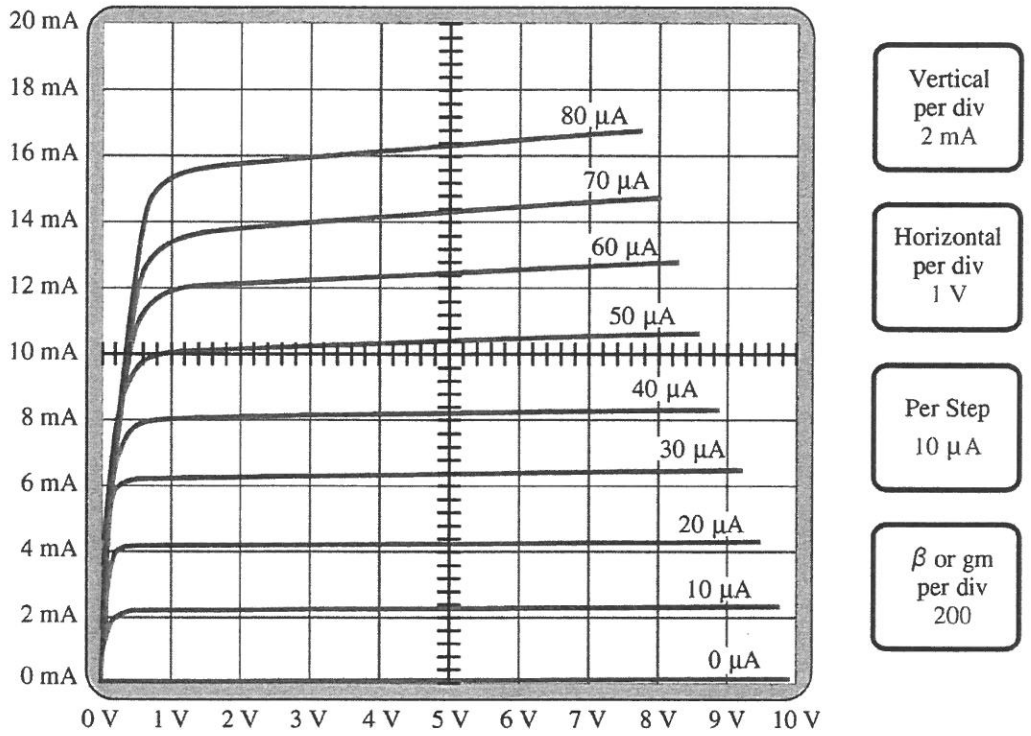

Figure 4(a)

(6 marks)

(b) For the fixed-bias configuration network as shown in Figure 4(b) with the $\beta = 50$, calculate:

(i) I_{B_Q} and I_{C_Q}.

(3 marks)

(ii) V_{CE_Q}.

(2 marks)

(iii) V_C, V_B and V_E.

(3 marks)

(iv) V_{BC}.

(2 marks)

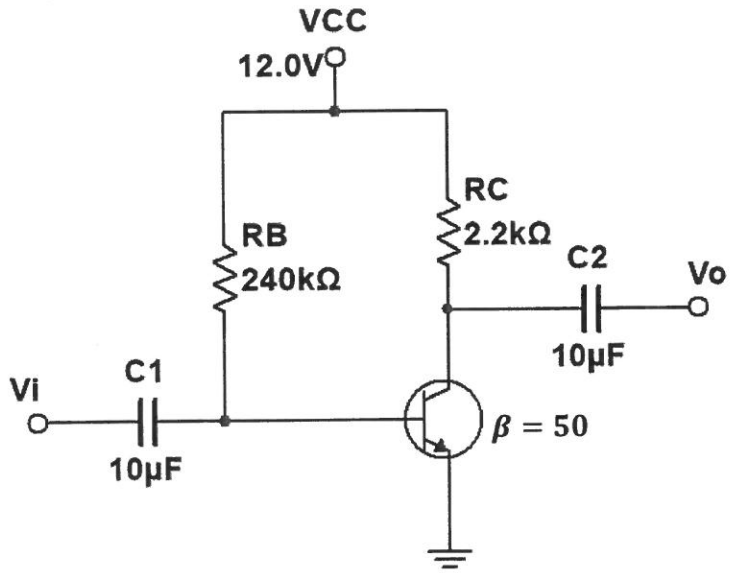

Figure 4(b)

(c) Determine the dc bias voltage, V_{CE} and the current, I_C for the voltage-divider configuration in Figure 4(c). Assume $V_{BE} = 0.7$ V and $\beta = 100$.

(9 marks)

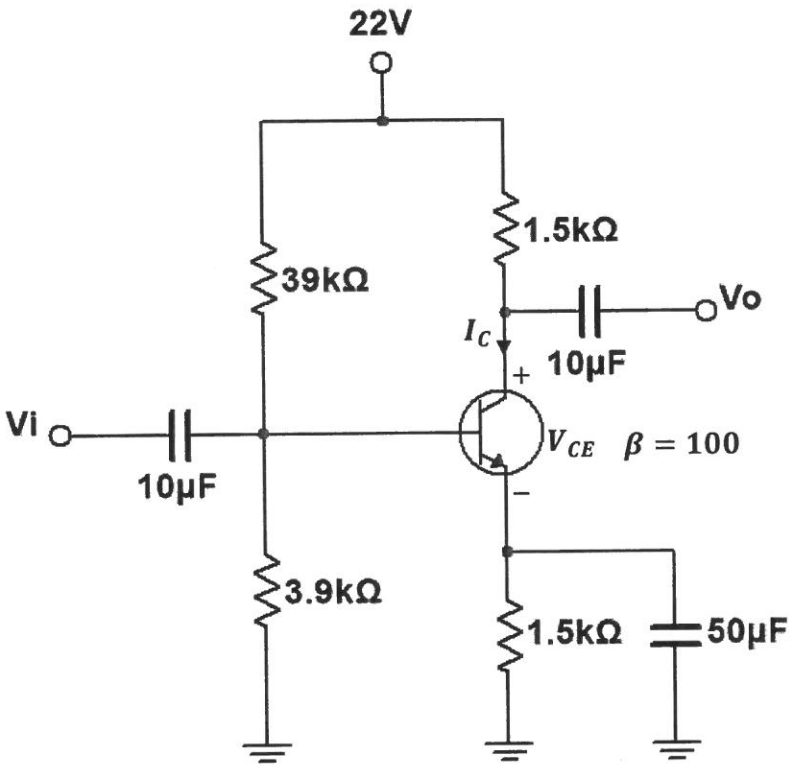

Figure 4(c)

Question 5

(a) Compute a value for the capacitor, C and the total impedance in polar form as shown in Figure 5(a). Assume that the voltage supply, V_S is $220\angle 0°\ V$, 60 Hz. The total current is given as $11.81\angle -7.12°\ A$.

(8 marks)

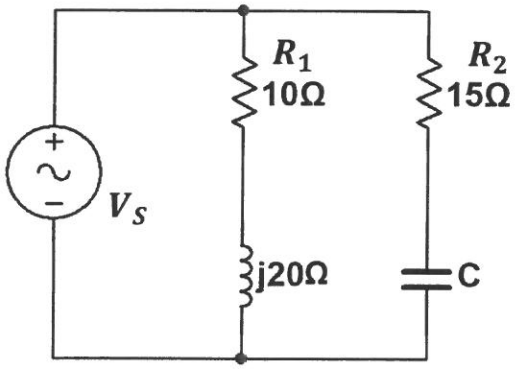

Figure 5(a)

(b) Figure 5(b) illustrates a self-biased configuration of Field Effect Transistor (FET) circuit.

(i) Determine I_{DQ} and V_{GSQ}.

(2 marks)

(ii) Given that the Shockley's equation is $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$, determine V_{DS}, V_D, V_G and V_S.

(5 marks)

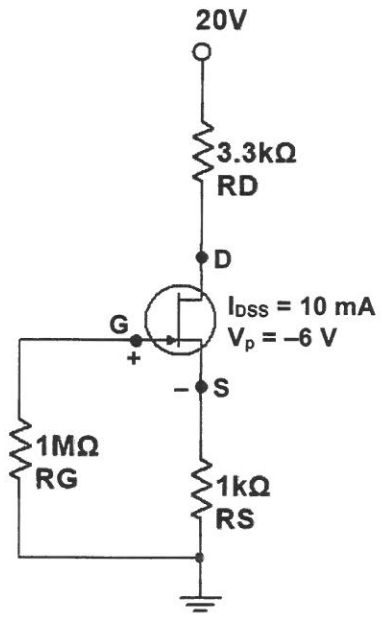

Figure 5(b)

(c) For the JFET biasing network shown in Figure 5(c), calculate:

(i) the I_{DQ} and V_{GSQ};

(6 marks)

(ii) the V_{DS} and V_{DG}.

(4 marks)

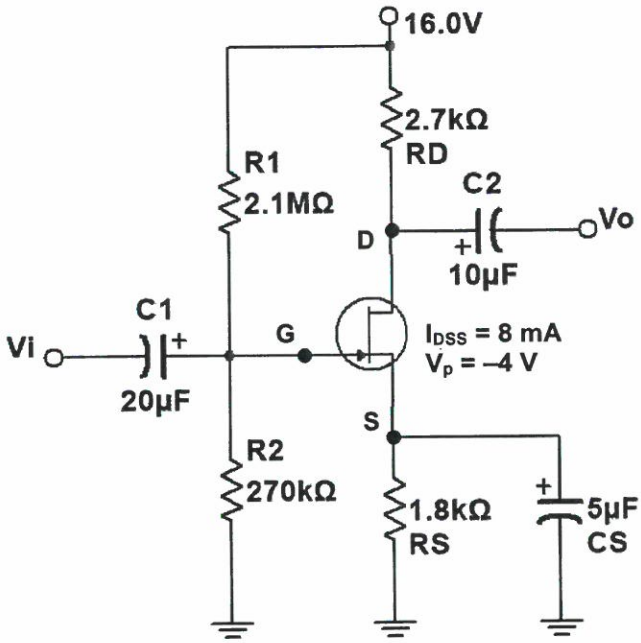

Figure 5(c)

Question 6

(a) Compute the voltage drops across all components in the circuit in Figure 6(a), expressing them in complex (polar) form with magnitudes and phase angles each.

(6 marks)

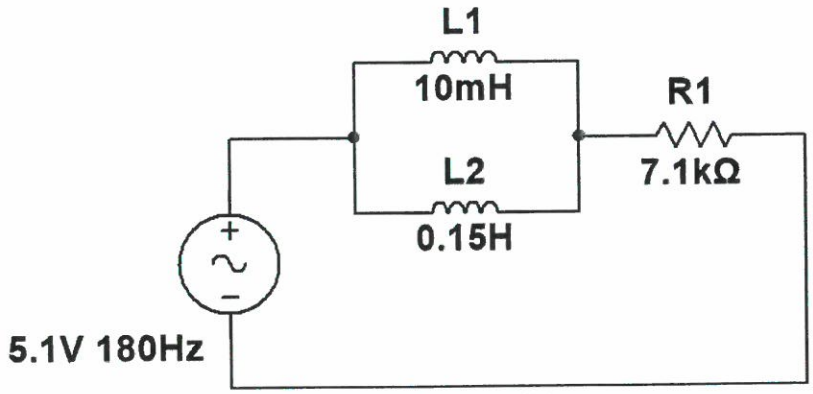

Figure 6(a)

(b) A circuit in Figure 6(b) shows the alternating currents (AC) circuit for certain application with the given V_S as $250\angle 0°\ V, 50Hz$ supply connected across terminal **X** and terminal **Z**. Given:
$Z_1 = R_1 + jX_{L1} = 3 + j4\Omega,\ \ Z_2 = R_2 + jX_{L2} = 5 + j5\Omega,\ \ Z_3 = R_3 - jX_{C2} = 5 - j10\Omega$

(i) Draw the equivalent electrical circuit diagram for Figure 6(b).

(2 marks)

(ii) Find the total impedance, Z_T that is "seen" by the voltage source. Express the answer in Polar form.

(5 marks)

(iii) Compute the current passing through each components. Express the answer in Polar form.

(3 marks)

(iv) Compute the voltage across each components. Express the answer in Polar form.

(6 marks)

(v) Find the power factor and state the circuit is "lagging" or "leading".

(3 marks)

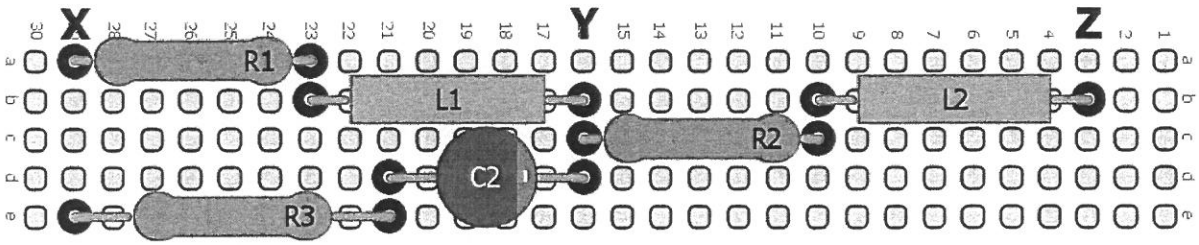

Figure 6(b)

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