INTI
International College Penang

FINAL
Examination Paper

(COVER PAGE)

Session	:	**April 2018**
Programmes	:	Diploma in Electrical and Electronic Engineering (DEEI)
Course	:	**EEE1106: Analogue Electronics**
Date of Examination	:	28 July 2018 (Saturday)
Time	:	11:00am – 1:00pm
Duration	:	2 Hours Reading Time Nil

Special Instructions :

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL BY THE STUDENTS.

Materials Permitted :

Non-programmable Calculator (e.g. Model fx570 Series)

Materials Provided :

Semilog graph paper

Examiner(s)	:	**Chan Tse Wei**
Moderator	:	Assoc. Prof. Dr. Khoo Bee Ee

*This paper consists of **8** printed pages, including the cover page.*

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE1106: ANALOGUE ELECTRONICS
FINAL EXAMINATIONS: APRIL 2018 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks. The marks allocated to each sub-question are shown in square brackets at the right-hand margin. Present your answers neatly and clearly. The assessor reserves the rights to ignore your answers if they are ambiguous.

Question 1

a. Figure-Q1(a) shows a complete AC equivalent circuit model of a small signal voltage amplifier. C_1 and C_2 are coupling capacitors, while C_3 is the decoupling capacitor. C_{bc} and C_{be} are parasitic capacitance of the transistor used in the amplifier. C_W models the wiring capacitance at the output stage. The wiring capacitance at the input stage is negligible.

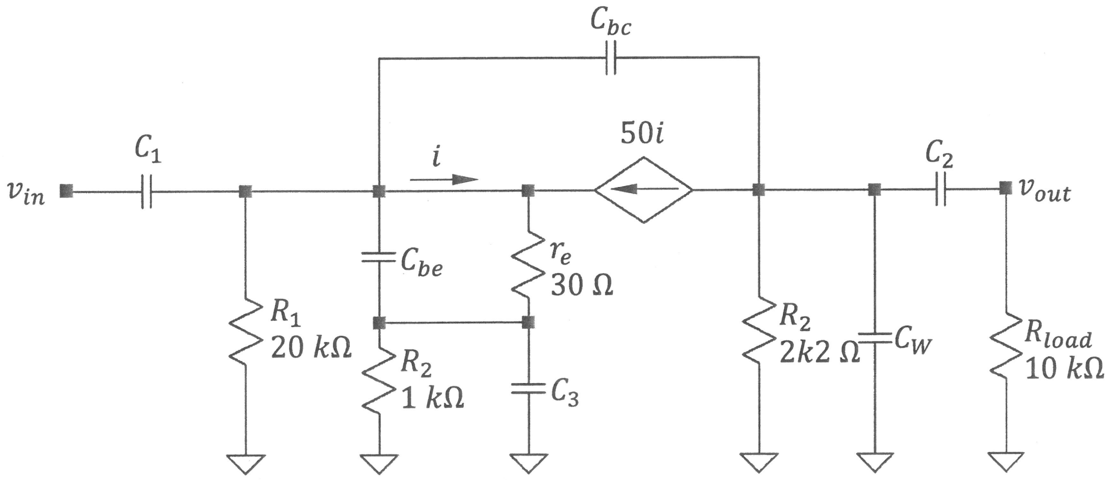

Figure-Q1(a)

i. Based on the circuit given in Figure-Q1(a), redraw a simplified circuit model for low frequency analysis. [3]

ii. Based on the circuit given in Figure-Q1(a), redraw a simplified circuit model for high frequency analysis. [3]

iii. Based on the circuit given in Figure-Q1(a), calculate the voltage amplifier mid-band gain. [4]

b. i. Calculate the input resistance of the circuit in Figure-Q1(b) as seen by the input voltage V_{in}. [5]

ii. If resistors R_1 and R_2 in Figure-Q1(b) remain unchanged, while resistor R_3 is replaced by a capacitor having capacitance C Farad, examine the effect of an increment in input frequency towards the circuit's input impedance. [5]

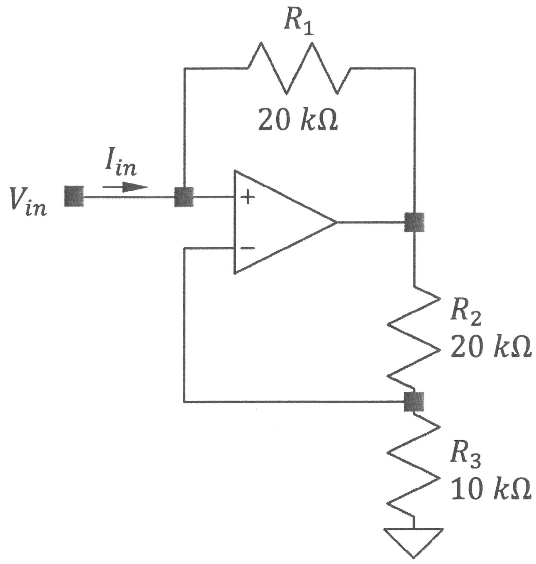

Figure-Q1(b)

c. Explain the difference between harmonic oscillators and relaxation oscillators and their similarity. [5]

Question 2

a. With the aid of a diagram, explain crossover distortion which is found in basic class B power amplifier operations. [5]

b. The voltage transfer function of an active filter is given by,

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{a_1 s}{s^2 + b_1 s + b_0}$$

Quantitatively show that the maximum voltage gain magnitude of this filter is given by,

$$\left|\frac{V_{out}}{V_{in}}\right| = \frac{a_1}{b_1}$$ [10]

c. Figure-Q2(c) shows a Wien Bridge oscillator circuit. R_t is a thermistor which reduces its resistance when the voltage drop across it increases.

i. Calculate the range of oscillating frequency when the 10 $k\Omega$ variable resistor is adjusted between its extreme ends. [5]

ii. Calculate the resistance of R_t to sustain output oscillation when the variable resistor is adjusted to 2 $k\Omega$. [5]

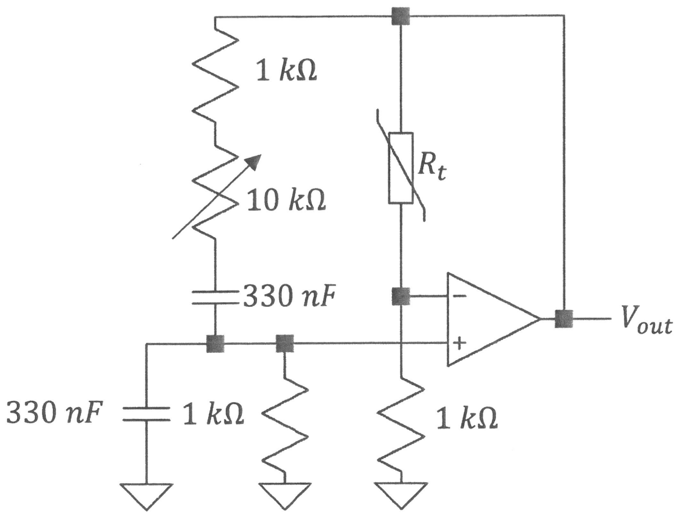

Figure-Q2(c)

Question 3

a. Figure-Q3(a) shows the ideal AC load line of a series-fed class-A power amplifier, associated with its Q-point, drawn on its output IV characteristics graph. Quantitatively show that its theoretical maximum power efficiency is 17.5% [10]

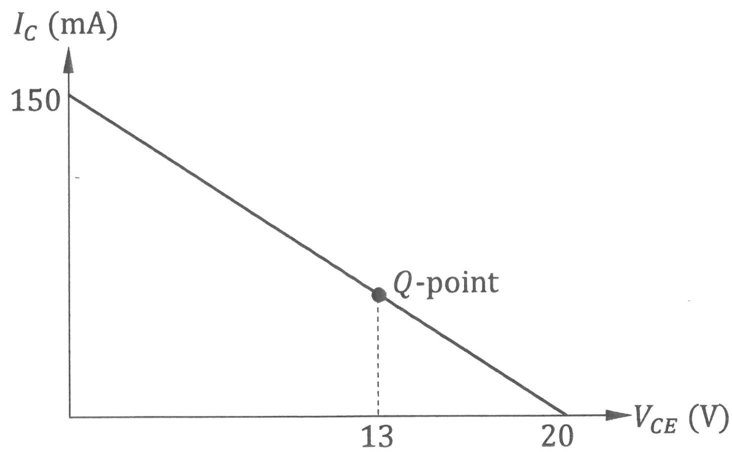

Figure-Q3(a)

b. Explain the identification of second order filter type from its voltage transfer function expressed in the s-domain. [5]

c. Figure-Q3(c) shows a relaxation oscillator implemented using a 555 timer. Sketch the synchronized timing diagrams of the voltages across capacitor C_1 and V_{out}. Clearly label the sketches with timings and voltage levels. [10]

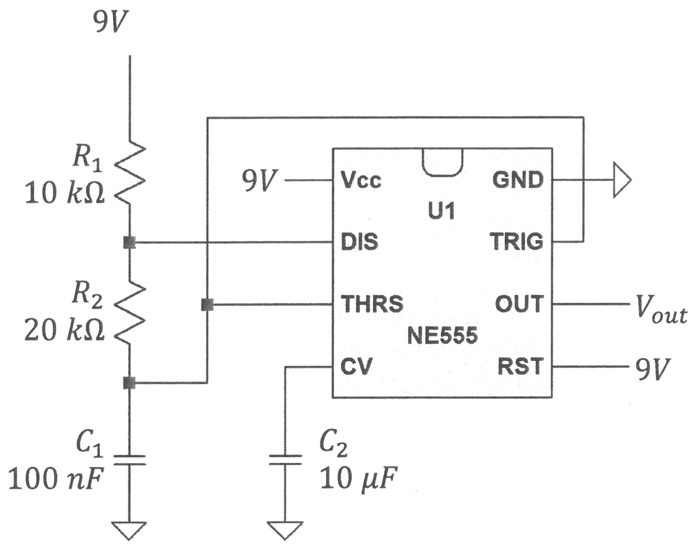

Figure-Q3(c)

Question 4

a. Explain two differences between the inverting and non-inverting amplifiers implemented using op-amps, in terms of their operations. [5]

b. Figure-Q4(b) shows a basic complementary pair push-pull power amplifier. Assume ideal transistor operation, determine

i. the maximum input power drawn from the supply voltage, [4]

ii. the maximum output power, and [4]

iii. the power dissipation of each transistor during maximum output. [2]

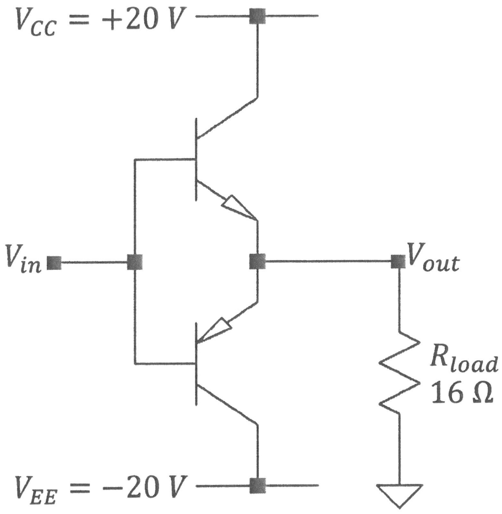

Figure-Q4(b)

c. Figure-Q4(c) shows an audio amplifier circuit. Transistor J_1 exhibits a transconductance (g_m) of 1.2 mS based on the biasing resistances and its static characteristics. Determine the lower cutoff frequency of the audio amplifier circuit. [10]

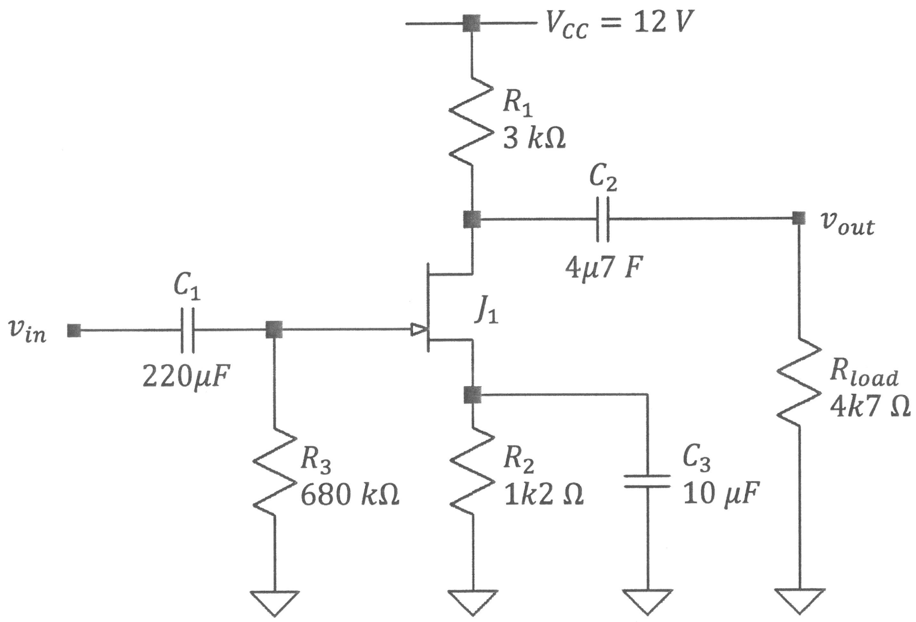

Figure-Q4(c)

Question 5

a. Two voltage amplifiers which respectively have voltage gain of 40 and -55 are cascaded together. Convert their voltage to dB unit and thus find the system's overall voltage gain. [5]

b. Figure-Q5(b) shows a modified Schmitt triggered comparator. m and n are ratios of R_3 to R_1 and R_2 to R_1 respectively. Assume that the op-amp is ideal, quantitatively show that the circuit allows independent adjustment of the center voltage (V_{ctr}) and the hysteresis voltage (V_H), where,

$$V_{ctr} = \frac{UTP + LTP}{2}$$

$$V_H = UTP - LTP$$

UTP = upper threshold point

LTP = lower threshold point [10]

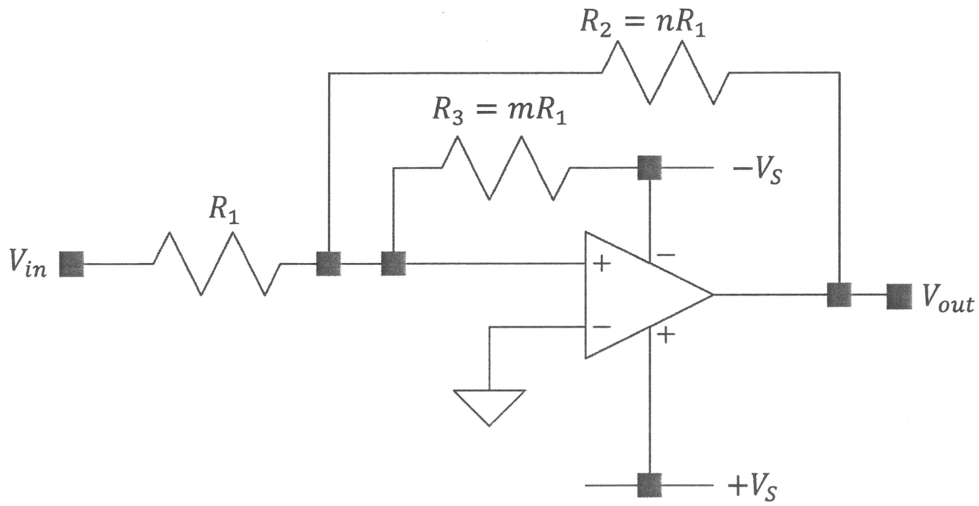

Figure-Q5(b)

c. Figure-Q5(c) shows a Sallen-Key low pass filter. Calculate its upper cutoff frequency in Hz. [10]

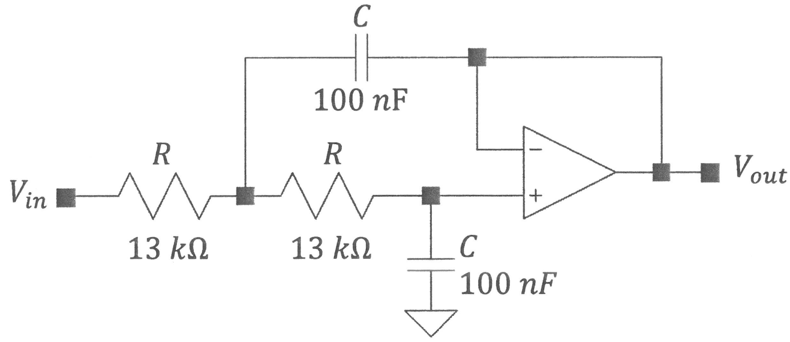

Figure-Q5(c)

Question 6

a. Table-Q6(a) shows the test results of a small signal voltage amplifier when it is being tested.

f (kHz)	0.05	0.08	0.10	0.20	0.50	0.80	1.00	2.00	5.00	8.00	10.00	20.00	50.00	80.00
A_v	2.21	3.50	4.34	8.15	15.05	17.72	18.57	19.84	19.75	18.91	18.20	14.30	7.45	4.86

Table-Q6(a)

i. Plot the frequency response of the small signal voltage amplifier based on the results shown. [5]

ii. Determine the bandwidth of the voltage amplifier. [5]

b. Theoretically produce an electronic circuit that fulfills the input-output relationship shown in Figure-Q6(b). Clearly state the needed passive component values used in the electronic circuit. [5]

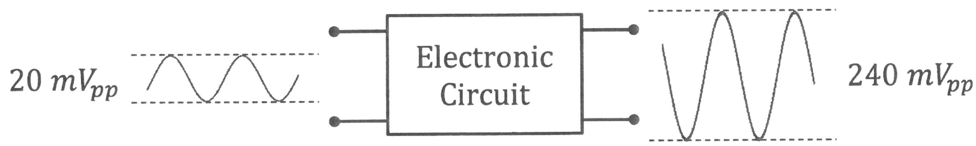

Figure-Q6(b)

c. An op-amp has the following specifications:

Maximum power supply voltage: ±18 V

Differential input voltage: 36 V

Input voltage: 36 V

Large signal voltage gain: 100 V/mV

Slew rate = 0.7 V/μs

This op-amp is used to implement a non-inverting amplifier with a voltage gain of 50. A sinusoidal voltage of 0.6 V peak-to-peak at 8 kHz is applied to this amplifier. Theoretically examine if this op-amp is suitable for such implementation. [10]

~ The End ~