INTI
International College Penang

FINAL
Examination Paper

(COVER PAGE)

Session	:	**April 2018**
Programme	:	Diploma in Electrical and Electronic Engineering (DEEI)
Course	:	**EEE 1105: Circuit Theory & Electronic Devices**
Date of Examination	:	26 July 2018 (Thursday)
Time	:	11:00am – 1:00pm Reading Time : Nil
Duration	:	2 Hours
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL

Materials permitted :

Non-Programmable Scientific Calculator

Materials provided :

Worksheet 5(a) & Graph Paper (A4 size)

Examiner(s)	:	**Mr. Steven Khoo Boo Tap**
Moderator	:	Dr. Ooi Beng Lee

*This paper consists of **11** printed pages, including the cover page.*

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE1105: CIRCUIT THEORY & ELECTRONIC DEVICES
FINAL EXAMINATION: APRIL 2018 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

(a) For the network shown in Figure 1(a), compute the total resistance, R_T of the circuit. Also, compute I_1 and I_2 and V_{R_6} in Figure 1(a).

(9 marks)

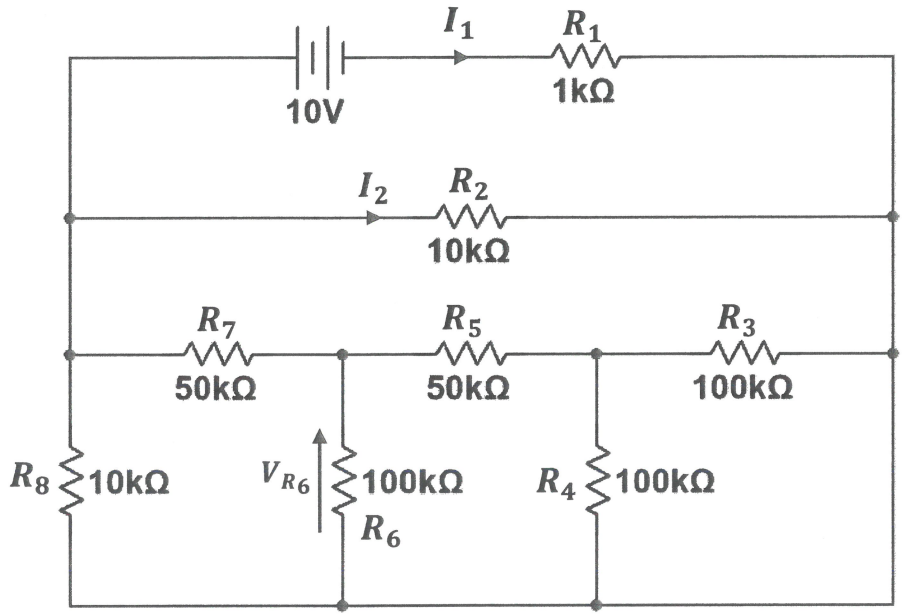

Figure 1(a)

(b) A network is arranged as shown in Figure 1(b). Compute the value of the current in the 10Ω resistor with clear working using:

(i) the Nodal analysis.

(8 marks)

(ii) the Mesh analysis.

(8 marks)

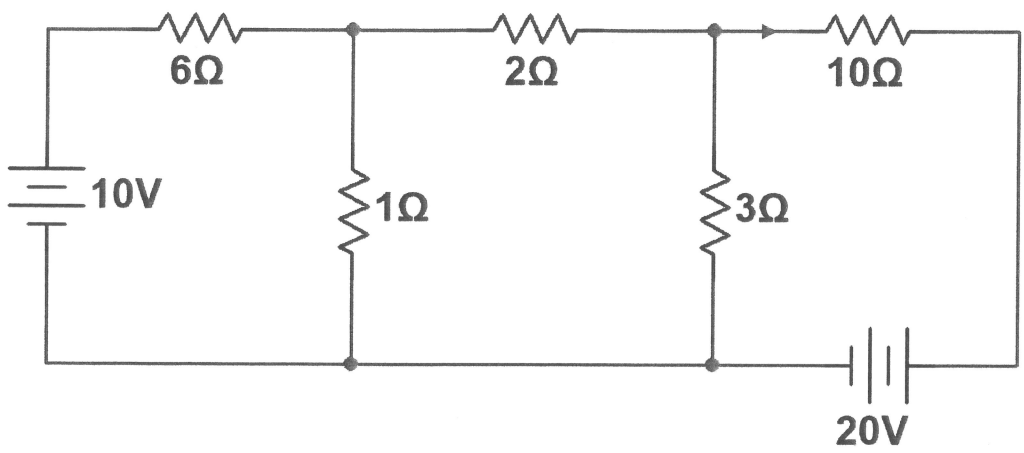

Figure 1(b)

Question 2

(a) A circuit as shown in Figure 2(a) having a resistance of 0.2kΩ, an inductance of 500mH and a capacitance of 0.02mF in series, is connected across a 80∠0°V, 0.06kHz supply. Compute:

(i) the impedance;

(3 marks)

(ii) the current;

(2 marks)

(iii) the voltages across R, C and L;

(3 marks)

(iv) the power factor and phase angle.

(2 marks)

Sketch the phasor diagram of currents and voltage supply.

(2 marks)

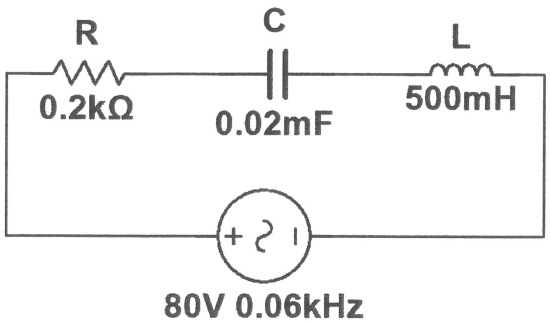

Figure 2(a)

(b) Find the voltage at each node and the current flowing through each resistor.

(13 marks)

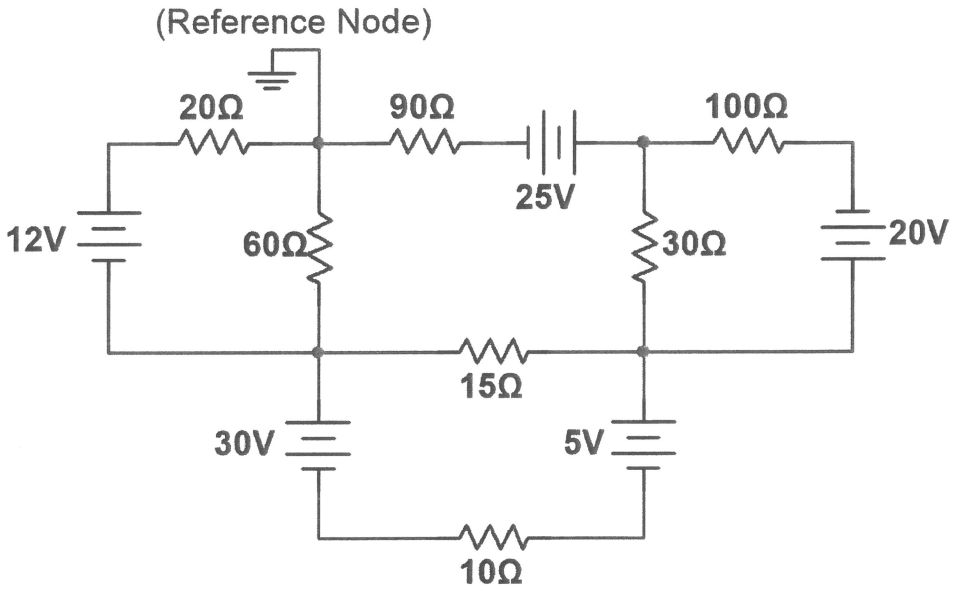

Figure 2(b)

Question 3

(a) Find the voltage drops across all components in the circuit in Figure 3(a), expressing them in complex (polar) form with magnitudes and phase angles each. Also, draw the equivalent electrical circuit diagram for Figure 3(a).

(6 marks)

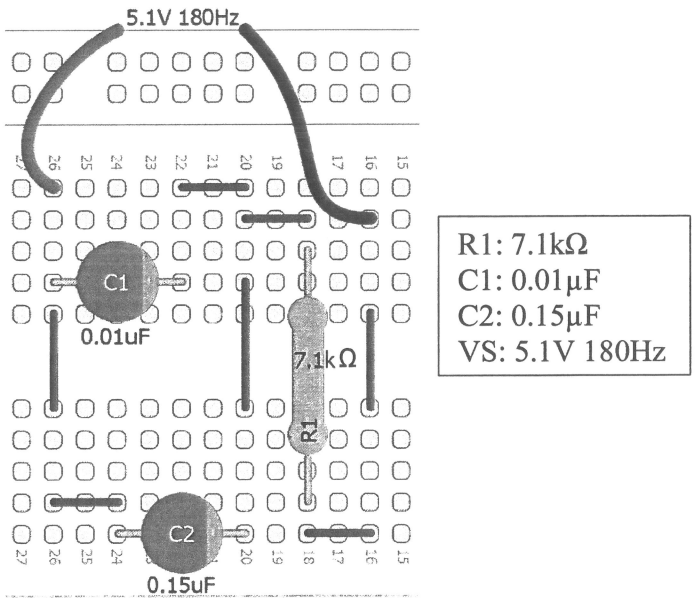

Figure 3(a)

(b) A circuit as shown in Figure 3(b) with the given V_S as $100\angle 0°\ V$ supply. Find:

(i) the total impedance, Z_T;

(3 marks)

(ii) the current, $I_{j8\Omega}$ and the voltage, V_{R_1};

(4 marks)

(iii) the power factor and the phase angle.

(2 marks)

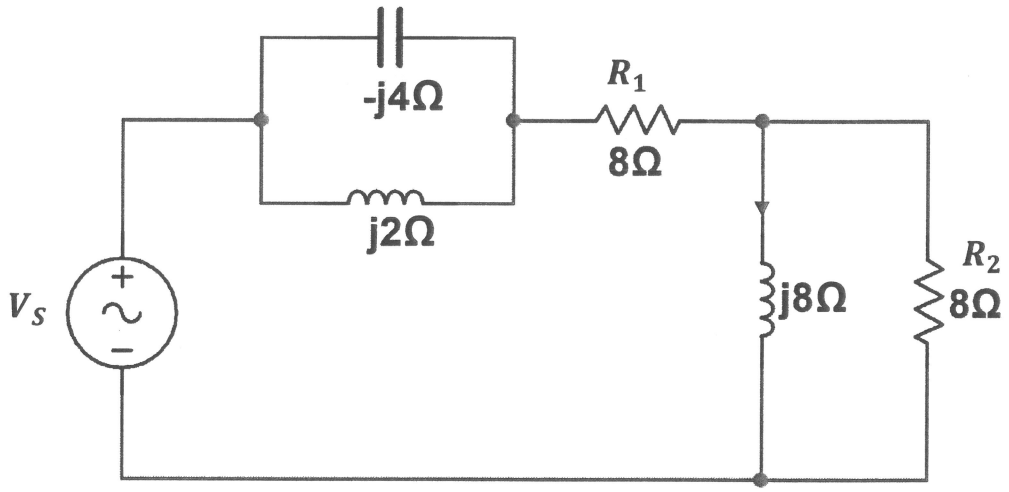

Figure 3(b)

(c) For the circuit shown in Figure 3(c), compute the current passing through each element. Sketch a phasor diagram showing all the currents. Assume the supply current, I_S is $33\angle -13°\ A$, 50Hz.

(10 marks)

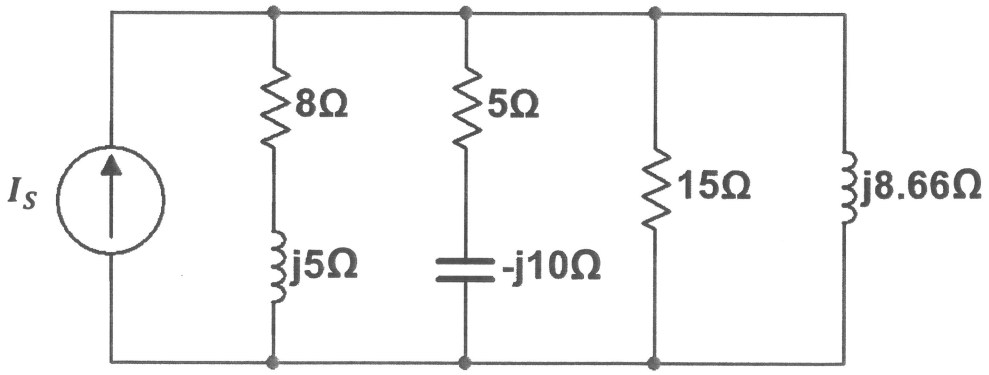

Figure 3(c)

Question 4

(a) Determine I, V_1, V_2 and V_0 for the series dc configuration of Figure 4(a). Show the working clearly.

(7 marks)

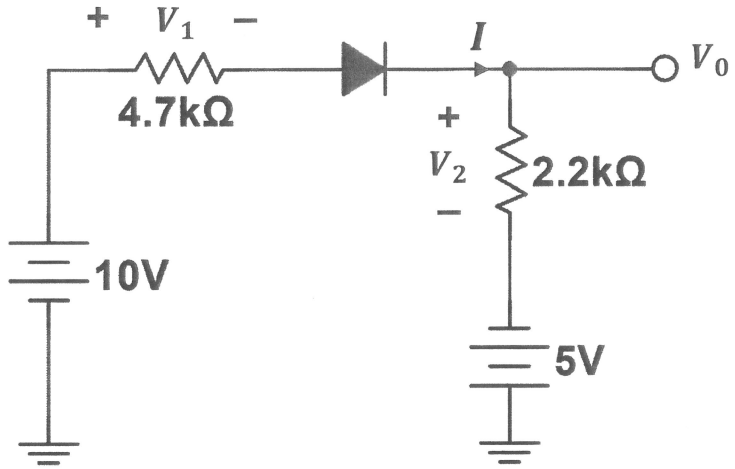

Figure 4(a)

(b) Determine V_0, I_D, I_{D1} and I_{D2} for the parallel diode configuration of Figure 4(b). Explain the purpose of an additional diode, D_2 that is placed in parallel for Figure 4(b). Assume that both diodes are having similar characteristics.

(7 marks)

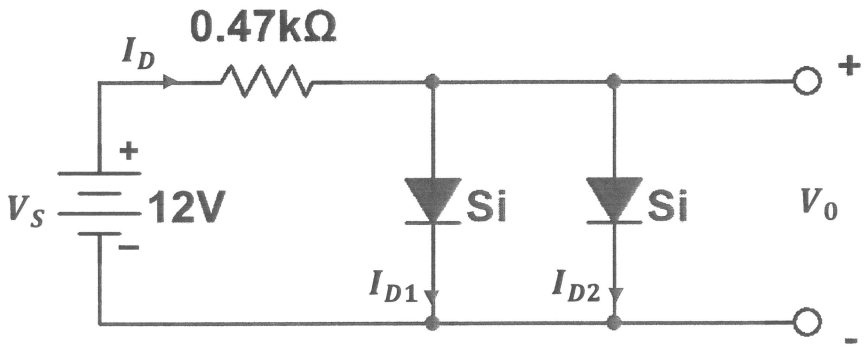

Figure 4(b)

(c) For the Zener diode network of Figure 4(c), determine:

(i) the voltages at references V_1 and V_2.

(4 marks)

(ii) the current through white LED and the power delivered by the supply. Assume that the white LED has a forward voltage of 3.5V.

(3 marks)

(iii) the power absorbed by the white LED compare to the 3.3V Zener diode.

(4 marks)

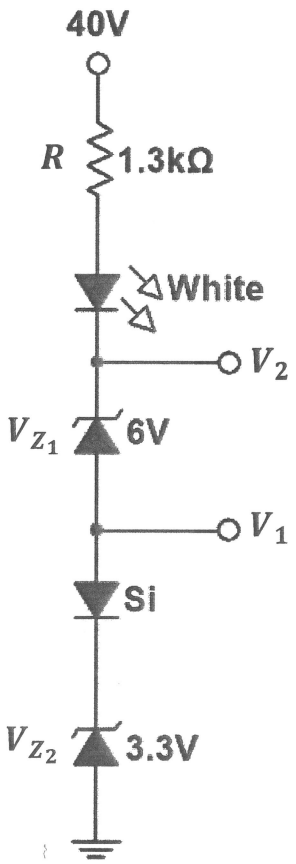

Figure 4(c)

Question 5

(a) Figure 5(a)(i) shows the transistor circuit and Figure 5(a)(ii) shows the device characteristics.

(i) Sketch the load line for the network of Figure 5(a)(i) on the characteristics for the transistor appearing in Figure 5(a)(ii).

(5 marks)

(ii) Find the values of I_{C_Q} and V_{CE_Q} with a base current of $30\mu A$.

(3 marks)

(iii) Determine the dc beta at the Q-point.

(2 marks)

(iv) Using the beta for the network determined in part (iii), calculate the required value of R_B and suggest a possible standard value.

(5 marks)

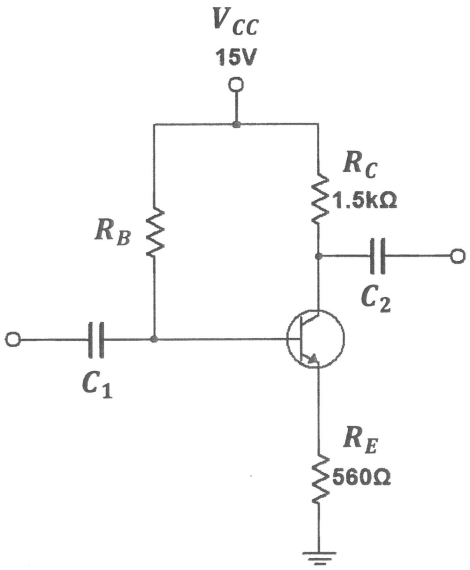

Figure 5(a)(i)

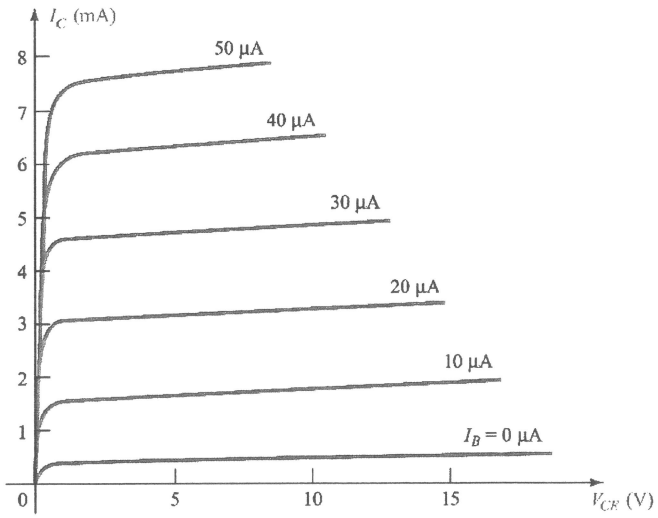

Figure 5(a)(ii)

Note: Use **Worksheet 5(a)** to answer Question 5(a)(i), detach Worksheet 5(a) and tie with the answer booklet.

(b) For the emitter-bias network of Figure 5(b) with the $\beta = 50$, determine:

(i) I_B and I_C.

(3 marks)

(ii) V_{CE}.

(2 marks)

(iii) V_C, V_E and V_B.

(3 marks)

(iv) V_{BC}.

(2 marks)

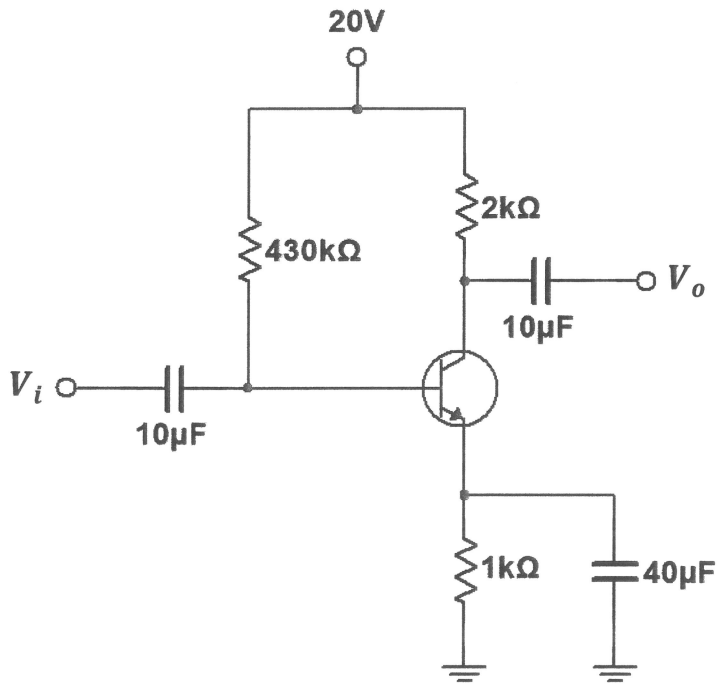

Figure 5(b)

Question 6

(a) Find value of **C** in the circuit shown in Figure 6(a). Assume that the voltage supply, V_S is $220\angle 0°\ V$, 60 Hz. The total current is given as $11.81\angle -7.12°\ A$. Also, find the total impedance in polar form.

(8 marks)

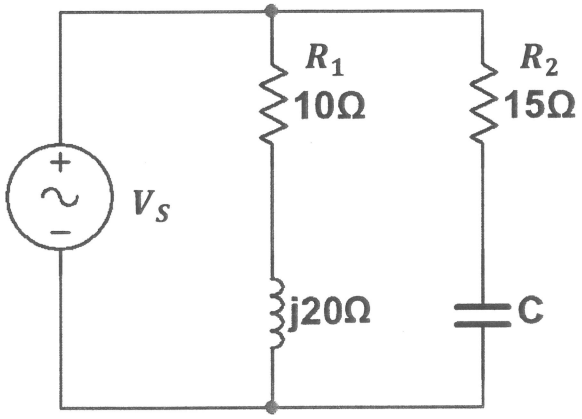

Figure 6(a)

(b) By using Mathematical approach, determine V_{GSQ} and I_{DQ} for the circuit of Figure 6(b). Show that Graphical approach can be used to estimate the I_{DQ} with resulting Shockley curve.

(7 marks)

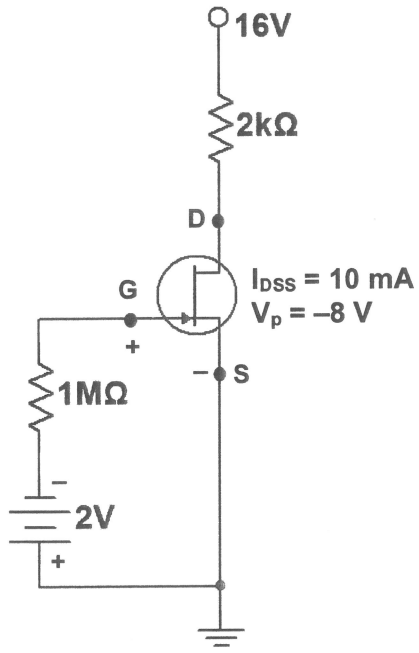

Figure 6(b)

(c) For the JFET biasing network in Figure 6(c), determine:

(i) the I_{DQ} and V_{GSQ};

(6 marks)

(ii) the V_{DS} and V_{DG}.

(4 marks)

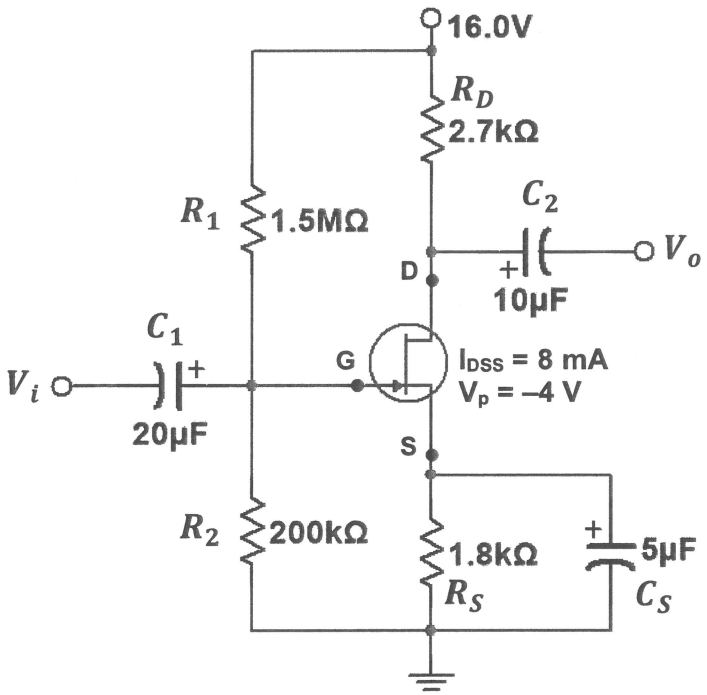

Figure 6(c)

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EEE1105(F)/Apr18/Steven Khoo/10/04/18

Worksheet 5(a)

(a) Figure 5(a)(i) shows the transistor circuit and Figure 5(a)(ii) shows the device characteristics.

(i) Draw the load line for the network of Figure 5(a)(i) on the characteristics for the transistor appearing in Figure 5(a)(ii).

(5 marks)

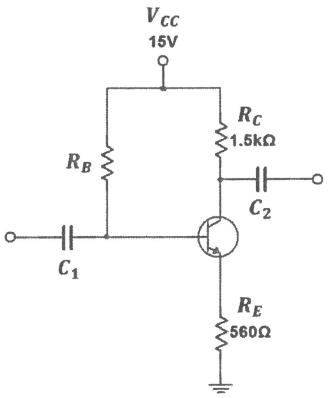

Figure 5(a)(i)

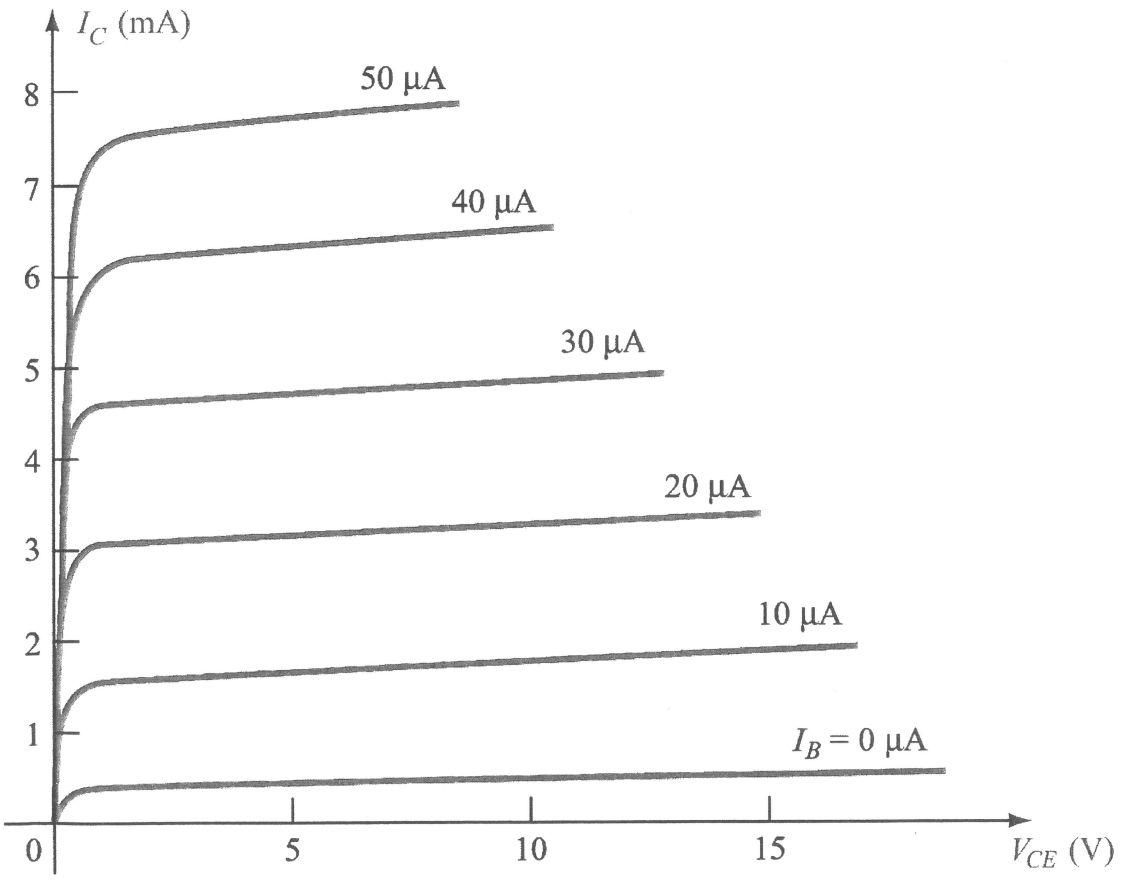

Figure 5(a)(ii)