INTI
International College Penang
LAUREATE INTERNATIONAL UNIVERSITIES*

FINAL
Examination Paper

(COVER PAGE)

Session	:	**APRIL 2016**
Programmes	:	Diploma in Electrical and Electronic Engineering (DEEI)
Course	:	**EEE2112: Introduction to Power Electronics & Drives**
Date of Examination	:	25 July 2016, Monday
Time	:	11.00am – 1.00pm
Duration	:	2 Hours Reading Time : Nil
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL BY THE STUDENTS.

Materials Permitted :
Scientific Calculator (Model fx570 Series)

Materials Provided :
NIL

Examiner(s)	:	**Chan Tse Wei**
Moderator	:	Dr. Ooi Beng Lee

*This paper consists of **8** printed pages, including the cover page.*

INTI INTERNATIONAL COLLEGE

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING (DEEI)
EEE2112: INTRODUCTION TO POWER ELECTRONICS AND DRIVES
FINAL EXAMINATIONS: APRIL 2016 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks. The marks allocated to each sub-question are shown in square brackets at the right-hand margin. The assessor reserves the rights to ignore your answers if they are ambiguous.

Question 1

a. Figure-Q1(a)(i) shows a circuit which utilizes a variable resistor to control power delivered to a resistive load, whereas Figure-Q1(a)(ii) shows a circuit utilizing a switching scheme to perform a similar function.

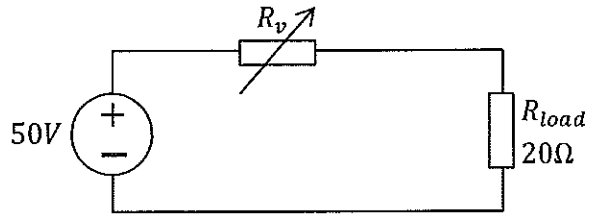


Figure-Q1(a)(i)

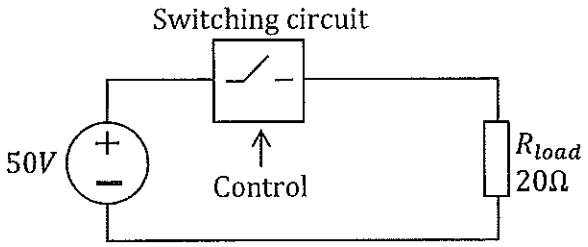


Figure-Q1(a)(ii)

i. Calculate the value of variable resistor R_v in Figure-Q1(a)(i) so that 2W of power is delivered to the 20Ω load. [4]

ii. Calculate the efficiency of the circuit in Figure-Q1(a)(i) base on the condition in part (a)(i). [4]

iii. Quantitatively determine the switching scheme needed to deliver 2W of power to the 20Ω load in Figure-Q1(a)(ii). [4]

iv. Calculate the efficiency of the circuit in Figure-Q1(a)(ii) assuming the switching mechanism is ideal. [2]

v. Between a power MOSFET and a silicon controlled rectifier (SCR), which one is more suitable to be used as the switching element in Figure-Q1(a)(ii)? Justify your answer. [5]

b. Sketch the timing diagrams of a diode current and its voltage characteristic during a recovery interval. Clearly show in the sketch, the reverse recovery time, t_{RR}, the reverse maximum current, I_{RM}, and the reverse recovery storage charge, Q_{RR}. [6]

Question 2

a. i. State one advantage and one disadvantage of power transistors as compared to thyristors in power electronic applications. [4]

ii. Explain the requirement(s) to drive a bipolar junction transistor (BJT) into saturation, and state the characteristic of a saturated BJT. [4]

iii. Draw the large signal DC operation model of a power NPN transistor which includes a current dependent current source, the junction diodes and the collector leakage current. [4]

b. Figure-Q2(b) shows a transistor switching circuit with a resistive load, R_{load}. Switch S_1 is a semiconductor device with switching time shorter than the switching time of the transistor.

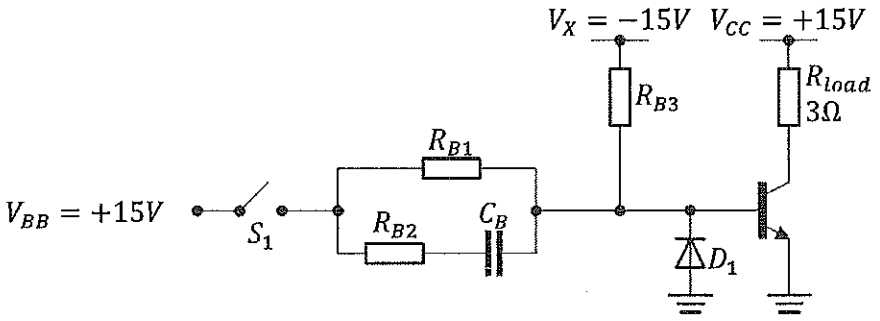


Figure-Q2(b)

i. State the functions of voltage source V_x and diode D_1 respectively. [2]

ii. Explain the function of capacitor C_B. [4]

iii. Given that the transistor has

$\beta_F = 10$ at the moment of turn on

$\beta_F = 20$ at the end of conduction

$V_{BE} = 0.9V$

$V_{CE_{sat}} = 0.02V$

A collector current of 1 μs rise time and a time constant of at least 5 times bigger than the collector current rise time for the capacitor C_B are desirable.

If $|I_{B2}/I_{B1}| = 1$ at turn off, where I_{B1} is the current required to turn on the transistor to achieve the desired level of saturation and I_{B2} is the current required to turn off the transistor rapidly, determine the component values for R_{B1}, R_{B2}, R_{B3} and C_B so that the desired circuit performance is achieved. [7]

Question 3

a. i. Define power electronics. [2]

ii. List any four types of thyristors. [4]

iii. What is a commutation circuit? [2]

iv. List the six general categories of power electronics. [6]

b. Figure-Q3(b) shows an SCR circuit.

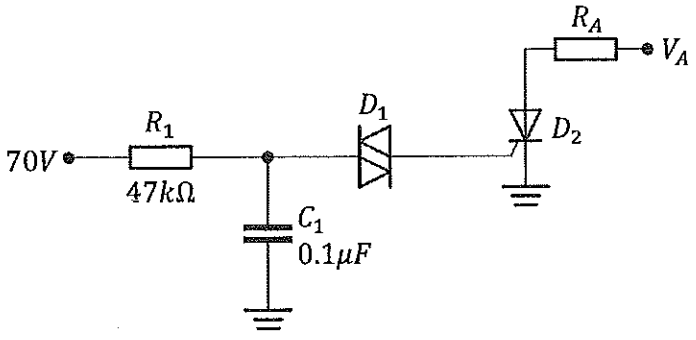


Figure-Q3(b)

i. The SCR and DIAC used in the circuit have the following specifications:

SCR: $V_{GK} = 1V$ (in series with $R_{GK} = 25\Omega$)

DIAC: $V_{ON} = 12V$, $R_{ON} = 4\Omega$, $I_{ON} = 10mA$, $V_{BO} = 30V$

Based on the given specifications, draw an SCR gate circuit model. [3]

ii. Determine the capacitor's peak voltage. [2]

iii. Determine the peak gate current. [3]

iv. Determine the time where the gate current ceases. [3]

Question 4

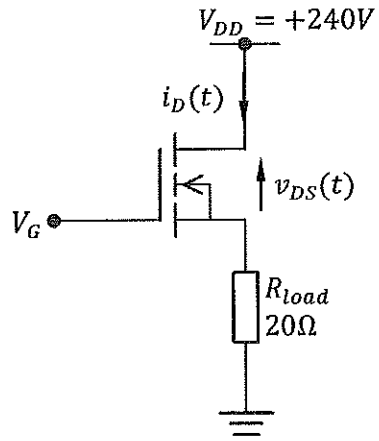
Figure-Q4(i) shows a simple MOSFET based switching circuit. The wave shape of V_G is show in Figure-Q4(ii). The MOSFET has the following specifications:

Drain current rise time, $t_r = 2\mu s$

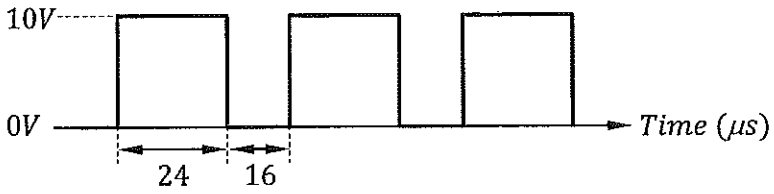
Drain current fall time, $t_f = 3\ \mu s$

$R_{DS(ON)} = 1\Omega$

Drain-source leakage current, $I_{DSS} = 3\ mA$



(i) MOSFET switching circuit.



(ii) Wave shape of V_G.

Figure-Q4

a. Calculate the steady-state load current, $I_{D(max)}$ during ON state. [2]

b. Calculate the saturated voltage across the drain and source terminals, $V_{DS(sat)}$. [2]

c. Assume piecewise linear operation, sketch the respective timing diagram for $i_D(t)$ and $v_{DS}(t)$, synchronized with the waveform of V_G. [6]

d. Show that the maximum power dissipated by the MOSFET when $V_G = 10\,V$ is,

$$P_{D_{ON}(max)} = \frac{I_{D(max)}V_{DD}^2}{4[V_{DD} - V_{DS(sat)}]}$$

Hence, calculate the maximum transistor power dissipation during this period of time. [15]

Question 5

Figure-Q5 shows a single-phase controlled rectifier circuit with a resistive load.

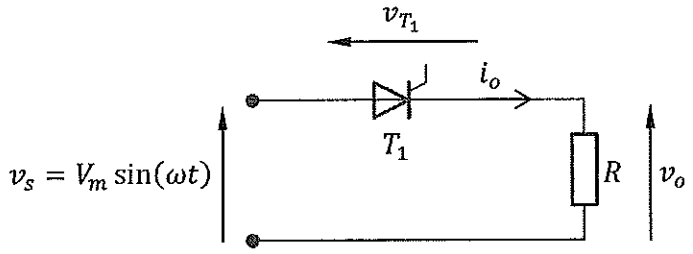


Figure-Q5

a. Sketch the timing diagrams of v_o, i_o and v_{T_1} for one complete cycle of v_s. Assume that thyristor T_1 is fired at an arbitrary angle, α such that $0 \leq \alpha \leq \pi/2$. [6]

b. Derive the average output voltage, $V_{o(DC)}$ expression in Figure-Q5. Hence, calculate the average output voltage if $V_m = 339\,V$ and $\alpha = \pi/3$ radian. [8]

c. i. Derive the rms output voltage, $V_{o(rms)}$ expression in Figure-Q5. Hence, calculate the rms output voltage if again $V_m = 339\ V$ and $\alpha = \pi/3$ radian. [7]

ii. Calculate the rectification efficiency of the circuit in Figure-Q5 base on the firing angle and peak input voltage in part (c)(i). [4]

Question 6

a. Figure-Q6(a) shows a simple transistor switching circuit controlling energy delivered to the inductive load.

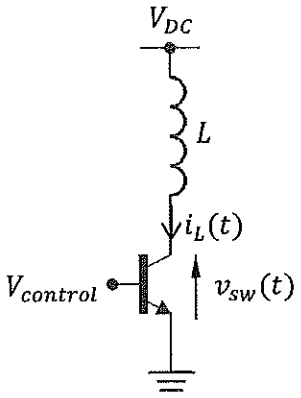


Figure-Q6(a)

Quantitatively explain the consequences of turning off the switching element in Figure-Q6(a) from its saturation state. [6]

b. i. Explain the two basic functions of a snubber circuit. [4]

ii. Draw a RCD snubber circuit onto the circuit in Figure-Q6(a) that will improve the performance of the circuit. [3]

iii. Explain the operation of the RCD snubber circuit drawn in part (b)(ii) to improve the performance of the circuit. [3]

c. i. Explain the method where power transistors increase the rate at which heat is removed from the devices. [3]

ii. Sketch a power derating curve for a power transistor. Label the axes clearly. [2]

iii. A power transistor has a maximum collector dissipation of 4W for an ambient temperature of 30°C. If the maximum junction temperature is 170°C and the thermal resistance θ_{JS} between junction (device) and heat sink is 4°C/W, calculate the maximum possible thermal resistance for the heat sink. [4]

~ The End ~

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