



FINAL
Examination Paper

(COVER PAGE)

Session : April 2016

Programme : Diploma in Electrical and Electronic Engineering (DEEI)

Course : EEE 2105: Introduction to Microprocessors

Date of Examination : 30 July 2016, Saturday

Time : 8.00am – 10.00am Reading Time : Nil

Duration : 2 Hours

Special Instructions :

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL

Materials permitted :
Non-Programmable Scientific Calculator

Materials provided :
Appendix A (8086 Instruction Set Summary), Appendix B (ASCII Table),
Appendix C (8255 PPI), Appendix D (8253/8254 PIT), Appendix E (8259 PIC)

Examiner(s) : Mr. Steven Khoo Boo Tap

Moderator : Dr. Mandeep Singh

This paper consists of 11 printed pages, including the cover page.

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DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING (DEEI)
 EEE2105: INTRODUCTION TO MICROPROCESSORS
 FINAL EXAMINATION: APR2016 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

- (a) Referring to Program 1(a) as shown in Figure Q1, the equivalent machine code for JNZ LOOP1 is 75 FA. If JNZ operation code is 75, explain how LOOP1 is equivalent to FA. Justify your answer with the aid diagram. Show all working clearly.

	MOV CL, 04H
LOOP1:	INC DL
	DEC CL
	JNZ LOOP1
	JMP LOOP2
	ADD AL, AL
LOOP2:	HLT

Figure Q1: Program 1(a)

(7 marks)

- (b) Comment on the validity of the following instructions. For those invalid instructions, explain why. For those valid instructions, state the addressing mode.

(i) MOV BX, [AX]

(2 marks)

(ii) MOV DL, [BX][BP][SI][DI] 11H

(2 marks)

(iii) MOV CL, ES:[BX]

(2 marks)

(iv) MOV AL, [BX+0AH]

(2 marks)

- (c) Perform the following number system transformation. Show all working clearly.
- (i) $[3020.3020_8 - 1002.1002_8]$ to decimal equivalent with 9 decimal points accuracy. (3 marks)
 - (ii) $[106.01_8 \times 1.6_8]$ to binary equivalent with 11 binary points accuracy. (4 marks)
 - (iii) $[163.0703125_{10} - 11.101_8]$ to hexadecimal equivalent with 3 hexadecimal points accuracy. (3 marks)

Question 2

- (a) The bus cycle of the 8088 microprocessor consists of at least FOUR clock periods, namely T_1 , T_2 , T_3 and T_4 . Discuss in detail what is happening in each T-state for a read bus cycle of memory in 8088.
- (i) During T_1 cycle. (3 marks)
 - (ii) During T_2 cycle. (3 marks)
 - (iii) During T_3 cycle. (1 mark)
 - (iv) During T_4 cycle. (2 marks)
- (b) What is the different between JMP (Unconditional Jump) and CALL (Unconditional Call) instructions? Provide FOUR (4) detail comparisons. Illustrate clearly using an appropriate example to show the differences. Use same data for the comparison of both the instruction. (6 marks)

- (c) At a certain moment the state of an 8086 microprocessor based system is as follows: (All values are in Hexadecimal)

Registers			Memory			
	H	L	9000B	12	4010E	6F
AX	2C	10	9000A	34	4010D	2D
BX	00	14	90009	56	4010C	C1
CX	10	01	90008	78	4010B	25
DX	2B	33	90007	9A	4010A	3F
CS	05	00	90006	BA	40109	12
DS	90	00	90005	DE	40108	FF
SS	30	10	90004	F0	40107	FC
ES	61	00	90003	21	40106	E1
BP	00	1F	90002	43	40105	10
SP	00	08	90001	09	40104	00
IP	11	0D	90000	67	40103	36
SI	21	34	8FFFF	54	40102	21
DI	FF	FF	8FFFE	DF	40101	88

- (i) What is the physical address of the next instruction to be executed? (2 marks)
- (ii) What is the physical address of the top of the stack? (2 marks)
- (iii) Draw a memory map for the 8086 microprocessor, indicating clearly the start and end addresses of the segments. (3 marks)
- (iv) Provide the registers and memory locations that are effected, and their new values after the execution of `ADD [BX - 0EH], AX`, also state the number of bytes used for this instruction. (3 marks)

Question 3

- (a) The 8255 PPI is configured as shown in Figure 3(a). Write a program to count the number of 'ones' in the incoming data received from port C continuously via 8255 PPI. The results will be sent to port A if the count result is odd and sent to port B if the count result is even. Assume the configuration below is using Mode 0. Also, include comments for any instruction used. The program length should be as minimum as possible. (12 marks)

Examples of incoming data and the respective action:

- 25_H (00100101) ⇒ send 03_H (Odd) out to port A
- CC_H (11001100) ⇒ send 04_H (Even) out to port B
- 00_H (00000000) ⇒ send 00_H (Even) out to port B
- EF_H (11101111) ⇒ send 07_H (Odd) out to port A
- FF_H (11111111) ⇒ send 08_H (Even) out to port B
- 73_H (01110011) ⇒ send 05_H (Odd) out to port A

[Refer to Appendix C for 8255 PPI Control Word]

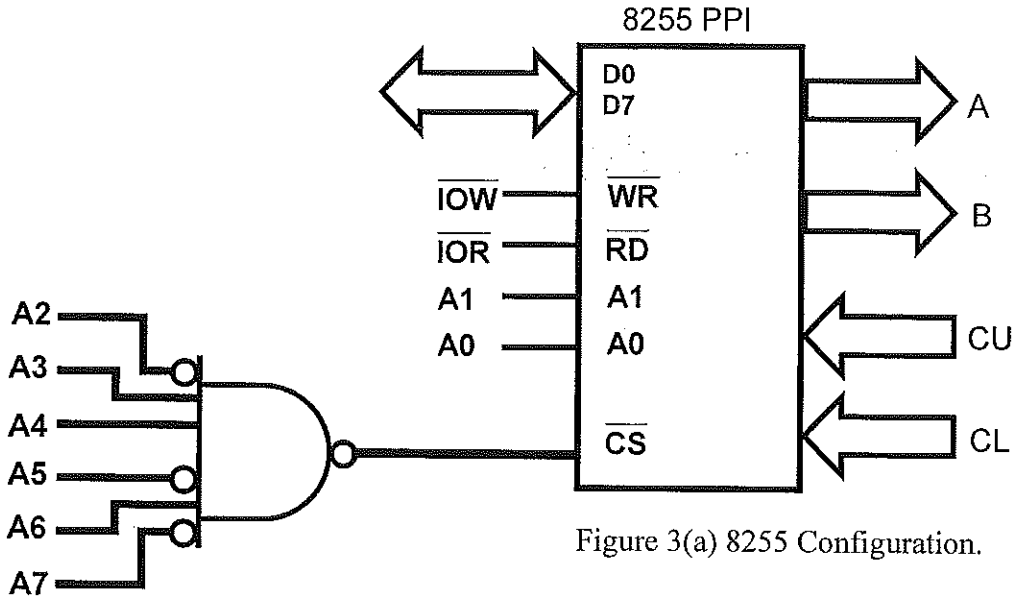


Figure 3(a) 8255 Configuration.

- (b) Suppose that AX = 3024_H, BX = 20CC_H, CX = 8250_H and SP = 0302_H. Determine the value of SP and the values of the data in the registers concerned as we progress through the following instructions. Show step-by-step after each instruction being executed using the aid of diagram as shown below to start with.

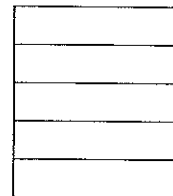
(13 marks)

PUSH CX
 PUSH BX
 PUSH BX
 PUSH AX
 POP AX
 POP BX
 POP CX
 PUSH AX
 POP BX
 POP CX

Stack Memory

SS: 0300_H
 SS: 0301_H
 SS: 0302_H
 SS: 0303_H
 SS: 0304_H

⇒



START
 SP = 0302_H

Question 4

- (a) Given the registers and the memory locations contents of 8086 as follows: (All values are in Hexadecimal).

Registers								
AX	1234H	CS	3010H	DI	0555H			
BX	0404H	DS	5F41H	SI	5060H			
CX	5678H	SS	5F81H	BP	6070H			
DX	789AH	ES	7040H	IP	7100H			

Figure 4(a-1) Registers and the content

Memory																
	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
5F800H	11	22	33	44	55	66	77	88	99	00	A1	B1	C1	D1	E1	F1
5F810H	02	04	45	78	90	11	22	33	44	55	66	77	88	99	00	12
5F820H	34	56	78	90	12	34	56	78	90	12	34	56	78	90	11	22
5F830H	33	44	55	66	77	88	99	00	10	A0	12	34	56	78	9A	BC
5F840H	DE	F0	00	11	00	11	10	21	99	B8	77	33	58	45	33	22
5F850H	25	31	19	00	01	22	20	31	89	C8	66	22	CC	54	44	06
5F860H	DC	F0	20	18	02	33	30	41	79	D8	55	11	BB	67	55	20
5F870H	FE	F1	10	12	03	44	40	51	69	E8	44	AA	55	76	66	21
5F880H	00	FF	00	FF	00	FF	00	60	5F	FF	14	00	FF	F1	80	09

Figure 4(a-2) Memory locations and the content

Perform the following operations. Indicate the result in the register and the content where it is stored. The operations are independent of each other. Show all workings of before and after with appropriate diagram illustration.

- (i) XOR [0416H – 32], DX (3 marks)

- (ii) SUB [BP] + 23 + 23H – 60213o, BH (3 marks)

- (iii) ADD [DI] + 101b + 101o – 101 – 101H, AX (3 marks)

- (iv) AND [SI + BP + 0EB0H – BFADH + 10010000b], CX (3 marks)

- (b) Calculate the time delay taken for the program in Figure 4(b-2) running on 8086 microprocessor at 8-MHz. At a certain moment the state of an 8086 microprocessor based system is as follows: (All values are in Hexadecimal).

Assume that DS register contains 0700H. Show all workings clearly for each instruction.

(13 marks)

[Refer to Appendix A for the cycle time]

Memory																
	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
07700H	08	04	45	78	10	21	22	33	34	25	26	27	28	49	40	14
07800H	02	03	05	01	12	24	56	01	16	00	34	56	98	50	19	62
07900H	07	20	30	40	50	60	70	80	90	02	00	C0	D0	E0	F0	00
07A00H	1D	1C	1B	1A	19	18	55	66	47	46	05	44	43	42	41	0F
07B00H	18	19	23	48	25	26	27	58	29	31	32	35	36	37	38	39

Figure 4(b-1) Random Address Memory

Program	
	MOV AL, 02H
LOOP4:	MOV BL, [0A0AH]
LOOP3:	MOV DX, [0808H]
LOOP2:	MOV CX, [0909H]
LOOP1:	NOP
	NOP
	LOOP LOOP1
	DEC DL
	JNZ LOOP2
	NOP
	DEC BL
	JNZ LOOP3
	XOR AL, AL
	JNZ LOOP4
	HLT

Figure 4(b-2) Coding.

Question 5

- (a) A 5-MHz 8086 microprocessor interfaces with a 3-MHz 8237 DMA. The CPU bus cycle uses one wait state and the bus cycle for the DMA is 4 clocks. Calculate the DMA data transfer rate if the system bus is used alternately by the CPU and DMA. Calculate the answer in Kbytes/s.

(6 marks)

- (b) The 8259 PIC is configured as shown in Figure 5(b). Write a program to initialize the 8259 using the port addresses in Figure 5(b). Assume the ICW1 is 1BH, ICW2 is 58H, no ICW3 and ICW4 is 2FH. Also include comments for any instruction used. (5 marks)

(5 marks)

[Refer to Appendix E for 8259 PIC Control Words]

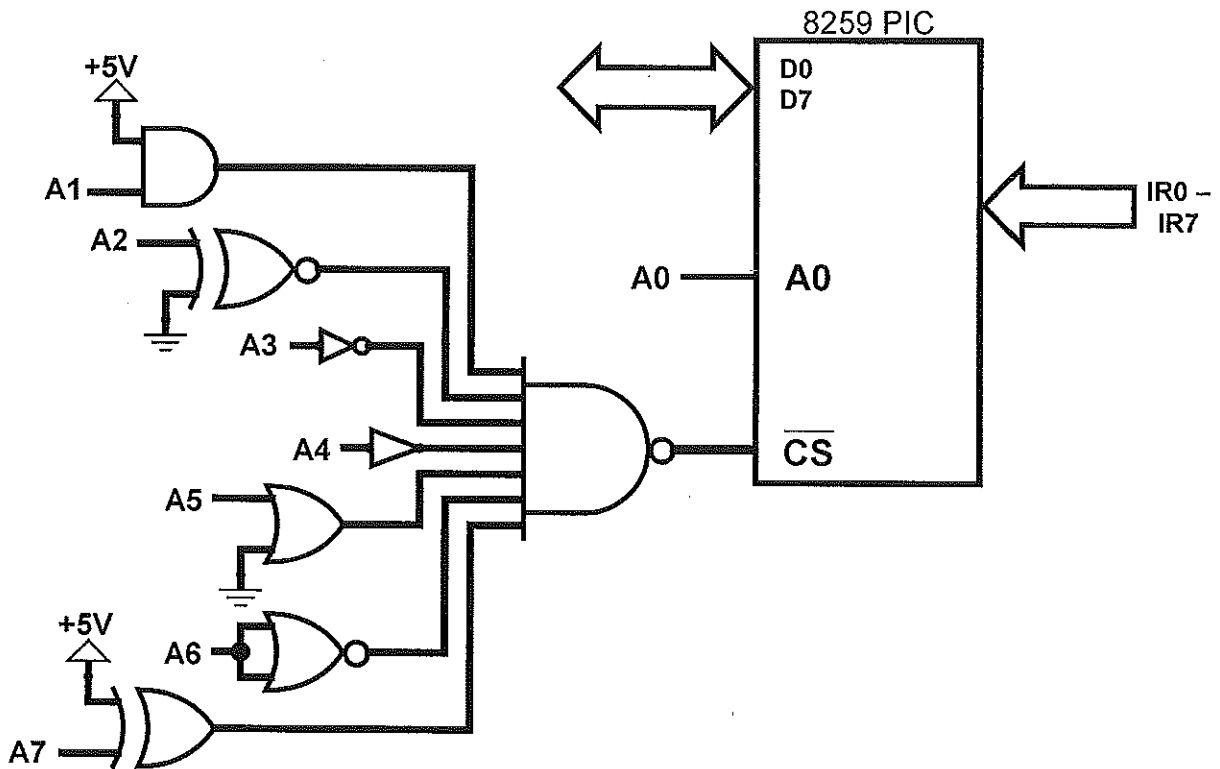


Figure 5(b) 8259 Configuration.

- (c) A transmission system uses asynchronous serial data communication setting as shown in Figure 5(c) to transmit extended ASCII characters message "S", "k", "2", "!" using continuous character transmission via 8250 UART chip. The **LSB** is transmitted first.

Bits per second:	4800
Data bits:	8
Parity:	Odd
Stop bits:	1
Flow control:	None

Figure 5(c) UART setting.

- (i) Draw the frame format of the message transmission with complete labeling. (10 marks)
 - (ii) Calculate the total time it takes to transfer 300 times of the message and the time wasted due to overhead. (4 marks)
- [Refer to Appendix B for ASCII codes]

Question 6

- (a) The 8254 PIT chip is configured as shown in Figure 6(a). CLK1 of counter 1 is 1.19318-MHz and Gate1 is connected to high permanently. Counter 1 generates a periodic pulse every 45.2573- μ s to refresh DRAM memory of the computer. Write assembly instructions to generate this periodic pulse through OUT1. (5 marks)
- [Refer to Appendix D for 8253/8254 PIT Control Word]

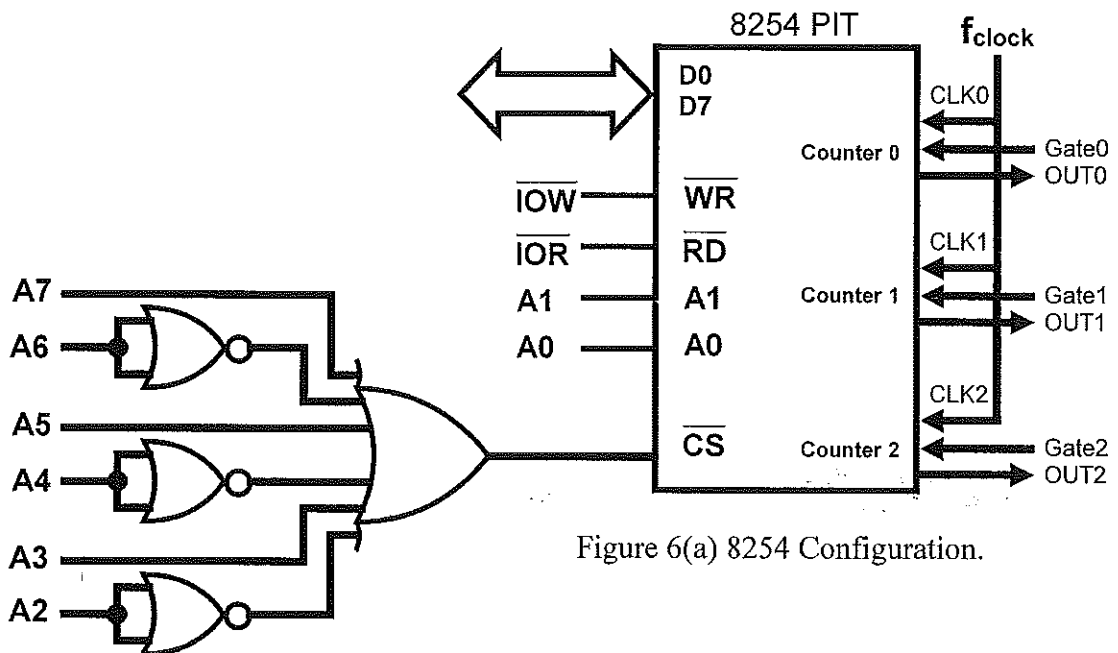


Figure 6(a) 8254 Configuration.

- (b) Figure 6(b-1) shows a TM4100GAD8 Dynamic RAM Module pin configuration. Figure 6(b-2) shows a TM497GU8 Dynamic RAM Module pin configuration.

Determine the:

- (i) total memory capacity of the area (A and B) memory device in Kbits, (4 marks)
- (ii) individual memory organization, (2 marks)
- (iii) number of address pins and number of data pins of each memory device. (4 marks)

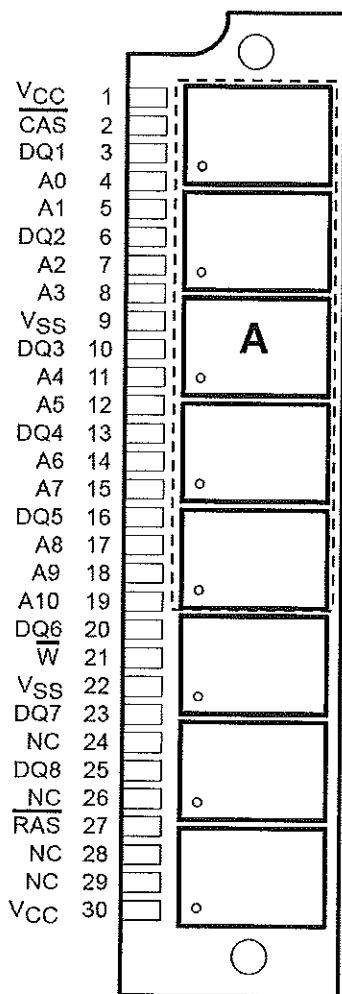


Figure 6(a-1) TM4100GAD8 DRAM Module pin configuration.

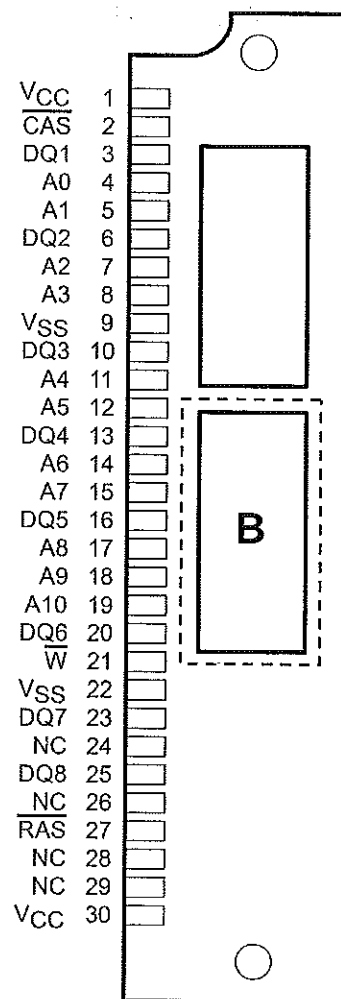


Figure 6(a-2) TM497GU8 DRAM Module pin configuration.

- (c) With the aid of a suitable diagram with details labelling, illustrate step-by-step how DMA can be used to speed up CPU operation during the transfer of data from memory to an I/O device.

The diagram should include the control signals for Microprocessor (CPU), DMA, Memory and I/O Device. The steps describe should be as detail as possible describing all control signals operation.

(10 marks)

- THE END -

EEE2105(F)/Apr16/Steven Khoo/07/04/16

Mnemonic	Description	Clock cycles	Number of bytes	Flags							Page ref.	
				O	D	I	T	S	Z	A		P
	Immediate to accumulator	4	2-3									
CMPS/ CMPSB/ CMPSW	Compare string/ Compare byte string/ Compare word string	Not repeated Repeated	1	x	-	-	-	x	x	x	x	208
CWD	Convert word to double word	22 9+22/rep	1									68
DAA	Decimal adjust for addition	4	1	u	-	-	-	x	x	x	x	74
DAS	Decimal adjust for subtraction	4	1	u	-	-	-	x	x	x	x	74
DEC	Decrement by 1			x	-	-	-	x	x	x	x	69
	16-bit register	2	1									
	8-bit register	3	2									
	Memory	15+EA	2-4									
DIV	Unsigned division			u	-	-	-	u	u	u	u	70
	8-bit register	80-90	2									
	16-bit register	144-162	2									
	8-bit memory	(86-96) +EA	2-4									
	16-bit memory	(150-168) +EA	2-4									
ESC	Escape			-	-	-	-	-	-	-	-	457
	Register	2	2									
	Memory	8+EA	2-4									
HLT	Halt	2	1	-	-	-	-	-	-	-	-	91
IDIV	Integer division			u	-	-	-	u	u	u	u	70
	8-bit register	101-112	2									
	16-bit register	165-184	2									
	8-bit memory	(107-118) +EA	2-4									
	16-bit memory	(171-190) +EA	2-4									
IMUL	Integer multiplication			x	-	-	-	u	u	u	u	70
	8-bit register	80-98	2									
	16-bit register	128-154	2									
	8-bit memory	(86-104) +EA	2-4									
	16-bit memory	(134-160) +EA	2-4									
IN	Input from I/O port			-	-	-	-	-	-	-	-	232
	Fixed port	10	2									
	Variable port	8	1									
INC	Increment by 1			x	-	-	-	x	x	x	x	69
	16-bit register	2	1									
	8-bit register	3	2									
	Memory	15+EA	2-4									
INT	Interrupt			-	-	0	0	-	-	-	-	172

Mnemonic	Description	Clock cycles	Number of bytes	Flags							Page ref.		
				O	D	I	T	S	Z	A		P	C
STI	Set interrupt flag	2	1	-	-	1	-	-	-	-	-	92	
STOS/ STOSB/ STOSW	Store string/ Store byte string/ Store word string		1	-	-	-	-	-	-	-	-	208	
	Not repeated	11											
	Repeated	9+10/rep											
SUB	Subtraction			x	-	-	-	x	x	x	x	65	
	Register from register	3	2										
	Memory from register	9+EA	2-4										
	Register from memory	16+EA	2-4										
	Immediate from accumulator	4	2-3										
	Immediate from register	4	3-4										
	Immediate from memory	17+EA	3-6										
TEST	Test			0	-	-	-	x	x	u	x	0	93
	Register with register	3	2										
	Memory with register	9+EA	2-4										
	Immediate with accumulator	4	2-3										
	Immediate with register	5	3-4										
	Immediate with memory	11+EA	3-6										
WAIT	Wait while TEST pin not asserted	3+5n	1	-	-	-	-	-	-	-	-	457	
XCHG	Exchange			-	-	-	-	-	-	-	-	60	
	Register with accumulator	3	1										
	Register with memory	17+EA	2-4										
	Register with register	4	2										
XLAT/ XLATB	Translate	11	1	-	-	-	-	-	-	-	-	221	
XOR	Logical exclusive OR			0	-	-	-	x	x	u	x	0	93
	Register with register	3	2										
	Memory with register	9+EA	2-4										
	Register with memory	16+EA	2-4										
	Immediate with accumulator	4	2-3										
	Immediate with register	4	3-4										
	Immediate with memory	17+EA	3-6										

EA No. of Clock Cycles

Direct	6
Register indirect	5
Register relative	9
Based indexed	
(BP)+(DI) or (BX)+(SI)	7
(BP)+(SI) or (BX)+(DI)	8
Based indexed relative	
(BP)+(DI)+DISP or (BX)+(SI)+DISP	11
(BP)+(SI)+DISP or (BX)+(DI)+DISP	12

Flag Setting Symbols:

O D I T S Z A P C:

- Not affected
- x Set or cleared according to the result
- u Undefined
- 0 Cleared to 0
- 1 Set to 1
- r Restored from previously saved value

Conditional Jump Instructions

Instruction	Description	Condition	Aliases	Opposite
JC	Jump if carry	Carry = 1	JB, JNAE	JNC
JNC	Jump if no carry	Carry = 0	JNB, JAE	JC
JZ	Jump if zero	Zero = 1	JE	JNZ
JNZ	Jump if not zero	Zero = 0	JNE	JZ
JS	Jump if sign	Sign = 1	-	JNS
JNS	Jump if no sign	Sign = 0	-	JS
JO	Jump if overflow	Overflow = 1	-	JNO
JNO	Jump if no overflow	Overflow = 0	-	JO
JP	Jump if parity	Parity = 1	JPE	JNP
JPE	Jump if parity even	Parity = 1	JP	JPO
JNP	Jump if no parity	Parity = 0	JPO	JP
JPO	Jump if parity odd	Parity = 0	JNP	JPE

Unsigned Comparisons				
Instruction	Description	Condition	Aliases	Opposite
JA	Jump if above (>)	Carry = 0, Zero = 0	JNBE	JNA
JNBE	Jump if not below nor equal (not <=)	Carry = 0, Zero = 0	JA	JBE
JAE	Jump if above or equal (>=)	Carry = 0	JNC, JNB	JNAE
JNB	Jump if not below (not <)	Carry = 0	JNC, JAE	JB
JB	Jump if below (<)	Carry = 1	JC, JNAE	JNB
JNAE	Jump if not above nor equal (not >=)	Carry = 1	JC, JB	JAE
JBE	Jump if below or equal (<=)	Carry = 1 or Zero = 1	JNA	JNBE
JNA	Jump if not above (not >)	Carry = 1 or Zero = 1	JBE	JA
JE	Jump if equal (=)	Zero = 1	JZ	JNE
JNE	Jump if not equal (≠)	Zero = 0	JNZ	JE

Signed Comparisons				
Instruction	Description	Condition	Aliases	Opposite
JG	Jump if greater (>)	Sign = Overflow & Zero = 0	JNLE	JNG
JNLE	Jump if not less than nor equal (not <=)	Sign = Overflow & Zero = 0	JG	JLE
JGE	Jump if greater than or equal (>=)	Sign = Overflow	JNL	JGE
JNL	Jump if not less than (not <)	Sign = Overflow	JGE	JL
JL	Jump if less than (<)	Sign Overflow	JNGE	JNL
JNGE	Jump if not greater nor equal (not >=)	Sign Overflow	JL	JGE
JLE	Jump if less than or equal (<=)	Sign Overflow or Zero = 1	JNG	JNLE
JNG	Jump if not greater than (not >)	Sign Overflow & Zero = 1	JLE	JG
JE	Jump if equal (=)	Zero = 1	JZ	JNE
JNE	Jump if not equal (≠)	Zero = 0	JNZ	JE

8086 Flags Register

|ODITSZAPC| Overflow Flag, Direction Flag, Interrupt Flag, Trap Flag, Sign Flag, Zero Flag, Auxiliary carry Flag, Parity Flag, Carry Flag

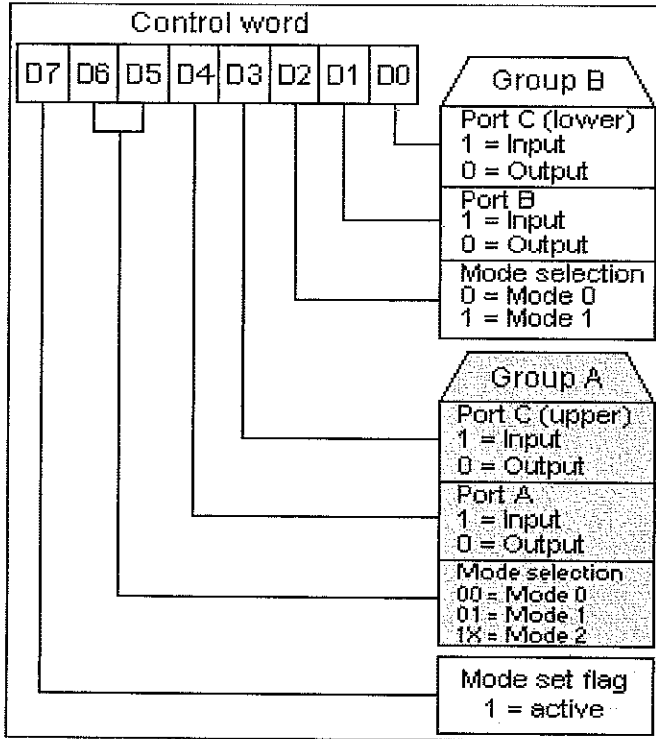
APPENDIX B: ASCII TABLE

ASCII Codes

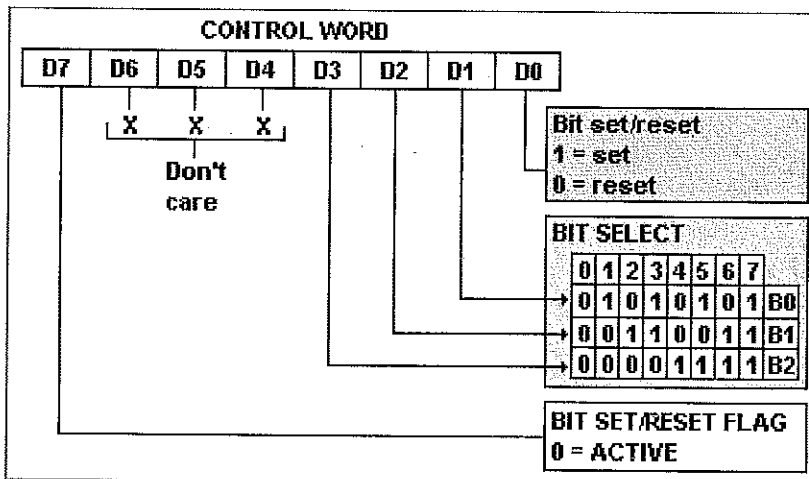
ascii codes															
00:	null	20:	spa	40:	@	60:	`	80:	Ç	A0:	á	C0:	À	E0:	α
01:	␣	21:	!	41:	A	61:	a	81:	ü	A1:	í	C1:	±	E1:	β
02:	␣	22:	"	42:	B	62:	b	82:	é	A2:	ó	C2:	⌈	E2:	Γ
03:	␣	23:	#	43:	C	63:	c	83:	â	A3:	ú	C3:	⌋	E3:	Π
04:	␣	24:	\$	44:	D	64:	d	84:	à	A4:	ñ	C4:	⌋	E4:	Σ
05:	␣	25:	%	45:	E	65:	e	85:	ä	A5:	ñ	C5:	⌋	E5:	σ
06:	␣	26:	&	46:	F	66:	f	86:	å	A6:	ä	C6:	⌋	E6:	μ
07:	beep	27:	'	47:	G	67:	g	87:	æ	A7:	æ	C7:	⌋	E7:	τ
08:	back	28:	<	48:	H	68:	h	88:	ç	A8:	ç	C8:	⌋	E8:	θ
09:	tab	29:	>	49:	I	69:	i	89:	ê	A9:	ê	C9:	⌋	E9:	Θ
0A:	newl	2A:	*	4A:	J	6A:	j	8A:	ë	AA:	ë	CA:	⌋	EA:	Ω
0B:	δ	2B:	+	4B:	K	6B:	k	8B:	è	AB:	è	CB:	⌋	EB:	δ
0C:	♀	2C:	,	4C:	L	6C:	l	8C:	é	AC:	é	CC:	⌋	EC:	ω
0D:	cret	2D:	-	4D:	M	6D:	m	8D:	ì	AD:	ì	CD:	⌋	ED:	ø
0E:	⌘	2E:	.	4E:	N	6E:	n	8E:	ï	AE:	ï	CE:	⌋	EE:	€
0F:	*	2F:	/	4F:	O	6F:	o	8F:	â	AF:	»	CF:	⌋	EF:	€
10:	␣	30:	0	50:	P	70:	p	90:	é	B0:	⌋	D0:	⌋	F0:	±
11:	␣	31:	1	51:	Q	71:	q	91:	æ	B1:	⌋	D1:	⌋	F1:	±
12:	␣	32:	2	52:	R	72:	r	92:	æ	B2:	⌋	D2:	⌋	F2:	±
13:	!!	33:	3	53:	S	73:	s	93:	ö	B3:	⌋	D3:	⌋	F3:	±
14:	¶	34:	4	54:	T	74:	t	94:	ö	B4:	⌋	D4:	⌋	F4:	±
15:	§	35:	5	55:	U	75:	u	95:	ö	B5:	⌋	D5:	⌋	F5:	±
16:	±	36:	6	56:	V	76:	v	96:	û	B6:	⌋	D6:	⌋	F6:	±
17:	±	37:	7	57:	W	77:	w	97:	û	B7:	⌋	D7:	⌋	F7:	±
18:	↑	38:	8	58:	X	78:	x	98:	ÿ	B8:	⌋	D8:	⌋	F8:	±
19:	↓	39:	9	59:	Y	79:	y	99:	ÿ	B9:	⌋	D9:	⌋	F9:	±
1A:	→	3A:	:	5A:	Z	7A:	z	9A:	ÿ	BA:	⌋	DA:	⌋	FA:	±
1B:	←	3B:	;	5B:	[7B:	<	9B:	ÿ	BB:	⌋	DB:	⌋	FB:	±
1C:	⌊	3C:	<	5C:	\	7C:		9C:	ÿ	BC:	⌋	DC:	⌋	FC:	±
1D:	⌋	3D:	=	5D:]	7D:	>	9D:	ÿ	BD:	⌋	DD:	⌋	FD:	±
1E:	▲	3E:	>	5E:	^	7E:	~	9E:	ÿ	BE:	⌋	DE:	⌋	FE:	±
1F:	▼	3F:	?	5F:	_	7F:	Δ	9F:	ÿ	BF:	⌋	DF:	⌋	FF:	res

APPENDIX C: 8255 PPI

Control Word



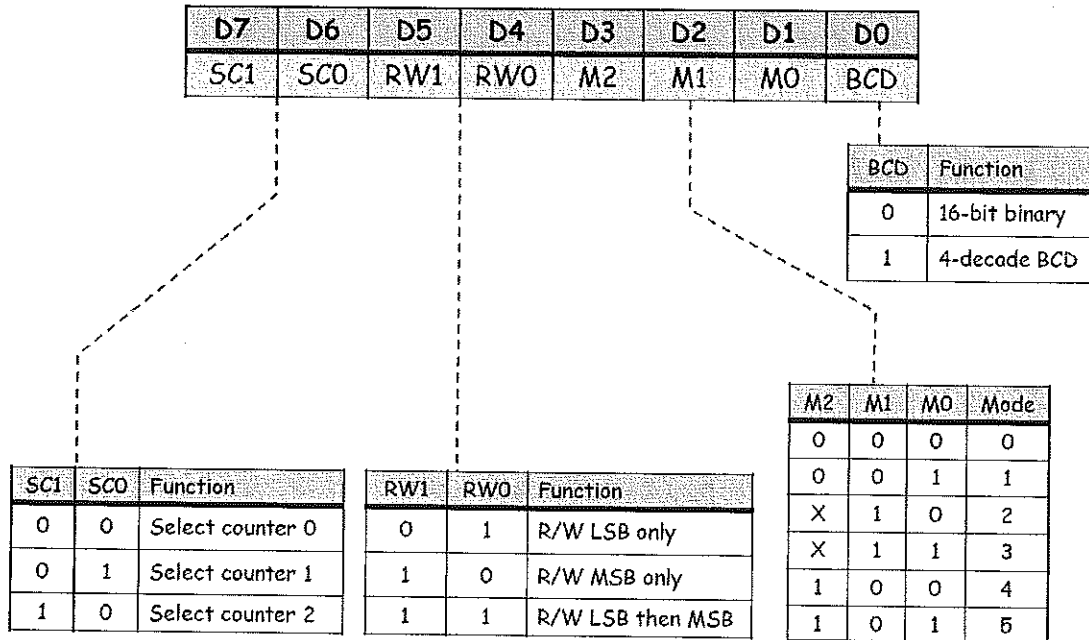
8255 Control Word Format (I/O Mode)



BSR Control Word

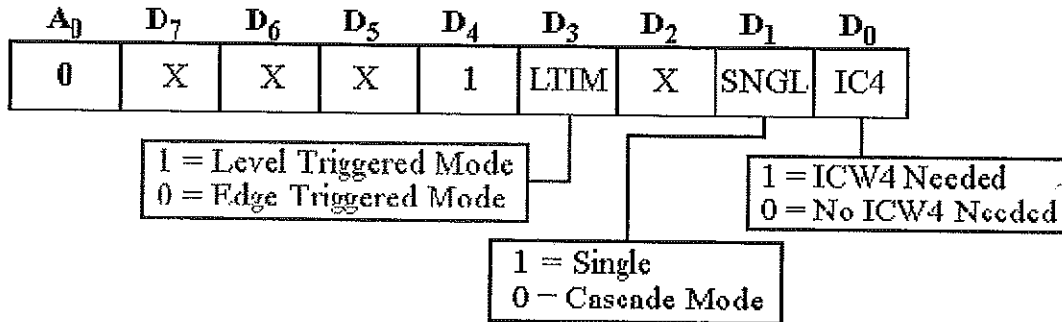
APPENDIX D: 8253/8254 PIT

Control Word



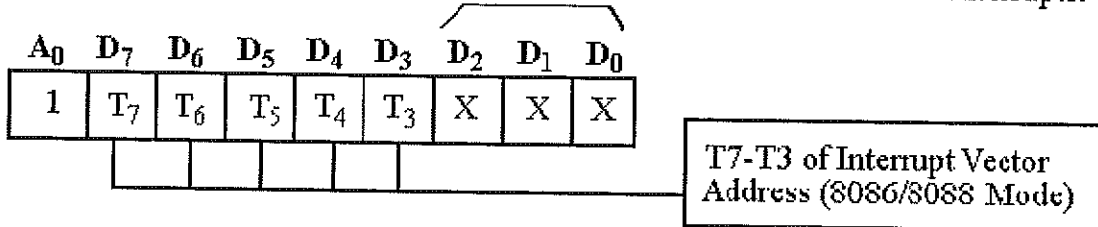
APPENDIX E: 8259 PIC

ICW1:

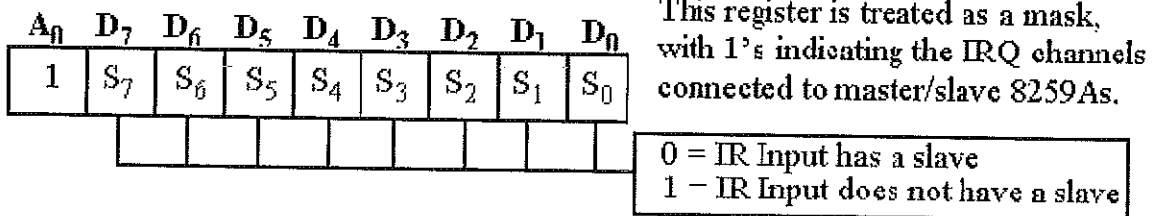


ICW2:

Low order bits are 0 since there are 8 interrupts.



ICW3:



ICW4:

